

### FEATURES

- Low Offset Voltage ..... 0.3mV Typ, 0.8mV Max
- Low Offset Current ..... 0.3nA Typ, 3nA Max
- Low Bias Current ..... 28nA Typ, 50nA Max
- Low Offset Drift .....  $1\mu\text{V}/^\circ\text{C}$ ,  $4\text{pA}/^\circ\text{C}$
- High Gain ..... 200,000 Min
- High CMRR ..... 110dB Typ, 94dB Min
- High Input Impedance .....  $16\text{M}\Omega$
- Fast Response Time ..... 190ns Typ, 270ns Max
- Standard Power Supplies .....  $+5\text{V}$  or  $\pm 5\text{V}$  to  $\pm 18\text{V}$
- Guaranteed Operation from Single  $+5\text{V}$
- No Pull-Up Resistor Required for TTL Drive
- Wired OR Capability
- Fits 111, 106, 710 Sockets
- Easy Offset Nulling ..... Single  $2\text{k}\Omega$  Potentiometer
- Easy to Use ..... Free from Oscillations
- Available in Die Form

### ORDERING INFORMATION†

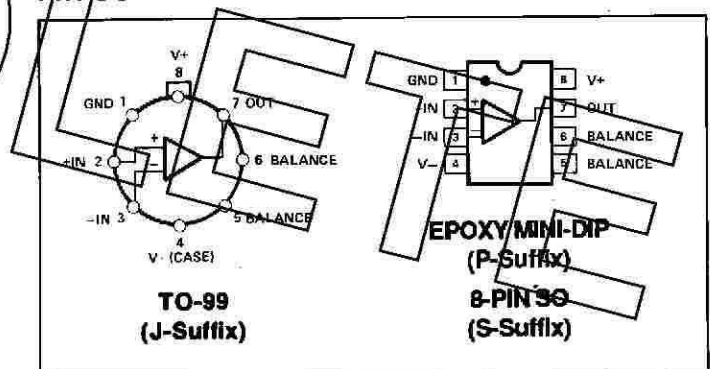
$T_A = +25^\circ\text{C}$ $V_{OS}$ MAX (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-99	PLASTIC 8-PIN	
0.8	—	CMP02EP	COM
2.8	CMP02CJ	CMP02CP	XIND

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

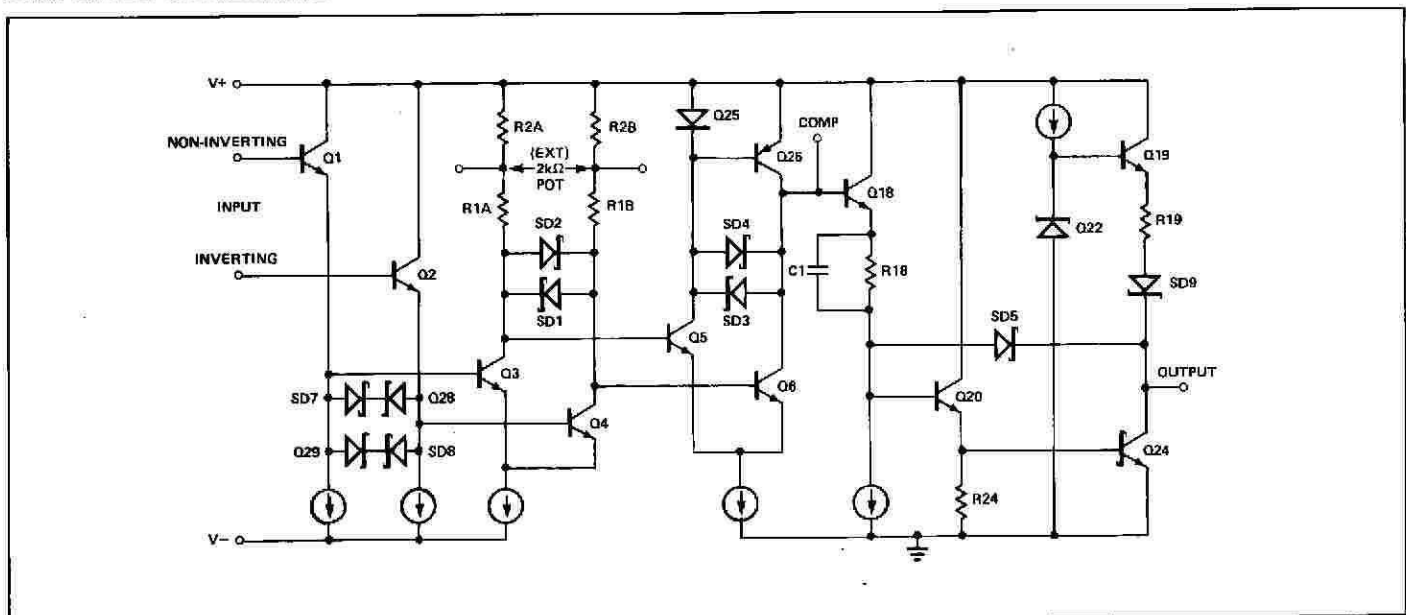
### GENERAL DESCRIPTION

The CMP-02 is a monolithic low input current comparator using an advanced NPN-Schottky Barrier Diode process. It features superior input characteristics with extremely low offset voltage, offset current, bias current and temperature drift. High common-mode and power supply rejection plus good response time contribute to excellent performance in the most demanding applications. The balanced offset nulling, large output drive, and wired-OR capability combined with internal pull-up maximize application convenience. The CMP-02 is capable of operating over a wide range of supply voltages, including single plus 5 volt supply operation, and is pin-compatible to earlier 111, 106, and 710 types. For applications requiring faster response time, please refer to the CMP-01 fast precision comparator data sheet.

### PIN CONNECTIONS



### SIMPLIFIED SCHEMATIC



# CMP-02

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage, $V_+$ to $V_-$	36V
Output to Ground	-5V to +32V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Positive Supply Voltage to Ground	30V
Positive Supply Voltage to Offset Null	0 to 2V
Differential Input Voltage	$\pm 11V$
Input Voltage ( $V_S = \pm 15V$ )	$\pm 15V$
Output Sink Current (Continuous Operation)	75mA
Operating Temperature Range	
CMP-02E	0°C to +70°C
CMP-02C	-40°C to +85°C
Junction Temperature ( $T_J$ )	-65°C to +150°C
Storage Temperature Range	-65°C to +150°C
P-Suffix	-65°C to +125°C

Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration	
To Ground	Indefinite
To $V_+$	1 Minute

PACKAGE TYPE	$\theta_{JA}$ (Note 2)	$\theta_{JC}$	UNITS
TO-98 (J)	150	18	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

### NOTES:

- Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
- $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for TO and P-DIP packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO package.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ , $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-02E			CMP-02C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$	$R_S \leq 5k\Omega$ , (Note 1)	—	0.3	0.8	—	0.4	2.8	mV
Input Offset Voltage	$V_{OS}$	$R_S \leq 50k\Omega$ , (Note 1)	—	0.3	0.9	—	0.4	3	mV
Input Offset Current	$I_{OS}$	(Note 1)	—	0.3	3.0	—	0.4	15	nA
Input Bias Current	$I_B$		—	28	50	—	35	100	nA
Differential Input Resistance	$R_{IN}$	(Note 2)	1.7	3	—	0.8	2	—	M $\Omega$
Voltage Gain	$A_V$	$V_O = 1$ to 3V, (Note 2)	200	500	—	100	500	—	V/mV
Response Time (Note 3)	$t_r$	100mV step, 5mV Overdrive No Load (No Pull-Up)	—	190	270	—	190	270	ns
		5k $\Omega$ to 5V (Pull-Up)	—	190	—	—	190	—	—
		TTL Fan-Out = 4, No Pull-Up	—	190	—	—	190	—	—
Input Slew Rate			—	15	—	—	15	—	V/ $\mu$ s
Input Voltage Range	CMVR		$\pm 12.5$	$\pm 13.0$	—	$\pm 12.5$	$\pm 13.0$	—	V
Common-Mode Rejection Ratio	CMRR		94	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 18V$ , $-18V \leq V_{S-} \leq 0V$	80	100	—	74	98	—	dB
Positive Output Voltage	$V_{OH}$	$V_{IN} \geq 3mV$ , $I_O = 320\mu A$	2.4	3.2	—	—	—	—	V
		$V_{IN} \geq 3mV$ , $I_O = 240\mu A$	—	—	—	2.4	3.4	—	—
		$V_{IN} \geq 3mV$ , $I_O = 0mA$	2.4	4.8	—	2.4	4.8	—	—
Saturation Voltage	$V_{OL}$	$V_{IN} \leq -10mV$ , $I_{sink} = 0mA$	—	0.16	0.40	—	0.16	0.40	V
		$V_{IN} \leq -10mV$ , $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.31	0.45	—
		$V_{IN} \leq -10mV$ , $I_{sink} \leq 12mA$ (CMP-02 only)	—	0.36	0.5	—	—	—	—
Output Leakage Current	$I_{LEAK}$	$V_{IN} \geq 10mV$ , $V_O = +30V$	—	0.03	2.0	—	0.05	8.0	$\mu A$
Positive Supply Current	$I_+$	$V_{IN} \leq -10mV$	—	5.5	8.0	—	5.6	8.5	mA
Negative Supply Current	$I_-$	$V_{IN} \leq -10mV$	—	1.1	2.2	—	1.2	2.2	mA
Power Dissipation	$P_d$	$V_{IN} \leq -10mV$	—	99	153	—	102	161	mW
Offset Voltage Adjustment Range		Nulling Pot $\geq 2k\Omega$	—	$\pm 5$	—	—	$\pm 5$	—	mV

### NOTES:

- These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k $\Omega$  load tied to +5V; thus, these parameters define an error band which takes into

account the worst case effects of voltage gain and input impedance.

- Guaranteed by design.
- Sample tested.

**ELECTRICAL CHARACTERISTICS** at  $V_S = 5V$ ,  $V_{S-} = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-02E			CMP-02C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$	$R_S \leq 5k\Omega$ , (Note 1)	—	0.4	1.5	—	0.5	3.5	mV
Input Offset Current	$I_{OS}$	(Note 1)	—	0.25	3	—	0.35	14	nA
Input Bias Current	$I_B$		—	24	45	—	30	90	nA
Voltage Gain	$A_V$	$V_O = 1$ to $3V$	—	50	—	—	50	—	V/mV
Response Time	$t_r$	100mV Step, 5mV Overdrive	—	250	—	—	250	—	ns
		5k $\Omega$ to 5V (Pull-Up)	—	250	—	—	250	—	
		TTL Fan-Out = 4, 5k $\Omega$ to 5V	—	250	—	—	250	—	
Input Voltage Range	CMVR		1.8-3.5	1.7-3.8	—	1.8-3.5	1.7-3.8	—	V
Saturation Voltage	$V_{OL}$	$V_{IN} \leq -3.5mV$ , $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.3	0.45	V
Positive Supply Current	$I_+$	$V_{IN} \leq -10mV$	—	2.2	3	—	2.3	3.6	mA
Power Dissipation	$P_d$	$V_{IN} \leq -10mV$	—	11	15	—	11.5	18	mW

**NOTE:**

- These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k $\Omega$  load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.

**ELECTRICAL CHARACTERISTICS**  $V_S = \pm 15V$ ,  $0^\circ C \leq T_A \leq +70^\circ C$  for E Grade,  $-40^\circ C \leq T_A \leq +85^\circ C$  for C Grade, unless otherwise noted.

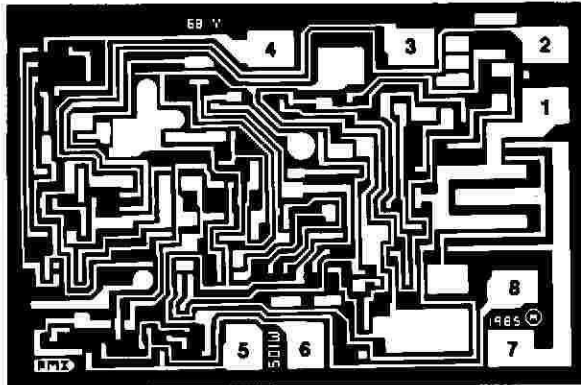
PARAMETER	SYMBOL	CONDITIONS	CMP-02E			CMP-02C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$	$R_S \leq 5k\Omega$ , (Note 1)	—	0.4	1.4	—	0.5	1.5	mV
		$V_{S+} = 5V$ , $V_{S-} = 0V$ , (Note 1)	—	0.5	2.4	—	0.6	4.3	
Average Input Offset Voltage Drift									
Without External Trim	$TCV_{OS}$	$R_S = 50\Omega$	—	1.5	—	—	1.8	—	$\mu V/^\circ C$
With External Trim	$TCV_{OSn}$	$R_S = 50\Omega$	—	1	—	—	1.2	—	$\mu V/^\circ C$
Input Offset Current	$I_{OS}$	$T_A = +70^\circ C$ , (Note 1)	—	0.3	3	—	0.4	15	nA
		$T_A = 0^\circ C$ , (Note 1)	—	0.4	6	—	0.5	25	
Average Input Offset Current Drift	$TCI_{OS}$	$+25^\circ C \leq T_A \leq +70^\circ C$	—	2	—	—	3	—	$pA/^\circ C$
		$0^\circ C \leq T_A \leq +25^\circ C$	—	4	—	—	5	—	
Input Bias Current	$I_B$	$T_A = +70^\circ C$	—	26	50	—	33	100	nA
		$T_A = 0^\circ C$	—	34	80	—	42	160	
Voltage Gain	$A_V$	$V_O = 1$ to $3V$ , (Note 2)	100	500	—	70	500	—	V/mV
Response Time	$t_r$	100mV Step, 5mV Overdrive	—	225	—	—	225	—	ns
		$T_A = +70^\circ C$ , No Load	—	180	—	—	180	—	
		$T_A = 0^\circ C$ , No Load	—	180	—	—	180	—	
Input Voltage Range	CMVR		$\pm 12.0$	$\pm 13$	—	$\pm 12$	$\pm 13$	—	V
Common-Mode Rejection Ratio	CMRR		90	108	—	86	108	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$ , $-15V \leq V_{S-} \leq 0V$	77	98	—	70	88	—	dB
Positive Output Voltage	$V_{OH}$	$V_{IN} \geq 4mV$ , $I_O = 200\mu A$	2.4	3.2	—	2.4	3.2	—	V
Saturation Voltage	$V_{OL}$	$V_{IN} \leq -10mV$ , $I_{sink} = 0$	—	0.17	0.4	—	0.17	0.4	V
		$V_{IN} \leq -10mV$ , $I_{sink} = 6.4mA$	—	0.30	0.5	—	0.31	0.5	

**NOTES:**

- These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k $\Omega$  load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
- Guaranteed by design.

# CMP-02

## DICE CHARACTERISTICS



1. GROUND
2. NONINVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY (SUBSTRATE)
5. BALANCE
6. BALANCE
7. OUTPUT
8. POSITIVE SUPPLY

DIE SIZE 0.065 × 0.043 inch, 2730 sq. mils  
(1.651 × 1.094 mm, 1.806 sq. mm)

### WAFER TEST LIMITS at $V_S = \pm 15V$ , $T_A = 25^\circ C$ .

PARAMETER	SYMBOL	CONDITIONS	CMP-02N LIMIT	CMP-02GR LIMIT	UNITS
Input Offset Voltage	$V_{OS}$	$R_S \leq 5k\Omega$ $R_S \leq 50k\Omega$	0.8 0.9	2.8 3	mV MAX
Input Offset Current	$I_{OS}$		3	15	nA MAX
Input Bias Current	$I_B$		50	100	nA MAX
Differential Input Resistance	$R_{IN}$		1.7	0.9	MOHMIN
Input Voltage Range	CMVR		$\pm 12.5$	$\pm 2.5$	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	94	90	dB MIN
Power Supply Rejection Ratio	PSRR	$5V \leq V_S + \leq 18V$ $-18V \leq V_S - \leq 0V$	80	74	dB MIN
Positive Output Voltage	$V_{OH}$	$V_{IN} \geq 3mV$ , $I_O = 320\mu A$ $V_{IN} \geq 3mV$ , $I_O = 240\mu A$	2.4 —	— 2.4	V MIN
Saturation Voltage	$V_{OL}$	$I_{sink} = 6.4mA$	0.45	0.45	V MAX
Output Leakage Current	$I_{LEAK}$	$V_{IN} \geq 10mV$ , $V_O = 30V$	2	8	$\mu A$ MAX
Positive Supply Current	$I_+$	$V_{IN} \leq -10mV$	8	8.5	mA MAX
Negative Supply Current	$I_-$	$V_{IN} \leq -10mV$	2.2	2.2	mA MAX
Power Consumption	$P_d$	$V_{IN} \leq -10mV$	153	161	mW MAX

### WAFER TEST LIMITS at $V_{S+} = 5V$ and $V_{S-} = 0V$ , $T_A = 25^\circ C$ .

PARAMETER	SYMBOL	CONDITIONS	CMP-02N LIMIT	CMP-02GR LIMIT	UNITS
Input Offset Voltage	$V_{OS}$	$R_S \leq 5k\Omega$	1.5	3.5	mV MAX
Input Offset Current	$I_{OS}$		3	14	nA MAX

#### NOTE:

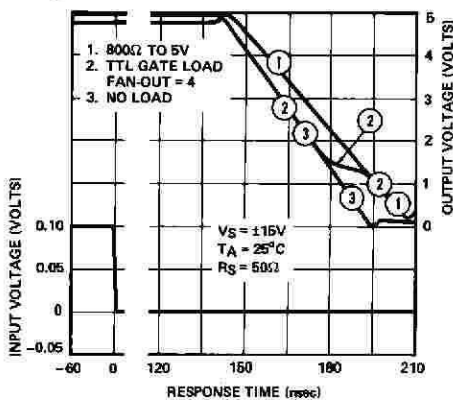
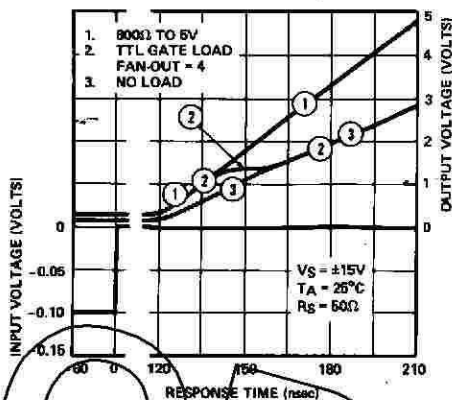
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

### TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ .

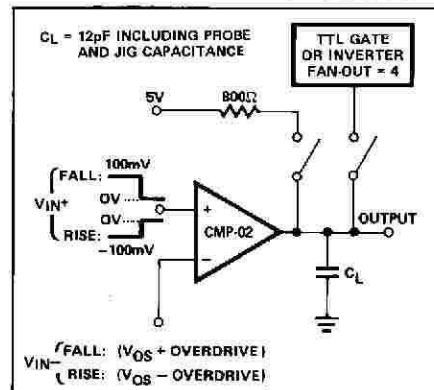
PARAMETER	SYMBOL	CONDITIONS	CMP-02N TYPICAL	CMP-02GR TYPICAL	UNITS
Average Input Offset Voltage Drift	$TCV_{OS}$	$R_S = 50\Omega$	1.5	1.8	$\mu V/^\circ C$
Average Input Offset Current Drift	$TCI_{OS}$		4	5	$pA/^\circ C$
Response Time	$t_r$	100mV Step, 5mV Overdrive No Load (No Pull-Up), $T_A = 25^\circ C$	190	190	ns

TYPICAL PERFORMANCE CHARACTERISTICS

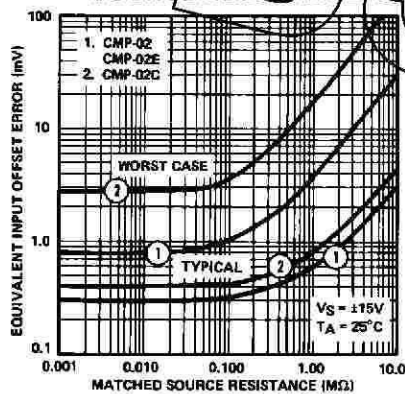
RESPONSE TIME,  
100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS



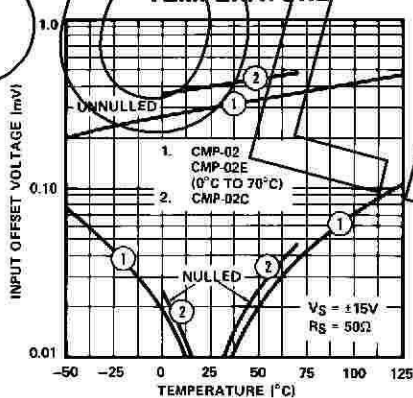
RESPONSE TIME TEST CIRCUIT



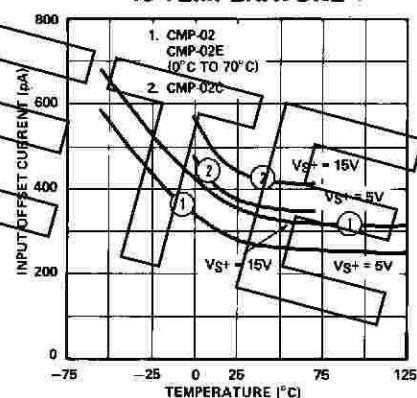
INPUT OFFSET ERROR vs  
SOURCE RESISTANCE



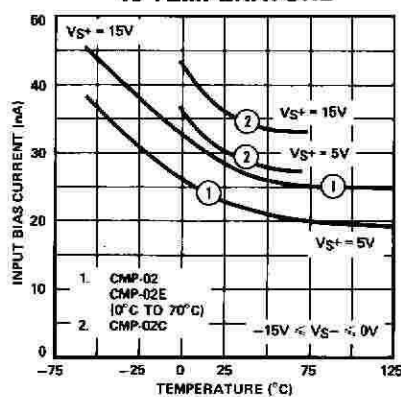
OFFSET VOLTAGE vs  
TEMPERATURE



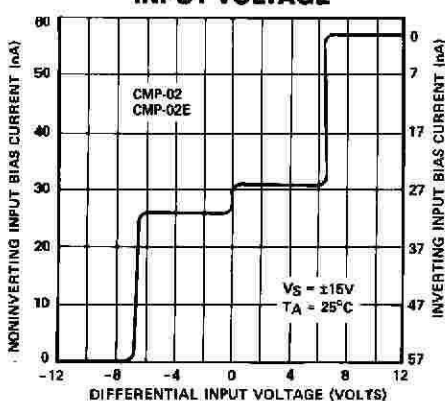
INPUT OFFSET CURRENT  
vs TEMPERATURE



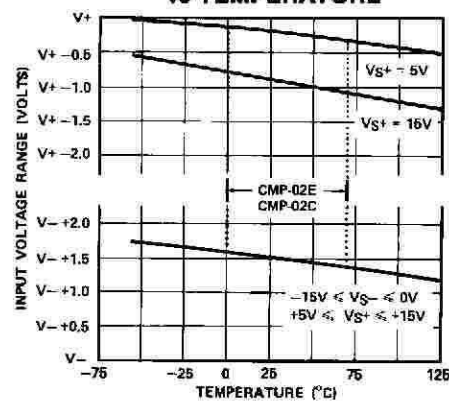
INPUT BIAS CURRENT  
vs TEMPERATURE



INPUT BIAS CURRENT  
vs DIFFERENTIAL  
INPUT VOLTAGE



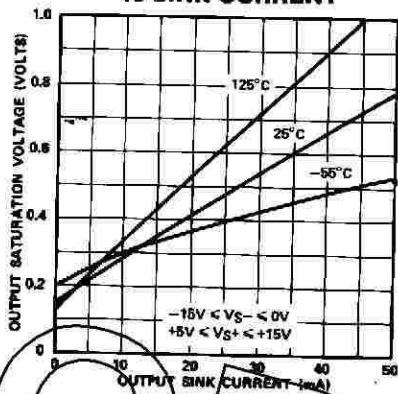
INPUT VOLTAGE RANGE  
vs TEMPERATURE



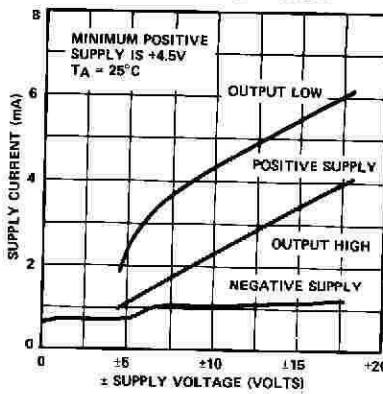
# CMP-02

## TYPICAL PERFORMANCE CHARACTERISTICS

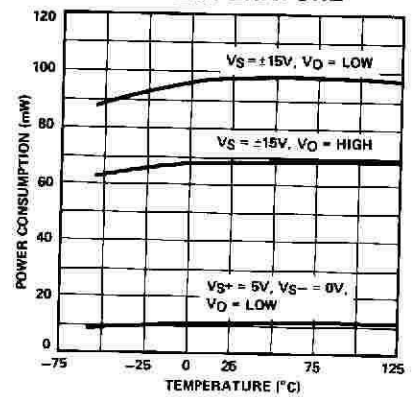
### SATURATION VOLTAGE vs SINK CURRENT



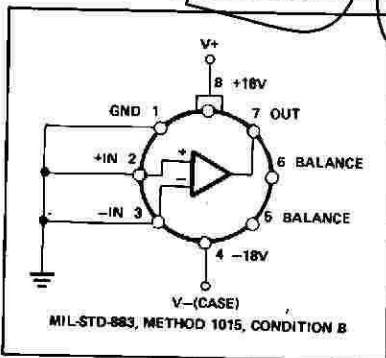
### SUPPLY CURRENT vs SUPPLY VOLTAGE



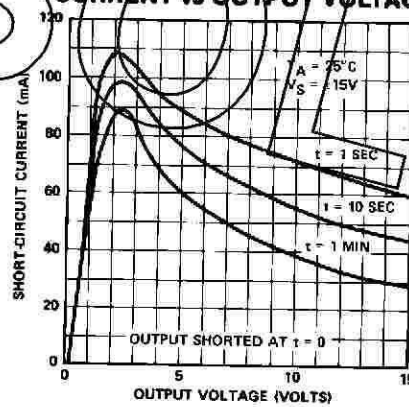
### POWER CONSUMPTION vs TEMPERATURE



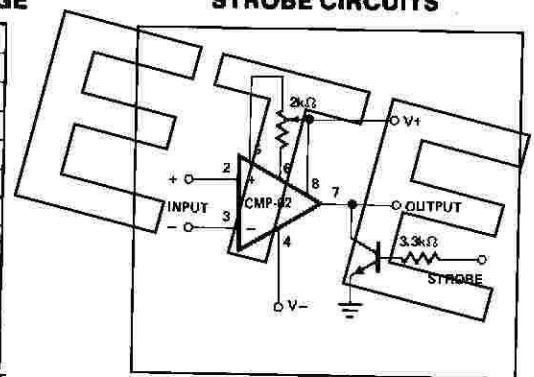
### STANDARD BURN-IN CIRCUIT



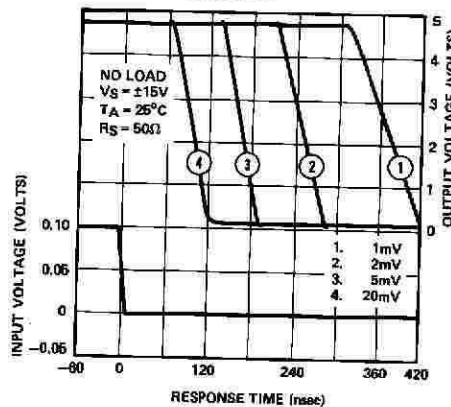
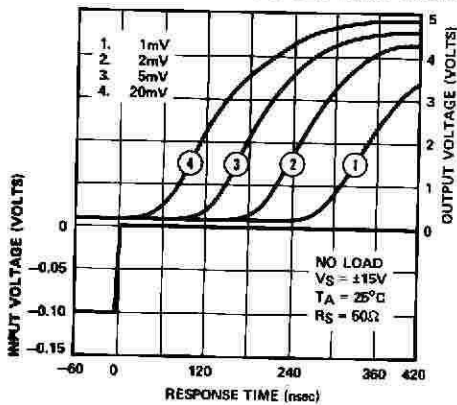
### OUTPUT SHORT-CIRCUIT CURRENT vs OUTPUT VOLTAGE



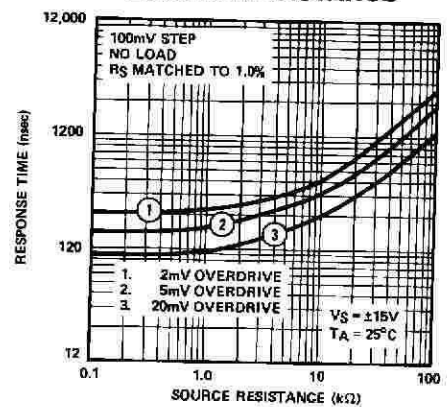
### OFFSET TRIMMING AND STROBE CIRCUITS



### RESPONSE TIME, 100mV STEP AND VARIOUS INPUT OVERDRIVES



### RESPONSE TIME vs SOURCE RESISTANCE



**APPLICATIONS INFORMATION**

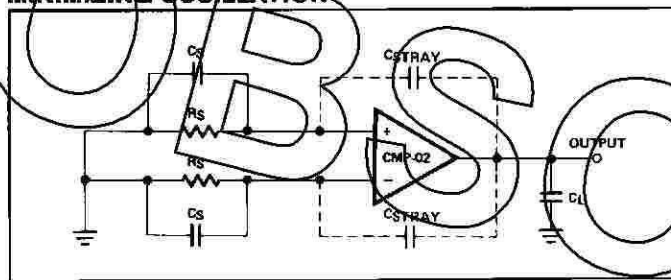
The CMP-02 provides fast response times even with small overdrives; to achieve this performance requires very high gain at high frequencies. The CMP-02 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. DC characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g., a ground plane between output and input), or capacitive output loading ( $C_L$ ). The capacitive loading techniques will eliminate the oscillations, but result in slower

response time. Matched bypass capacitors across the input resistors also can eliminate the instability,

$$\text{and if } C_S \geq 20pF \left( \frac{\text{maximum step size}}{\text{minimum overdrive}} \right)$$

the response time will approximate the response time for low values of  $R_S$ . It should be noted that the offset nulling terminals do not require bypassing for stability. As with all wideband circuits, it is recommended that the supplies be bypassed near the socket of the device.

**MINIMIZING OSCILLATION**



**PRECISION, DUAL LIMIT, GO/NO GO TESTER**

