14-Bit & 15-Bit Low Level Data Acquisition Systems

DAS1155/DAS1156

FEATURES

Functionally Complete:
Includes Instrumentation Amplifier, Sample/Hold Amplifier, and Analog to Digital Converter
Differential Nonlinearity: ±0.002% FSR max (DAS1156)
Guaranteed Nonlinearity: ±0.005% FSR (DAS1155)
±0.003% FSR (DAS1156)
High Common Mode Rejection: −80dB (up to 500Hz)
High Feedthrough Rejection: −96dB
Resistor Programmable Gain: 1V/V to 1000V/V
Byte Selectable Tri-State Buffer Outputs
Internal Gain and Offset Potentiometers

APPLICATIONS

Low Level High Accuracy Data Acquisition Systems
Process Control
Nuclear Instrumentation
Automated Test Equipment
Medical Instrumentation

GENERAL DESCRIPTION

The DAS1155/DAS1156 are 14-/15-bit low level data acquisition systems having a minimum throughput rate of 25kHz/20kHz. These data acquisition systems provide high accuracy, high stability, and functional completeness all in a 2″ × 4″ × 0.44″ metal case.

Guaranteed high accuracy system performance such as nonlinearity of ±0.005% FSR (DAS1155)/±0.003% FSR (DAS1156) and differential nonlinearity of ±0.003% FSR (DAS1155)/±0.002% FSR (DAS1156) are provided. Guaranteed stability such as differential nonlinearity T.C. of ±2ppm/°C maximum, offset T.C. of ±(1 + 50/G) μV/°C (RTI) and gain T.C. (RTI) of ±16ppm/°C are also provided by the DAS1155/DAS1156.

Each DAS1155/DAS1156 makes extensive use of both integrated circuit and thin-film components to obtain its excellent performance and small size. Incorporated in these devices are a gain programmable instrumentation amplifier, precision sample/hold amplifier, high accuracy 14-/15-bit analog to digital converter, tri-state output buffers, gain and offset trim potentiometers, and power supply bypass capacitors (as shown in Figure 1).

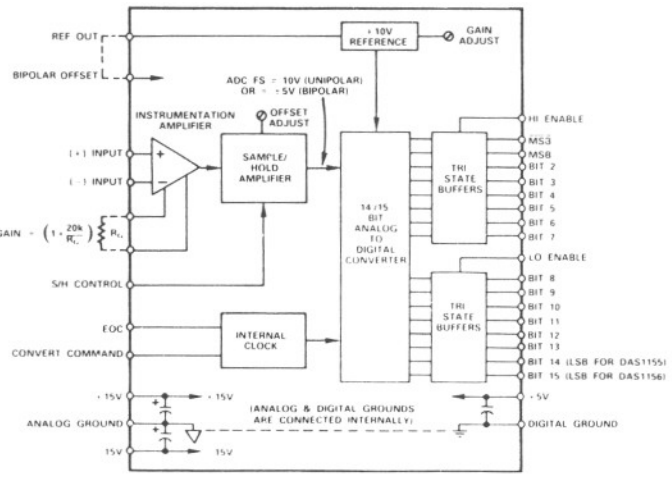

Figure 1. DAS1155/DAS1156 Block Diagram

Unipolar coding is provided for true binary format with bipolar coding displayed in offset binary or two's complement. Tri-state buffers are available for easy interface to bus structured applications.

OPERATION

The DAS1155/DAS1156 are designed, built, and tested to meet system data acquisition requirements. These units can significantly reduce design and debug time by providing, in one package, all of the circuitry necessary for low level data acquisition and microprocessor bus interface.

For operation, the only connections necessary to the DAS1155/DAS1156 are the ±15V and +5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Digital output programming is user selectable via external jumper connections.

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ANALOG INPUT SECTION

The analog input section consists of a true differential instrumentation amplifier used to obtain high accuracy measurements in the presence of noise (as shown in Figure 2). It also provides input impedance of (100MΩ) and high common mode rejection of (−80dB). User selectable gain of 1V/V to 1000V/V via an external resistor enables either low level or high level full scale ranges to be applied to the input (+10mV to +10V unipolar, ±5mV to ±5V bipolar) with gain determined by the following formula:

$$\text{GAIN} = 1 + \left(\frac{20k}{R_G}\right)$$

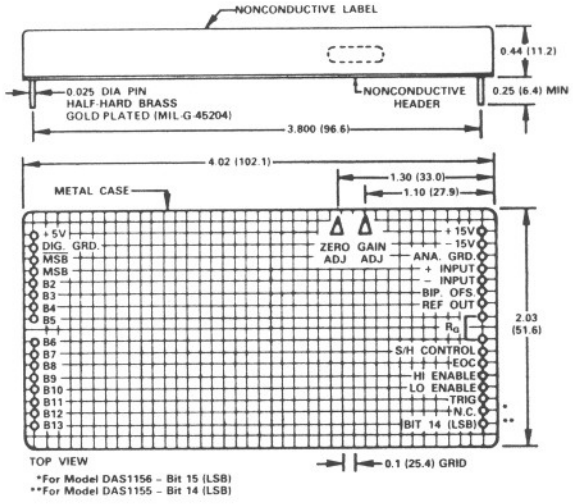
SPECIFICATIONS (typical @ +25°C and rated supplies unless otherwise noted)

MODEL	DAS1155	DAS1156
RESOLUTION	14 Bits	15 Bits
DYNAMIC CHARACTERISTICS		
ADC Conversion Time	35µs max	44µs max
IA Settling Time, (10V Output Swing)		
to 0.003% FSR @ G = 1	15µs max	*
to 0.003% FSR @ G = 10	15µs max	*
to 0.01% FSR @ G = 1000	50µs	*
Throughput Rate @ G = 1, 10	25kHz min	20kHz min
SAMPLE HOLD		
Acquisition Time	4µs max	5µs max
Aperature Delay Time	50ns	*
Aperture Uncertainty Time	1ns	*
Feedthrough Rejection [1]	−96dB	*
Droop Rate	0.05µV/µs	*
ACCURACY		
Differential Nonlinearity (FSR)[2]	±0.003% max	±0.002% max
Integral Nonlinearity (FSR)[3]	±0.005% max	±0.003% max
No Missing Codes	Guaranteed	*
Offset Error	Adjustable to Zero	*
Gain Error	Adjustable to Zero	*
STABILITY		
Offset (RTI) T.C.	$\pm\left(1+\frac{50}{G}\right)$ µV/°C	*
Gain (RTI) T.C.	±16ppm/°C	*
Differential Nonlinearity T.C.	±2ppm/°C max	*
Power Supply Sensitivity	±0.0015% FSR/% V_S	*
ANALOG INPUTS		
Voltage Input Range $\left(\frac{\text{ADC FSR}}{\text{Gain}}\right)$	+10mV to +10V (Unipolar)	*
	±5mV to ±5V (Bipolar)	*
Instrumentation Amplifier		
Gain	Resistor Programmable	*
Gain Range	1 to 1000	*
Gain Equation	$G=1+\left(\frac{20k\Omega}{R_G}\right)$	*
Input Impedance	$10^8\Omega$	*
Bias Current	50nA	*
Offset Current	2nA	*
CMR (up to 500Hz)	−80dB	*
CMV	±10V	*
DIGITAL INPUTS		
ADC Convert Command[4]	1TTL Load, Positive Pulse Negative Edge Triggered	
SHA Control	HOLD = Logic 0 SAMPLE = Logic 1	
Low Enable, High Enable	ENABLE = Logic 0	
DIGITAL OUTPUTS		
Parallel Data Outputs	Tri-State	
Unipolar	Binary	
Bipolar	Offset Binary, 2's Complement	
Output Drive	2TTL Loads	
Status	Logic "1" During Conversion	
Output Drive	2TTL Loads	
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%	
External Load Current (Rated Performance)	2mA (max)	
Temperature Stability	±8.5ppm/°C (max)	
POWER REQUIREMENTS		
Rated Voltages	±15V ±5%, +5V ±5%	
Operating Voltages[5]	±12V to ±17V, +4.75V to +5.25V	
Supply Current Drain ±15V	±40mA	
+5V	80mA	
TEMPERATURE RANGE		
Specified	0 to +70°C	
Operating	−25°C to +85°C	
Storage	−25°C to +85°C	
Relative Humidity	(Meets MIL-STD-202E, Method 103B)	
SHIELDING	Electrostatic (RFI) 6 sides, Electromagnet (EMI) 5 sides	
SIZE	2" × 4" × 0.44" metal package	

NOTES
[1]Measured in hold mode, input 20V pk-pk @ 10kHz.
[2]FSR means Full Scale Range.
[3]Worst-case summation of IA, S/H and A/D nonlinearity errors.
[4]When connecting the Convert Command the S/H control terminals together, the pulse width must be long enough for the S/H amplifier to acquire the input signal to the required accuracy 4µs (min, DAS1155) 5µs (min, DAS1156).
[5]If a ±12V operating power supply is used, the analog input must be limited to ±7V.
[6]Recommended Power Supply: Analog Devices Model 923.
*Same specifications as for DAS1155.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



*For Model DAS1156 – Bit 15 (LSB)
**For Model DAS1155 – Bit 14 (LSB)

INTERCONNECTION AND SHIELDING TECHNIQUES

To preserve the high CMR characteristics of the DAS1155/DAS1156, care must be taken to minimize noise wherever possible. For best performance use twisted shielded cable, for the sensitive input signal, to reduce inductive and capacitive pickup. The cable should be connected as close as possible to the input common mode signal source. Place the gain setting resistor as close as possible to its respective terminal connections to avoid pickup.

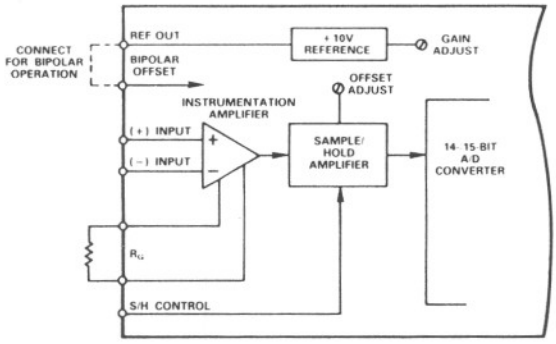


Figure 2. Analog Input Block Diagram

The gain T.C., of the DAS1155/DAS1156, will be directly affected by the resistor used for R_G. Using a high quality metal film resistor is recommended. Bipolar operation is obtained by connecting the REF OUT and the BIPOLAR OFFSET terminals together.

The output of the instrumentation amplifier drives the sample/hold amplifier which has a gain of 1V/V. The sample/hold amplifier holds the input signal at a constant level during the A/D conversion. Acquisition times of 4μs and 5μs maximum are provided respectively by the DAS1155 and DAS1156. Full scale A/D converter input range is programmed for ± 10V (unipolar) or ± 5V (bipolar). Therefore, the instrumentation amplifier gain must be set accordingly to obtain maximum usable resolution.

COMMON MODE REJECTION

CMR is dependent on source impedance imbalance, signal frequency, and amplifier gain. CMR is specified having a ±10V CMV and 1kΩ source imbalance over a frequency range of dc to 500Hz. Figure 3 illustrates the typical CMR vs. source impedance imbalance for the DAS1155/DAS1156. Increasing the input gain of the instrumentation amplifier increases the CMR. At Gain = 1V/V, CMR is maintained greater than 80dB for source impedance imbalance up to 10kΩ. Figure 4 illustrates the CMR vs. gain and frequency.

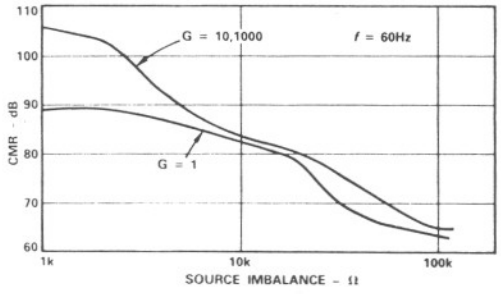


Figure 3. CMR vs Gain and Source Imbalance DAS1155/DAS1156

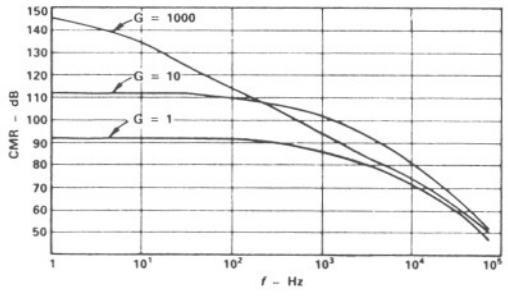


Figure 4. CMR vs Frequency DAS1155/DAS1156

SETTLING TIME VS. GAIN

Illustrated in Figure 5 is the typical settling time vs. gain of the instrumentation amplifier in the DAS1155/DAS1156. Settling times are specified to 0.003% FSR for gains 1 and 10, and to 0.01% FSR for gain to 1000 having an output step voltage of 10 volts. Settling time to 0.003% FSR for gains greater than 10 are not shown because of the effects of voltage noise at the higher gains.

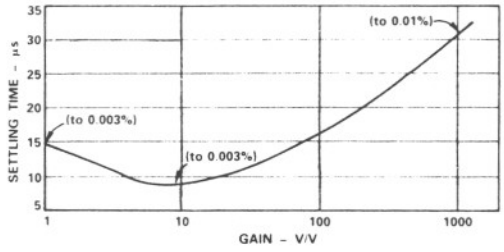
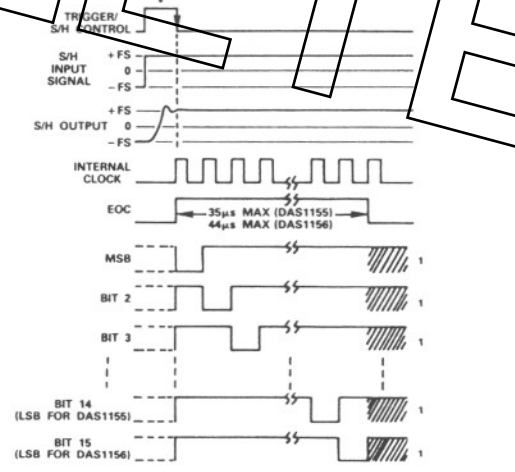


Figure 5. Typical Settling Time vs Gain

TIMING DIAGRAM

The timing diagram for the DAS1155/DAS1156 is illustrated in Figure 6. This figure includes the sample/hold amplifier characteristics and assumes that the instrumentation amplifier is allowed to settle during the previous conversion.



NOTES

1. Output Data Valid.
2. This Diagram assumes that the Instrumentation Amplifier is allowed sufficient time to settle before the Sample/Hold Amplifier is placed in the Sample Mode. Instrumentation Amplifier settling can take place during the A/D Conversion process for the next conversion (see throughput rate).
3. The S/H Control and Trigger are tied together, Pulse Width must be 4μs (min)/5μs (min) to allow the S/H Amplifier to acquire the Input Signal.

Figure 6. DAS1155/DAS1156 Timing Diagram

The TRIGGER input and S/H CONTROL terminal can be tied together requiring only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of 4μs/5μs, for the DAS1155/DAS1156 respectively, to insure accuracy is attained. At the falling edge of the TRIGGER pulse, the sample/hold amplifier is placed in the hold mode, the A/D conversion

begins, and all internal logic is reset. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With this negative edge of the trigger pulse the MSB is set low with the remaining digital outputs set to logic high state, and the status line is set high and remains high thru the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The internal DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-bit conversion taking 35μs/44μs maximum respectively for the DAS1155/DAS1156.

At this time, the STATUS line goes low signifying that the conversion is complete. For bus applications, the digital output can now be applied to the selected data bus by enabling the tri-state buffers with the HI-ENABLE and LO-ENABLE terminals.

GAIN AND OFFSET ADJUSTMENTS

The DAS1155/DAS1156 each are provided with internal gain and offset adjustment potentiometers. Each potentiometer has ample adjustment range so that gain and offset errors can be trimmed to zero.

Since offset calibration is not affected by changes in gain calibration, it should be performed first. Proper gain and offset calibration require great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable and be capable of being set to within ±1/10LSB of the desired value at any point within its range.

The analog input values given in Tables I, II, III and in the following Offset & Gain Calibration Section, are values that should be present at the input to the internal ADC. The value of the analog input will be affected by the gain of the input instrumentation amplifier.(Example: For a full scale input of 0 to +5V, divide the 0 to +10V range input values by 2 and set input gain to 2.)

Analog Input 0 to +10V Range		Digital Output Binary Code	
DAS1155	DAS1156	DAS1155	DAS1156
+9.99939V	+9.99969V	11 111 111 111 111	111 111 111 111 111
+5.00000V	+5.00000V	10 000 000 000 000	100 000 000 000 000
+1.25000V	+1.25000V	00 100 000 000 000	001 000 000 000 000
+0.0006V	+0.0003V	00 000 000 000 001	000 000 000 000 001
+0.0000V	+0.0000V	00 000 000 000 000	000 000 000 000 000

Table I. Nominal Unipolar/Output Relationships

Analog Input ±5V Range	Digital Output Offset Binary Code	Two's Complement Code
+4.99939V	11 111 111 111 111	01 111 111 111 111
+2.50000V	11 000 000 000 000	01 000 000 000 000
+0.00061V	10 000 000 000 001	00 000 000 000 001
+0.00000V	10 000 000 000 000	00 000 000 000 000
−5.00000V	00 000 000 000 000	10 000 000 000 000

Table II. DAS1155 Bipolar Input/Output Relationships

Analog Input ±5V Range	Digital Output Offset Binary Code	Two's Complement Code
+4.99969V	111 111 111 111 111	011 111 111 111 111
+2.50000V	110 000 000 000 000	010 000 000 000 000
+0.00030V	100 000 000 000 001	000 000 000 000 001
+0.00000V	100 000 000 000 000	000 000 000 000 000
−5.00000V	000 000 000 000 000	100 000 000 000 000

Table III. DAS1156 Bipolar Input/Output Relationships

OFFSET CALIBRATION

For 0 to +10V unipolar range set the input voltage precisely to +305μV for the DAS1155 and +153μV for the DAS1156. Then adjust the zero potentiometer until the converter is just on the verge of switching from 00-----00 to 00-----01.

For the ±5V bipolar range set the input voltage precisely to +305μV for the DAS1155 and +153μV for the DAS1156. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 00-----00 to 00-----01 and the two's complement coded units are just on the verge of switching from 10-----00 to 10-----01.

GAIN CALIBRATION

Set the input voltage precisely to +9.99909 (DAS1155)/+9.99954V (DAS1156) for the 0 to +10V units, or +4.99909V (DAS1155)/+4.99954V (DAS1156) for ±5V units. Note that these values are 1 1/2LSB less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11-----10 to 11-----11 and two's complement coded units are just on the verge of switching from 011-----10 to 011-----11.

THROUGHPUT RATE

Throughput rates for the DAS1155/DAS1156 can be increased by the use of the OVERLAP MODE, i.e. updating the input while the ADC is making a conversion.

The guaranteed throughput rates are 25kHz @ G = 1, 20kHz @ G = 1000 for the DAS1155 and 20kHz @ G = 1 and 1000 for the DAS1156. When the IA settling time is less than or equal to the sum of SHA acquisition time and ADC conversion time, 39μs, the DAS throughput rate equals 1/39μs or 25.6kHz. When IA settling time is greater than 39μs (see Figure 5), the DAS throughput rate becomes dependent upon the IA settling time and equals its reciprocal.

DAS1155/DAS1156 INPUT/OUTPUT RELATIONSHIPS

The DAS1155/DAS1156 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is used to obtain the binary and offset binary code while the ($\overline{MSB}$) is used to obtain the two's complement code. Table I shows the unipolar analog input/digital output DAS1155/DAS1156 relationships. Tables II and III show the DAS1155/DAS1156 bipolar analog input/digital output relationships respectively.

TRI-STATE DIGITAL OUTPUT

The digital outputs are provided in parallel format to the output tri-state buffers. The output information can be applied to a data buss in either a one-byte or a two-byte format by using the HI-ENABLE and LO-ENABLE terminals. If the tri-state feature is not required, normal digital outputs can be obtained by connecting the enable pins to ground.

POWER SUPPLY AND GROUNDING CONNECTIONS

Although the analog power ground and the digital ground are connected in the DAS1155/DAS1156, care must still be taken to provide proper grounding due to the high accuracy nature of the devices. Though only general guidelines can be given, grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. Analog and digital grounds should remain separated on the PC board and terminated at the respective DAS1155/DAS1156 terminals.

No power supply decoupling is required since, both the DAS1155 and DAS1156, contain high quality tantalum capacitors on each of the power supply inputs to ground.