This document outlines the basic procedure for designing a loop filter for legacy HMC products such as the HMC439QS16G, HMC3716LP4E, HMC440QS16GE, HMC698LP4E and HMC699LP4E that do not utilize a charge pump. Because a charge pump isn't used, voltage pulses, as opposed to current pulses are output. There is a work around for this using the HMC PLL Design tool. If not found on the product splash page on the website please use the link provided below.

http://www.hittite.com/products/view.html/view/HMC703LP4E



Under the "Product Support" heading click on "Software Download" and fill out the form. A link will be sent that allows you to download and install the software.

Once installed Launch the application using the executable shown below.

Hittite Microwave Corp Hittite PLL Design Launch HITT- PLL Design.exe Hittite PLL VCO Eval Software

	Hittite Microwave PL	L Design & Analysis Tool	Filter Design	Fix RC Values
MICHOWAVE CORPORATION	Version 1.1			
VCO Frequency	S-Domain Respo	onse Settings		
Fixed In-Loop Divider	Start Frequency	10	C1	R1
PFD Frequency	Stop Frequency	1e7	R2	C2
TCX0 Frequency	Number of Points	100	R3	C3
VCO Gain [Hz/V]	Transient Resp	onse Settings		
Phase Detector Gain		Frequency Step 💌	R4	
Phase Detector Gain	Initial Frequency	Initial Time	L7	RL
Phase belector on set	Frequency Step	Final Time	2dD Dandwidth	
Desired Bandwidth	Noise Contributions	Show Integration Limits? V	Actual Phase Mar	gin
Desired Phase Margin	Noise Integration From	To		
				Loop Parameters
1		Time Domain Se	ettling <	Integrated Noise >
0.9		±Hz	±Degrees	
0.8				
		Select Plot 1	уре	
		Open Loop Respo	nse T	
0.6				
0.5				
	+++++++++++++	Frequency Domain	Plot Settings	
0.4		inclusion bonnan		
0.3		fmin fr	nax	
		Ymin Y	max	
	++++++++			
0.2				

Under File, select "Load Hittite PLL Model File", then select "PLLs with Integrated Microwave VCOs", "HMC778LP6CE" and finally "hmc778 Eval Board as Built.pll". Click "Open". Note the "Filter Design" radio button in the upper right side – this will be used later to select the proper loop filter type while the "Noise Contributions" radio button will allow us to enter the phase noise for various components in our synthesizer.

MICHOWAVE CORPORATION		Hittite Microwave PLL D Version 1.1	esign & Analysis Tool	Filter Desi	jn	🔽 Fix RC Values
VCO Frequency	10 GHz	S-Domain Respons	e Settings	Filter Type: a Filter Order:	ictiveC 4	
Fixed In-Loop Divider	4	Start Frequency	100 Hz	C1 560 p	F	
PFD Frequency	50 MHz	Stop Frequency	100 MHz	R2 390 0	hms C2	18 nF
TCX0 Frequency	50 MHz	Number of Points	100	R3 390 0	hms C3	270 pF
VCO Gain [Hz/V]	160 M	Transient Respons	e Settings	R4 13 0	nms C4	3.9 nF
Phase Detector Gain	2.5 m	Transient Mode	Frequency Step			
Phase Detector Offset	0	Initial Frequency 1.7000(Initial Time 0 s			
PLL Division Ratio N	50.000	Frequency Step 100 MH	Final Time 280 us	3dB Bandwid	ith	120.6 kHz
Desired Bandwidth	60 kHz	Noise Contributions Sho	w Integration Limits? 🔽	Actual Phase	Margin	63.93
Desired Phase Margin	70	Noise Integration From 10	kHz To 10 MHz			
	All Noise Cont	ributors			Loop P	arameters
-80		VCO: 10 GHz	Time Domain Se	ttling	< PLL Pa	arameters >
-90		TAL PD Filter Div DS	1 kHz ±Hz Select Plot T	10 ±Degrees ype	Operating Temp.: VCO Period: PFD Period: Reference Spur Lev Locked Phase: Phase Noise FOM-	27.0 °C 100 ps 20 ns rel: -300.00 dBo 0 s, 0.00 ° 225.8 dBo at 13.3 kHz
110		Total PLL Phase Noise Spec	All Noise Contribu	tors	In-Band Phase Nois Zero Frequency Loc -22.7 kHz Pole Frequency Loc	e Peak 0.6 dB sations: sations:
130			Frequency Respon	se Scale	-3.1 MHz -1.69 MHz -428 kHz	
140	/		fmin 100 Hz fn	nax 100 MHz	-147 kHz -29.4 kHz	
			Ymin -165.00 Yr	nax -75.00	Ref. Frequency to	PLL BW Ratio: 414.4
150			TITTO			

HMC778LP6CE PLL file. Note that this will automatically populate the main form as well as other sub-forms with information that is relevant to the HMC778LP6CE. Much of this information will need to be altered for our application.

Calculate VCO Frequency or Division F	Ratio ?	Division Ratio N
Phase Detector Range	2pi 🗾	6.28319
Phase Noise Dynamic Range to Plot	90 dB	From Maximum 📃
Plot Line Width	2	
Operating Temperature (Celcius)	27	
Phase Detector Noise Specification	Input Referred No	bise 💌
Time Domain Plot Scaling	Absolute	•
Plot Appearance	Change Line	Styles and Colors
Component Selection		
Resistors	E96 (1%)	×
Capacitors	E24 (5%)	¥
Inductors	E24 (5%)	•

Under "Tools" there are several features that are helpful. Under "Options" one can define the component series that will be used to generate the loop filter values. I typically set these as shown.

Specify List of Parts	
Specify Part Information for Report	
Part Type	Part Name
PFD	HMC439QS16G
vco	Crystek CVCO55CL-0902-0928
Opamp	ADA 4084-1
Ref	920MHz
N = 1	Active Loop
	<u>OK</u>

Under "Parts Information", details relative to the design may be entered. Here I've updated the values.

— Loon Filter Type————		
Select Filter Type		K2 C2
Pro Filer		↑ [~]
Filter Order	3	RL VOC
Calculation Method Exact Ca	lculation	
Damping Factor For Approximate Metho	od 0.7071	
- 3rd and 4th Pole Calculation		
3rd Pole By Ratio to 2nd Pole	2.00	
4th Pole By Ratio to 2nd Pole	4.00	
Optimization Parameter	1.00	
-		VCO Input 100 pF Cp 3.3 nF
	— Filter Parameters —	C3/Cvco 1000.00 R1 200 Ohms
	Zero at: 10.8 kHz	Rg 183 C2 5.1 uF
Apply Ratio C2/C3 3.00	Poles at: 0 Hz	Rf 1e3 p2 2.87 Ohms
Apply Ratio C2/C4 3.00	-125 kHz -251 kHz	Ch. I nE. co. 100 nE
		R3 jo.34 Ohms
LC Ladder Parameters		R1/RL Ratio 1 Ohms
Corner Frequency Stop	Frequency	RL 200
Passhand Attenuation	and Attonuction	
Stopp		
		·····

Clicking the "FILTER DESIGN" radio button opens the Loop Filter design synthesis form. There are several key things to understand regarding this form and its use for designing a loop filter for legacy HMC (now Analog Devices) PFD's and PFD based synthesizers.

- 1) The only TYPE of loop filter that can be derived using this tool for these PFD based products (with this application) is the "PFD Filter". The remaining types apply to charge pump based PLL's.
- 2) The (2) columns of text boxes under the schematic allow the user to customize the synthesis of the loop values based on their specific application. The column of text boxes on the left should be considered "Inputs" while the column on the right will be the synthesized values. Our decisions here will affect R1 and C3 only, the remaining components will be synthesized later.

- a. VCO Input is equivalent to the input capacitance of the Vtune port on the VCO. Here it's been changed to 100pF to match that of the VCO we plan to use.
- b. C3/Cvco is simply the ratio of the capacitance of the shunt capacitor on the 3rd pole vs the Vco input capacitance. This drives the derivation of C3 when "Apply" is clicked. Note that 1000 * 100pF = 100nF.
- c. Lastly RL should be set to "200" since this is the value of our pull-up resistors on NU / ND and the R1 / RL ratio should be set to "1 Ohms". Click "Apply" and R1 should update to "200 Ohms" as well.
- d. Finally click "OK" and exit the form.



Typical PLL Application Circuit using HMC439QS16G

PLL application shown for a 12.8 GHz Fout. Contact HMC to discuss your specific application.

The applications circuit from the HMC439QS16G is shown above. Although this application is somewhat different than the one discussed here, there are still some important similarities. Note that the 200Ω pull-up resistors on the NU / ND outputs and the 20Ω resistors on the U/D outputs. We always want to use the NU / ND outputs as they are turned off most of the time and will thus have 6dBc/hz lower phase noise than the U/D output. The resistor values shown are set for optimal phase noise performance. Deviating from this will alter the output swing and degrade phase noise. For optimal temperature performance use 1% values. Lastly, note that the HMC439QS16G and HMC440QS16G are the only parts that utilize external pull-up resistors. These resistors have been integrated into newer parts such as the HMC3716LP4E, HMC698LP5E and HMC699LP5E.

L Noise Parameters	_				
Fractional N Enable Op-Amp Noise? Crystal Oscillator/Input Noise Reference Path Noise Phase Detector Noise VCO Noise VCO Noise RF Divider Noise Operational Amplifier Noise Detta Sigma Noise Composite Noise/Output Path High Pass Noise Integration		Frequency Offset Crystal Oscillator Noise Add/Subtract from Crsyta	100 1000 10000 100000 1e+006 1e+007 1e+0 -58.6 -88.6 -115.2 -137.4 -155.2 -160.9 -160 al Phase Noise?	08	Hz dBc/Hz dB
		ок	Apply Cancel		

Next use the "Noise Contributions" radio button to display the above menu. Here I've entered the Crystal Oscillator / Input Noise values from the phase noise plot shown in the VCO datasheet after adjusting them for the difference in frequency. Note that I've also de-selected the "Fractional N" mode check box. This will improve the phase noise inside the loop bandwidth by 2-3dB typically as Integer mode will be assumed. The "Add / Subtract from Crystal Phase Noise" can be used to quickly tweak the model if measured values differ from the typical values shown on the datasheet.

PLL Noise Parameters File			
Fractional N Enable Op-Amp Noise? Crystal Oscillator.Input Noise Crystal Oscillator.Input Noise Reference Path Noise Phase Detector Noise VCO Noise VCO Noise RF Divider Noise Operational Amplifier Noise Detta Sigma Hoise Composite Noise/Output Path	Frequency Offset Reference Buffer Noise Reference Buffer Gain Reference Buffer Noise Of Reference Buffer Gain Off	10000 100000 1e+006 1e+007 1e+008 -300 -300 -300 -300 0 0 0 0 0 ffset set	Hz dBc/Hz dB 0 dB 0 dB
	ОК	Apply Cancel	

Reference Path Noise can be left alone unless details are known.

Fractional N	Use Simple Phase Detector I	Model?	M
Enable Op-Amp Noise? 🔽	Phase Detector Noise Specif	ication Frequency	100 MHz Hz
Crystal Oscillator/Input Noise	Frequency Offset	100 1000 10000 100000 1e+006 1e+007 1e+008 1e+009	Hz
Deference Bath Noise	Supply Noise	-138 -162 -170 -170 -175 -180 -180 -180	dBV^2/Hz
Kelel elice Paul Huise	PSRR	20 20 20 20 20 20 20 20	dB
Phase Detector Noise	Gain/Cycle	Input Referred Phase Detector Phase Noise	
VCO Noise	Min:		dBc/Hz
RF Divider Noise	Mid:	-136 -146 -153 -156 -156 -156 -156 -156	dBc/Hz
Operational Amplifier Noise	Max		dBc/Hz
Detta Sigma Noise	Phase Detectot Noise Offset	for Frac-N Mode	3 dB
Composite Noise/Output Path	Add Subtract from Phase De	tector Noise	0 dB
High Pass Noise Integration			

Phase Detector noise scales at 10*Log(F) so the noise as shown on the HMC439 datasheet can be entered and the "Phase Detector Noise Specification Frequency" can be set to 100MHz and it will be scaled as the PFD frequency is altered on the main form.



Here is the phase noise plot from the oscillator that we plan to use. Enter this information into the

Fractional N 🗌	Use Simple VCO Model?		
Enable Op-Amp Noise? 🔽	VCO Noise Specification Fre	quency	907.444348 MHz HZ
Crystal Oscillator/Input Noise	Tuning Voltage		Volts
Deference Dath Noise	VCO Frequnecy		kHz 💌
Kererence Faur Horac	VCO Gain (Kvco)		MHz/V 🔻
Phase Detector Noise	Frequency Offset	100 1000 10000 100000 1e+006 1e+007 1e+008 1e+009	Hz
VCO Noise	VCO Supply Noise	-138 -162 -170 -170 -175 -180 -180 -180	dBV^2/Hz
RF Divider Noise	Frequency	Open Loop VCO Phase Noise	
Operational Amplifier Noise	Min.		dBc/Hz
Delta Sigma Noise	Mid.	-58.74 -88.74 -115.2 -137.38 -155.15 -160.88 -161 -161	dBc/Hz
	Max.		dBc/Hz
Composite Noise/Output Path	Offset [dB]		0 dB
High Pass Noise Integration	Pushing Figure		1.7 MHz Hz/Volt
	or	Canaal	
		Cancer	

The simplest method for accounting for the VCO contribution is to check the "Use Simple VCO Model?" box and enter the phase noise offset frequencies and the corresponding "Open Loop VCO Noise" shown on the VCO datasheet. Note that a slope of 30dB / decade was used to derive the 100hz value to account for the 1/f noise slope. If you have measured data that is slightly different you may enter an offset. Lastly, enter the Pushing Figure from the datasheet and click "Apply".

If an RF divider will be used between the VCO output and the input to the PFD the offsets and residual or additive noise may be entered using the RF Divider Noise radio button.

All devices discussed in this document require an active loop filter which means an op amp will be needed as part of the loop filter. Most of the microwave VCO's offered by Analog Devices require a tuning voltage range of 2 – 13V anyway. The offsets and residual noise from the Analog Devices ADA4084-1op-amp that will be used can be entered for the op amp based on the information shown in the op amp datasheet in the same manner as illustrated above.



Be sure to base the values on the information shown for the desired op amp bias conditions. You may need to convert the values from nV \vee hz to dB V² \vee hz or dB A² \vee hz. Use Zo = 50 Ω .

Fractional N	Frequency Offset	100 1000 10000 100000 1e+006 1e+00	07 1e+008	Hz
Enable Op-Amp Noise? 🔽	Phase Noise Mask	-180 -180 -180 -180 -180 -180 -180		dBc/H
Crystal Oscillator/Input Noise	Add/Subtract from Comp	osite Noise?		0 dB
Reference Path Noise	Refine Numer of Points?			
Phase Detector Noise	— Output Path [Post VCO]			
	Enable		Frequency Divider	~
VCO Noise	Division Ratio			1.00
RF Divider Noise	Phase Noise Floor FOM	-300.00 dBc/Hz	Spec Frequency	1 GHz
Operational Amplifier Noise	Flicker Noise FOM			-320.00 dBc/Hz
Detta Sigma Noise				
Composite Noise/Output Path	Divider Output Power		Γ	dBm
High Pass Noise Integration	Output Frequency			920 MHz
			1	

Other Noise contributors in the output path may be added as well using the Composite Noise / Output Path radio button. To compare the synthesized results to a desired specification, enter the values for the respective offsets in the Phase Noise Mask window.

Finally, the integrated noise can be viewed after passing it through an ideal high pass filter. The filter parameters are specified using the High Pass Noise Integration radio button. Typically this is left as is. Click "Apply" and close the Noise Contribution window.

	(Hittite Microwave I Version 1.1	PLL Design & Analy	/sis Tool	er Design Tyne: PED Filter	Fix RC Values
VCO Frequency	920 MHz	S-Domain Rea	sponse Settings	Filter	Order: 3	
Fixed In-Loop Divider	1	Start Frequency	100	Hz Cp	100 nF F	a 200 Ohms
PFD Frequency	920 MHz	Stop Frequency	100	MHz R2	97.6 mOhms	2 4.3 mF
TCXO Frequency	920 MHz	Number of Points	100	R3	200 Ohms	:3 100 nF
VCO Gain [Hz/V]	13 M	Transient Re	sponse Settings		c	:4
Phase Detector Gain	2	Transient Mode	Frequency Ste	»p L7	R	L 200 Ohms
Phase Detector Offset	0	Initial Frequency 920 1	MH Initial Time	0 s		Jees sumo
PLL Division Ratio N	1.000	Frequency Step 100 1	MH Final Time	280 us 3dB B	andwidth	1.003 kHz
Desired Bandwidth	1 kHz	Noise Contributions	Show Integration L	imits? 🔽 🛛 Actua	l Phase Margin	48.04
Desired Phase Margin	48	Noise Integration Fro	m 10 kHz To	10 MHz		
	All Noise Cont	ributors			Loo	p Parameters
		VCO: 9	20 MHz	ne Domain Settling	< PLI	. Parameters >
-60		TTAL	1 kH:	z ±Hz 10 ±Degr	ees Operating Temp VCO Period:	.: 27.0 °C 1.087 ns
-70	+++++++++++++++++++++++++++++++++++++++	Filter			Reference Spur	Level: -300.00 dBc
-80		Total P		Select Plot Type	Locked Phase: Phase Noise FC	0 s, 0.00° 0M - 173.0 dBc at 1 kHz Naisa Parah, 0.0 dB
-90	 		All No	vise Contributors	Zero Frequency -378 Hz	Locations:
100					Pole Frequency -748 Hz ±j451	Locations: Hz
			Frequ	iency Response Scale	-8.66 kHz	
110	X		fmin	100 Hz fmax 100 M	MHz Ref. Frequency	to PLL BW Ratio: 917624.5
120			Ymin	-143.00 Ymax -53.0	0	
1 1 1 1 1 1 N		· · · · · · · · · · · · · · · · · · ·				

MAIN WINDOW

Enter the desired synthesizer parameters into the region shown by the red box above. The Phase Detector Gain when the PFD Filter type is used will be specified in V / Rad (the output of the HMC439QS16GE is 2V pp).

FILTER DESIGN

The 'Filter Design' radio button allows selection of various loop filter types.

🕽 Loop Filter Design							
Loop Filter Type Select Filter Type Filter Order Calculation Method Exact Calculation Damping Factor For Approximate Method							
3rd and 4th Pole Calculation 3rd Pole By Ratio to 2nd Pole 4th Pole By Ratio to 2nd Pole 4th Pole							
Optimization Parameter 1.00	VCO Input 100 pF Cp 100 nF						
Filter Capacitor Ratio to C2 Filter Parameters Apply Ratio C2/C3 3.00 Apply Ratio C2/C3 3.00 Apply Ratio C2/C4 3.00 -7.94 kHz	C3/Cvco 1000.00 R1 200 Ohms Rg 1e3 C2 4.3 mF Rf 1e3 R2 97.6 mOhms Cb 1e-9 C3 100 nF Rb1 1 R3 200 Ohms						
LC Ladder Parameters Corner Frequency Stop Frequency Passband Attenuation Stopband Attenuation	LC Ladder Parameters R1/RL Ratio Corner Frequency Stop Frequency Passband Attenuation Stopband Attenuation						
ОК Арріу	Cancel						

We will need to use the PFD Filter type as shown above.

Next, enter the VCO Input capacitance from the VCO datasheet. C3 will be derived based on this value and the ratio shown for C3 / Cvco (1000 is typical).

R1 / RL Ratio should be left at 1 as R1 will be derived based on the value we list for RL. RL is equivalent to the 200 Ω pullup resistor shown on the applications circuits for the HMC439QS16GE. On newer parts these 200 Ω resistors were moved inside the device so although you will still need to specify the value here, you will not populate 'RL' on your layout, you

will still need to populate R1. Another pitfall that is often made is altering the value of RL. This sets the voltage swing and provides the optimum noise performance so the value should remain at 200Ω . R1 should match this value.

The remaining values will be automatically calculated from the 'Main' form. Click 'Apply' and close the 'Loop Filter Design' window.

		Hittite Microwave PLL Version 1.1	Design & Analysis Tool	Filter Design	Fix RC Values	
VCO Frequency	920 MHz	S-Domain Respon	se Settings	Filter Order: 3		
Fixed In-Loop Divider	1	Start Frequency	100 Hz	Cp 100 nF	R1 200 Ohms	
PFD Frequency	920 MHz	Stop Frequency	100 MHz	R2 97.6 mC	ihms C2 4.3 mF	
TCXO Frequency	920 MHz	Number of Points	100	R3 200 Ohr	ns C3 100 nF	
VCO Gain [Hz/V]	13 M	Transient Respon	se Settings		C4	
Phase Detector Gain	2	Transient Mode	Frequency Step	L7	RL 200 Ohms	
Phase Detector Offset	0	Initial Frequency 920 MH	Initial Time 0 s		1200 011110	
PLL Division Ratio N	1.000	Frequency Step 100 MH	Final Time 280 us	3dB Bandwidth	1.003 kHz	
Desired Bandwidth	1 kHz	Noise Contributions Sh	ow Integration Limits? 🔽	Actual Phase Ma	argin 48.04	
Desired Phase Margin	48	Noise Integration From 1	0 kHz To 10 MHz			
	All Noise Cont	ributors			Loop Parameters	
			Time Domain Se	ettling 🔽	PLL Parameters >	
-60		VCO: 920 MHz	1 kHz ±Hz	10 ±Degrees Ope	enanting Termp.: 27.0 °C O Period: 1.087 ns Period: 1.09 ns	
-70	+++++++++++++++++++++++++++++++++++++++	PD Fitter	11111	Ret	erence Spur Level: -300.00 dBc	
-80		Div	Select Plot T	fype Loc Pha	Locked Phase: 0 s, 0.00* Phase Noise FOM-173.0 dBc at 1 kHz	
-90		Total PLL Phase Noise Spec	All Noise Contribut	tors T Zer -3	and Phase Noise Peak 0.0 dB o Frequency Locations: 78 Hz	
				Pol-7	e Frequency Locations: 48 Hz ±j451 Hz 25 LUS	
			Frequency Respon	se Scale -8	.76 kHz .66 kHz	
110	X		fmin 100 Hz fn	nax 100 MHz Ret	. Frequency to PLL BW Ratio: 917624.5	
120			Ymin -143.00 Yr	max -53.00		
130			Set Scale	Export Plot		

Clicking 'Compute' yields the result shown above. Note that C2 is an unrealistically large value due to our narrow loop bandwidth.

		Hittite Microwave PLL [Version 1.1	Design & Analysis Tool	Filter Des	sign PED Filter	Fix RC Values
VCO Frequency	920 MHz	S-Domain Respons	Filter Orde	: 3		
Fixed In-Loop Divider	1	Start Frequency	100 Hz	Ср 10	nF R1	200 Ohms
PFD Frequency	920 MHz	Stop Frequency	100 MHz	R2 976	mOhms C2	43 uF
TCXO Frequency	920 MHz	Number of Points	100	R3 20 0	Ohms C3	100 nF
VCO Gain [Hz/V]	13 M	Transient Respon	se Settings		C4	
Phase Detector Gain	2	Transient Mode	Frequency Step	L7	RL	200 Ohms
Phase Detector Offset	0	Initial Frequency 920 MH	Initial Time 0 s			
PLL Division Ratio N	1.000	Frequency Step 100 MH	Final Time 280 us	3dB Bandw	idth	10 kHz
Desired Bandwidth	10 kHz	Noise Contributions She	ow Integration Limits? 🔽	Actual Phas	e Margin	48
Desired Phase Margin	48	Noise Integration From 1	0 kHz To 10 MHz			
	All Noise Cont	ributors]		Loop	Parameters
-60			Time Domain Se	ttling	< PLL F	arameters >
		VCO: 920 MHz	1 kHz ±Hz	10 ±Degrees	Operating Temp.: VCO Period: PED Period:	27.0 °C 1.087 ns 1.09 ns
-80	• • • • • • • • • • • • • • • • • • •	PD Filter			Reference Spur Le	vel: -300.00 dBc
		Div	Select Plot T	уре	Locked Phase: Phase Noise FOM In-Band Phase Noi	0 s, 0.00* -199.1 dBc at 10 kHz se Peak 0.0 dB
100		Phase Noise Spec	All Noise Contribut	ors 🗾	Zero Frequency Lo -3.78 kHz	cations:
130					Pole Frequency Lo -7.48 kHz ±j4.51 l	cantions: (Hz
			Frequency Respon	se Scale	-86.6 kHz	
140			fmin 100 Hz fn	nax 100 MHz	Ref. Frequency to	PLL BW Ratio: 92000.0
			Ymin -180.00 Yr	nax -53.00		
		N		Frank Black		

Increasing the Loop bandwidth yields a more realistic value. After computing use the 'Set Scale' buttons to re-scale if desired. To tweak the performance, check the 'Fix RC Values' box. This will calculate the loop response based on the component values instead of the 'Desired Bandwidth' and 'Desired Phase Margin' text boxes.

Note that depending on the design, when N = 1 you may see up to a 3dB degradation over the synthesized performance.