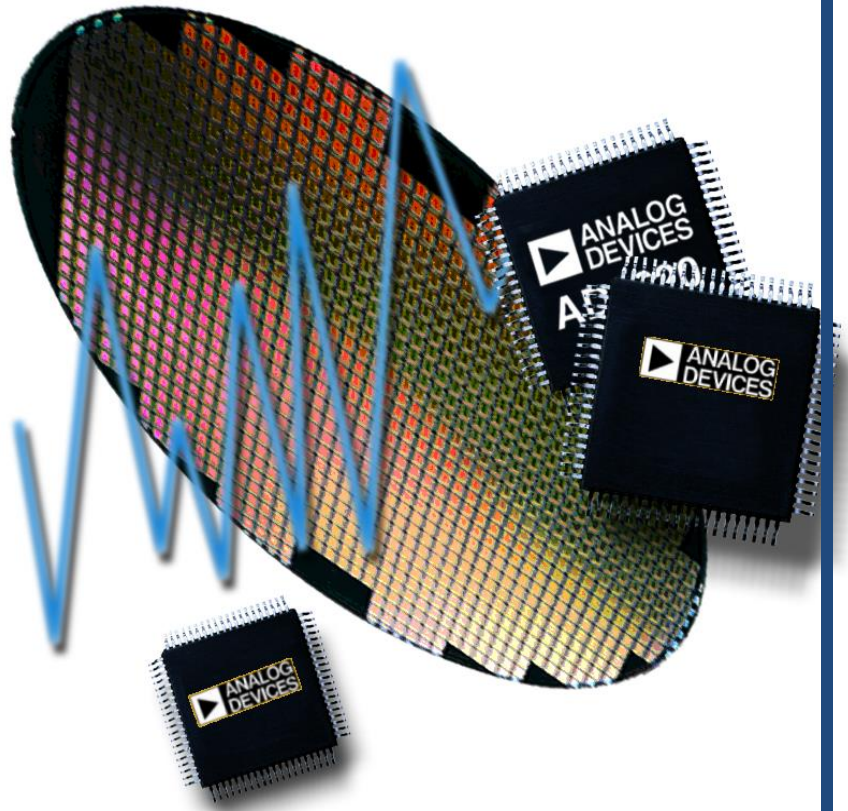


Analog Devices Welcomes Hittite Microwave Corporation

NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED





Reliability Report

Report Title:	Qualification Test Report
Report Type:	See Attached
Date:	See Attached

Process FIT Rate Report

QTR: 2013- 00269

Rev: 06

Wafer Process: PHEMT-F

ADMV1009	HMC578	HMC996
ADMV1011	HMC579	HMC997
HMC368	HMC594	HMC1082
HMC383	HMC598	HMC6187
HMC441	HMC608	
HMC442	HMC609	
HMC448	HMC633	
HMC449	HMC634	
HMC451	HMC635	
HMC459	HMC636	
HMC460	HMC639	
HMC462	HMC659	
HMC463	HMC693	
HMC464	HMC694	
HMC465	HMC709	
HMC490	HMC751	
HMC498	HMC752	
HMC499	HMC814	
HMC559	HMC815	
HMC561	HMC819	
HMC562	HMC870	
HMC573	HMC871	
HMC575	HMC924	
HMC576	HMC925	
HMC577	HMC942	

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- *Advance in state-of-the-art technology that supports our products*
- *Enhance our competitive position with superior product standards*

Hittite's employees recognize the responsibility to:

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- *Continue to improve quality practices*

Introduction

This report is intended to summarize all of the process related stress test data for the PHEMT-F process. The FIT/MTTF calculations contained in this report were calculated using the High Temperature Operating Life Test (HTOL) stress tests performed on this process to date and will be updated periodically as additional data becomes available. Data sheets for the tested devices can be found at www.analog.com.

Glossary of Terms & Definitions:

1. **HAST:** Highly Accelerated Stress Test (biased). Devices are subjected to 96 hours of 85% relative humidity at a temperature of 130°C and pressure (18.6 PSIG), while DC biased. This test is performed in accordance with JESD22-A110.
2. **HTOL:** High Temperature Operating Life. This test is used to determine the effects of bias conditions and temperature on semiconductor devices over time. It simulates the devices' operating condition in an accelerated way, through high temperature and/or bias voltage, and is primarily for device qualification and reliability monitoring. This test was performed in accordance with JEDEC JESD22-A108.
3. **HTSL:** High Temperature Storage Life. Devices are subjected to 1000 hours at 150°C per JESD22-A103.
4. **MSL:** Moisture sensitivity level pre-conditioning is performed per JESD22-A113.
5. **Operating Junction Temp (T_{j-use}):** Temperature of the die active circuitry during typical operation.
6. **Stress Junction Temp ($T_{j-stress}$):** Temperature of the die active circuitry during stress testing.
7. **Temperature Cycle:** Cond C (-65°C to 150°C), 500 cycles per JESD22-A104.
8. **UHASt:** Unbiased Highly Accelerated Stress Test. Devices are subjected to 96 hours of 85% relative humidity at a temperature of 130°C and pressure (18.6 PSIG). This test is performed in accordance with JESD22-A118.
9. **THB:** Temperature Humidity Bias. Devices are subjected to 1000 hours of 85% relative humidity at a temperature of 85°C while DC biased. This test is performed in accordance with JESD22-A101.

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Qualification Sample Selection:

All qualification devices used were manufactured and tested on standard production processes and met pre-stress acceptance test requirements.

Summary of Qualification Tests:

Table1: GaAs pHEMT Fab Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature operating Life (HTOL)	JESD22-A108	T _{J-stress} =150°C, biased, 1000 hours	HMC6445	QTR2012-00021	78	0
		T _{J-stress} =175°C, biased, 1000 hours	HMC996	QTR2012-00027	78	0
		T _{J-stress} =200°C, biased, 1000 hours	HMC996	QTR2012-00027	25	0
		T _{J-stress} =225°C, biased, 1000 hours	HMC996	QTR2012-00027	25	0
		T _{J-stress} =205°C, biased, 1000 hours	HMC996	QTR2012-00027	24	0
		T _{J-stress} =215°C, biased, 1000 hours	HMC996	QTR2012-00027	24	0
		T _{J-stress} =210°C, biased, 1000 hours	HMC996	QTR2012-00027	24	0
		T _{J-stress} =215°C, biased, 1000 hours	HMC996	QTR2012-00027	24	0
		T _{J-stress} =175°C, biased, 1000 hours	HMC383	QTR2012-00320	80	0
		T _{J-stress} =175°C, biased, 1000 hours	HMC814	QTR2012-00321	77	0
		T _{J-stress} =175°C, biased, 1000 hours	HMC451	QTR2012-00325	80	0
		T _{J-stress} =150°C, biased, 1000 hours	HMC2168	QTR2013-00339	81	0
		T _{J-stress} =135°C, biased, 1000 hours	ADMV1009	Q12547.7	77	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	HMC6445	QTR2012-00021	80	0
			HMC996	QTR2012-00027	80	0
			HMC383	QTR2012-00320	80	0
			HMC814	QTR2012-00321	80	0
			HMC451	QTR2012-00325	80	0
			ADMV1009	Q12547.6	25	0
			ADMV1011	Q12916.12	25	0
Highly Accelerated Stress Test (HAST) ¹	JESD22-A110	130C 85%RH 33.3 psia, 96 Hours, biased	HMC6445	QTR2012-00021	78	0
			HMC996	QTR2012-00027	77	0
Unbiased HAST (UHAST) ¹	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	HMC996	QTR2012-00027	77	0
			HMC383	QTR2012-00320	79	0
			HMC814	QTR2012-00321	78	0
Unbiased HAST (UHAST) ²	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	HMC451	QTR2012-00325	80	0
			ADMV1009	Q12547.5	25	0
			ADMV1011	Q12916.13	25	0

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Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
Temperature Humidity Bias (THB) ²	JESD22-A101	85°C, 85%RH, Cycled Bias, 1,000 Hours	ADMV1009	Q12547.4	25	0

¹ These samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 168 hrs @ 85°C, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

² These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

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PHEMT-F Failure Rate Estimate

Based on HTOL test results, a failure rate estimation was determined using the following parameters:

- Die Use Junction Temperature, $T_{j-use} = 125^{\circ}\text{C}$
- PHEMT-F Activation Energy = 1.57 eV

- Acceleration Factor (AF):
$$AF = \exp\left[\left(\frac{E_A}{k}\right) \cdot \left(\left(\frac{1}{T_{USE}}\right) - \left(\frac{1}{T_{STRESS}}\right)\right)\right]$$

- Equivalent hours = Device hours x Acceleration Factor

Table 2: Equivalent Device Hours Table

Device	Qual Number	Equivalent Device Hours
HMC6445	QTR2012-00021	1.17×10^6
HMC996	QTR2012-00027	1.27×10^8
HMC383	QTR2012-00320	1.34×10^7
HMC814	QTR2012-00321	1.29×10^7
HMC451	QTR2012-00325	1.34×10^7
HMC2168	QTR2013-00339	1.22×10^6
ADMV1009	Q12547.7	2.37×10^5
Total Equivalent Device Hours =		1.69×10^8

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The failure rate was calculated using Chi Square Statistic:

Since there were no failures and the tests were time terminated, $F=0$, and $R = 2F+2 = 2$

$$\lambda_{CL} = \frac{\chi^2_{(\%CL, 2F+2)} \cdot 10^9}{2 \cdot (\text{Equiv. Device Hours})} \text{ at 60\% and 90\% Confidence Level (CL) and a die use junction temp, } T_{j\text{-use}}=125^\circ\text{C};$$

Failure Rate:

$$\lambda_{60} = [(\chi^2)_{60,2}] / (2 \times 1.69 \times 10^8) = 1.8 / 3.38 \times 10^8 = 5.41 \times 10^{-9} \text{ failures/hour or } 5.4 \text{ FIT or MTTF} = 1.85 \times 10^8 \text{ Hours}$$

$$\lambda_{90} = [(\chi^2)_{90,2}] / (2 \times 1.69 \times 10^8) = 4.6 / 3.38 \times 10^8 = 1.36 \times 10^{-8} \text{ failures/hour or } 13.6 \text{ FIT or MTTF} = 7.33 \times 10^7 \text{ Hours}$$

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