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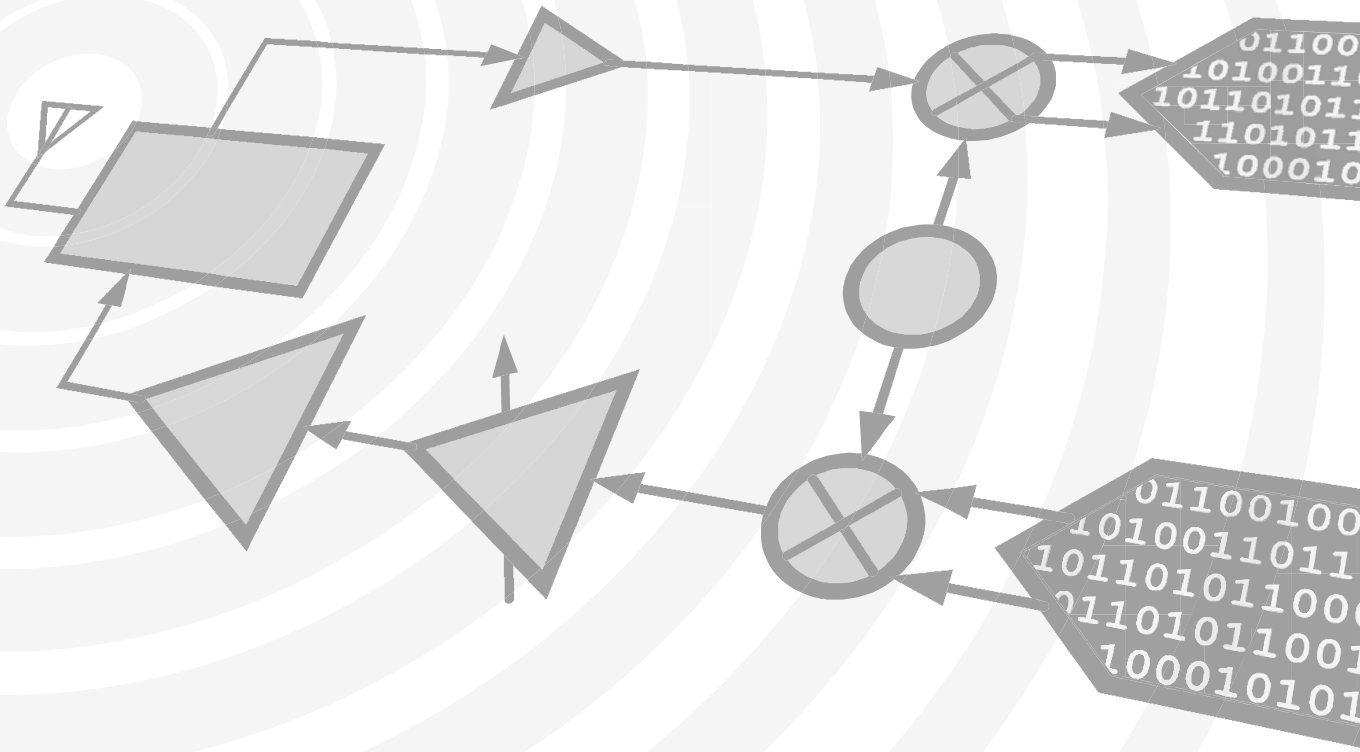

www.analog.com

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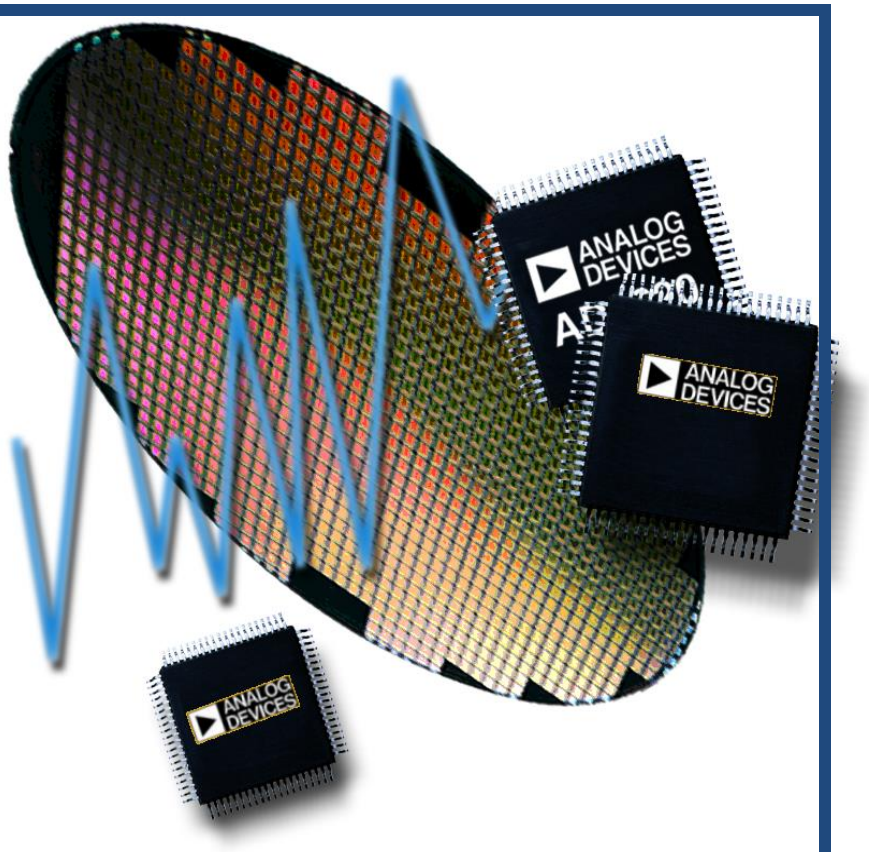

Reliability Report

Report Title: Qualification Test Report

Report Type: See Attached

Date: See Attached

Process FIT Rate Report

QTR: 2013- 00259 **Rev: 04**

Wafer Process: PHEMT-E

HMC756
HMC757
HMC949
HMC950
HMC952
HMC965
HMC995
HMC5846
HMC5879
HMC6741

Hittite Microwave Corporation is committed to:

- *Supplying products of the highest quality*
- *Advance in state-of-the-art technology that supports our products*
- *Enhance our competitive position with superior product standards*

Hittite's employees recognize the responsibility to:

- *Take the initiative to ensure product quality*
- *Create an environment where the highest standards are maintained*
- *Continue to improve quality practices*

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Introduction

The testing performed for this report is designed to accelerate the predominant failure mode, electro-migration (EM), for the devices under test. The devices are stressed at high temperature and DC biased to simulate a lifetime of use at typical operating temperatures. Using the Arrhenius equation, the acceleration factor (AF) is calculated for the stress testing based on the stress temperature and the typical use operating temperature.

This report is intended to summarize all of the High Temperature Operating Life Test (HTOL) data for the PHEMT-E process. The FIT/MTTF data contained in this report includes all the stress testing performed on this process to date and will be updated periodically as additional data becomes available. Data sheets for the tested devices can be found at www.hittite.com.

Glossary of Terms & Definitions:

1. **CDM:** Charged Device Model. A specified ESD testing circuit characterizing an event that occurs when a device acquires charge through some triboelectric (frictional) or electrostatic induction processes and then abruptly touches a grounded object or surface. This test was performed in accordance with JEDEC 22-C101.
2. **ESD:** Electro-Static Discharge. A sudden transfer of electrostatic charge between bodies or surfaces at different electrostatic potentials.
3. **HBM:** Human Body Model. A specified ESD testing circuit characterizing an event that occurs when a device is subjected to an electro-static charge stored in the human body and discharged through handling of the electronic device. This test was performed in accordance with JEDEC 22-A114.
4. **HAST:** Highly Accelerated Stress Test (biased). Devices are subjected to 96 hours of 85% relative humidity at a temperature of 130°C and pressure (15 PSIG), while DC biased. This test is performed in accordance with JESD22-A110.
5. **HTOL:** High Temperature Operating Life. This test is used to determine the effects of bias conditions and temperature on semiconductor devices over time. It simulates the devices' operating condition in an accelerated way, through high temperature and/or bias voltage, and is primarily for device qualification and reliability monitoring. This test was performed in accordance with JEDEC JESD22-A108.
6. **HTSL:** High Temperature Storage Life. Devices are subjected to 1000 hours at 150^{o}C per JESD22-A103.
7. **MSL:** Moisture sensitivity level pre-conditioning is performed per JESD22-A113.
8. **Operating Junction Temp (T_{oj}):** Temperature of the die active circuitry during typical operation.
9. **Stress Junction Temp (T_{sj}):** Temperature of the die active circuitry during stress testing.

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10. UHAST: Unbiased Highly Accelerated Stress Test. Devices are subjected to 96 hours of 85% relative humidity at a temperature of 130°C and pressure (15 PSIG). This test is performed in accordance with JESD22-A118.

Qualification Sample Selection:

All qualification devices used were manufactured and tested on standard production processes and met pre-stress acceptance test requirements.

Summary of Qualification Tests:

HMC965 (QTR11010)

TEST	QTY IN	QTY OUT	PASS / FAIL	NOTES
Initial Electrical	353	353	Complete	
HTOL, 1080 hours	78	78	Complete	
Post HTOL Electrical Test	78	78	Pass	
HTSL, 1000 hours	80	80	Complete	
Post HTSL Electrical Test	80	80	Pass	
MSL1 Preconditioning	159	159	Complete	
MSL1 Preconditioning Final Test	159	159	Pass	
UHAST (Preconditioned)	79	79	Complete	
UHAST Final Test	79	79	Pass	
Temperature Cycle (Preconditioned)	80	80	Complete	
Temperature Cycle Final Test	80	80	Pass	
ESD	36	36	Complete	HBM Class 1B CDM Class IV MM 50V

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HMC757 (QTR11014)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	70	70	Complete	
HTOL, 1000 hours	70	70	Complete	
Post HTOL Electrical Test	70	70	Pass	

HMC995 (QTR2012-00025)

TEST	QTY IN	QTY OUT	PASS / FAIL	NOTES
Initial Electrical			Complete	
HTOL, 1034 hours	78	78	Complete	
Post HTOL Electrical Test	78	78	Pass	
HTSL, 1000 hours	77	77	Complete	
Post HTSL Electrical Test	77	77	Pass	
MSL1 Preconditioning	154	154	Complete	
MSL1 Preconditioning Final Test	154	154	Pass	
HAST (Preconditioned)	77	77	Complete	
HAST Final Test	77	77	Pass	
Temperature Cycle (Preconditioned)	77	77	Complete	
Temperature Cycle Final Test	77	77	Pass	
ESD	36	36	Complete	HBM Class 0 CDM Class III

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HMC5879 (QTR2013-00067)

TEST	QTY IN	QTY OUT	PASS / FAIL	NOTES
Initial Electrical			Complete	
HTOL, 1000 hours	79	79	Complete	
Post HTOL Electrical Test	79	79	Pass	
HTSL, 1000 hours	80	80	Complete	
Post HTSL Electrical Test	80	80	Pass	
MSL3 Preconditioning	159	159	Complete	
MSL3 Preconditioning Final Test	159	159	Pass	
Temperature Cycle (Preconditioned)	80	80	Complete	
Temperature Cycle Final Test	80	80	Pass	
ESD	36	36	Complete	HBM Class 0 CDM Class IV

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PHEMT-E Failure Rate Estimate

Based on the HTOL test results, a failure rate estimation was determined using the following parameters:

With Device Operating Case Temp = 65°C

HMC965 (QTR11010)
Operating Junction Temp (T_{oj}) =118°C(391°K)
Stress Junction Temp (T_{sj}) = 150°C(423°K)

HMC757 (QTR11014)
Operating Junction Temp (T_{oj}) =115°C(388°K)
Stress Junction Temp (T_{sj}) = 180°C(453°K)

HMC995 (QTR2012-00025)
Operating Junction Temp (T_{oj}) =126°C(399°K)
Stress Junction Temp (T_{sj}) = 150°C(423°K)

HMC5879 (QTR2013-00067)
Operating Junction Temp (T_{oj}) =125°C(398°K)
Stress Junction Temp (T_{sj}) = 150°C(423°K)

Device hours:

HMC965 (QTR11010) = (78 X 1080hrs) = 84,240 hours
HMC757 (QTR11014) = (70 X 1000hrs) = 70,000 hours
HMC995 (QTR2012-00025) = (78 X 1034hrs) = 80,652 hours
HMC5879 (QTR2013-00067) = (77 X 1000hrs) = 77,000 hours

For PHEMT-E MMIC, Activation Energy = 1.3 eV

Acceleration Factor (AF): $$AF = \exp\left[\left(\frac{E_A}{k}\right)\cdot\left(\left(\frac{1}{T_{USE}}\right)-\left(\frac{1}{T_{STRESS}}\right)\right)\right]$$

HMC965 (QTR11010) Acceleration Factor = exp[1.3/8.6 e-5(1/391-1/423)] = 18.6
HMC757 (QTR11014) Acceleration Factor = exp[1.3/8.6 e-5(1/388-1/453)] = 267.8
HMC995 (QTR2012-00025) Acceleration Factor = exp[1.3/8.6 e-5(1/399-1/423)] = 8.6
HMC5879 (QTR2013-00067) Acceleration Factor = exp[1.3/8.6 e-5(1/398-1/423)] = 9.4

Equivalent hours = Device hours x Acceleration Factor

Equivalent hours = (84,240x18.6)+(70,000x267.8)+(80,652x8.6)+(77,000x9.4) = 2.17×10^7 hours

Since there were no failures and we used a time terminated test, F=0, and R = 2F+2 = 2

The failure rate was calculated using Chi Square Statistic:

$\lambda_{CL} = \frac{\chi^2_{\%CL,2f+2} \cdot 10^9}{2 \cdot t \cdot ss \cdot AF}$ at 60% and 90% Confidence Level (CL), with 0 units out of spec and a 65°C package backside temp;

Failure Rate

$\lambda_{60} = [(\chi^2)_{60,2}]/(2X\ \ 2.17x10^7)] = 1.8/\ 4.35x10^7 =\ \ 4.21x10^{-8}$ failures/hour or 42.1 FIT or MTTF = $2.38x10^7$ Hours

$\lambda_{90} = [(\chi^2)_{90,2}]/(2X\ \ 2.17x10^7)] = 4.6/\ 4.35x10^7 =\ \ 1.06x10^{-7}$ failures/hour or 106 FIT or MTTF = $9.43x10^6$ Hours

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