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RF PLL+VCO Power-Up & Brown-Out Design Considerations

Application Note

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Revision History

Revision	Date	Description
Rev 1.0	November 2012	First release
Rev 2.0	November 2012	Second release
Rev 2.1	March 2014	Third Release

2 Introduction

A device containing digital circuits needs to be properly powered up to ensure that the digital gates are initialized in a known state. This is important at initial device power-up as well as after an unscheduled power interruption or a power supply “brown-out” event.

This application note addresses the power-up management and partial loss of power events such as “brown-outs” and design considerations related to the Hittite RF PLL+VCO product lines. It should be noted that many of the concepts and recommendations in this note are applicable to all digital IC’s.

3 Applicable Products

This application note applies to the following products:

HMC820LP6CE	HMC821LP6CE	HMC822LP6CE	HMC824LP6CE	HMC826LP6CE
HMC828LP6CE	HMC829LP6GE	HMC830LP6GE	HMC831LP6CE	HMC833LP6GE
HMC834LP6GE	HMC836LP6CE	HMC837LP6CE	HMC838LP6CE	HMC839LP6CE
HMC840LP6CE	HMC1032LP6GE	HMC1033LP6GE	HMC1034LP6GE	

4 Proper Biasing of the Device

It is commonly known that applying voltages to IC signal pins prior to application of power can result in a state known as ‘Latch-Up’. Latch-Up injects charge into the substrate of the device and can cause the device to malfunction or create a short circuit across power supply rails through parasitic connections inside the IC. The Latch-Up state can only be cleared by first removing the offending signal voltage, then cycling power off, waiting, powering on and then applying the signal again. If left unchecked, Latch-Up can result in damage due to the excess current through the device.

In addition to Latch-Up, there are other reasons for making sure that no voltages are applied to the IC signal pins prior to the application of power. Frequently overlooked, ESD diodes inside an IC provide an undesired conduction path from signal pins through to power supply pins as shown in Figure 1. When power to VDD has not been applied yet, the upper ESD diode can conduct. This has the unfortunate effect of providing a significant bias on the power pins, which can partially power up the internal circuits.

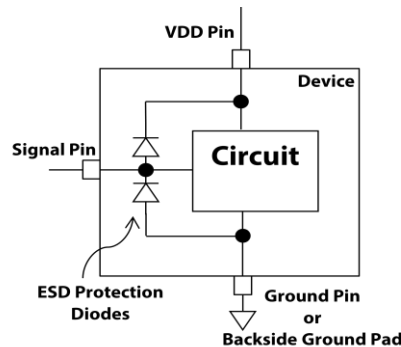


Figure 1 ESD Structure

One of the effects of this unwanted bias is that it can impair the function of the Power-On-Reset (POR) circuit. Figure 2 shows a simplified sketch of a POR circuit. The purpose of the POR circuit is to provide a delay at device power up until the power supplies are at a valid level and then resetting the digital circuits into a known state. This happens automatically every time the chip is powered up.

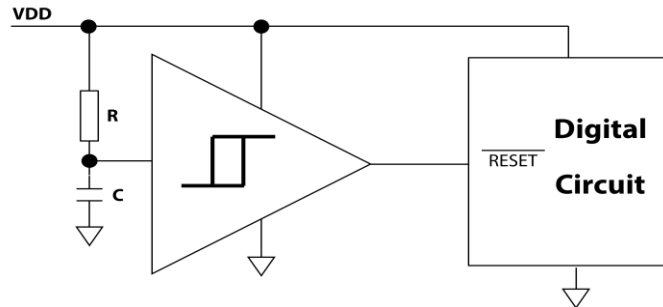


Figure 2 Simple POR Circuit

The time constant provided by the RC circuit delays the input voltage to the POR Schmitt trigger relative to the VDD voltage. This delay period needs to be long enough to ensure the digital circuit is held in reset until the VDD voltage level is sufficiently high for the digital circuits to maintain their state. If the POR circuit removes the reset and goes high before a valid VDD exists, then the digital circuits may not maintain the desired reset state and could start in an unknown or illegal condition.

When signal voltages and resulting path via the ESD diode to VDD are present prior to applying VDD then a partially charged RC chain inside the POR circuit may release reset early so that when VDD is applied, the digital circuits are not in the correct state.

In summary, stray voltages or external logic signals should not be applied to the device prior to VDD. This includes voltages from logic devices on all pins, such as serial port pins or even external clock sources on reference input pins.

5 Managing the Device Power-Up

Power management can be designed to handle device power-up at both start-up and after a brown-out event.

Power interruptions can occur at any time and can last from microseconds to hours. All electric utilities companies can experience power outages, and systems that rely on these electric utilities must be designed to manage such events by incorporating a power management scheme.

Power management at start-up and after a brown-out is often fully incorporated into the system's existing microcontroller. Alternatively, an external Brown-Out Detection (BOD) circuit can be implemented using the circuit shown in Figure 3. The ratio of resistors R and 2R sets the Brown-Out Detection threshold voltage. The comparator BOD signal is monitored by the system microcontroller.

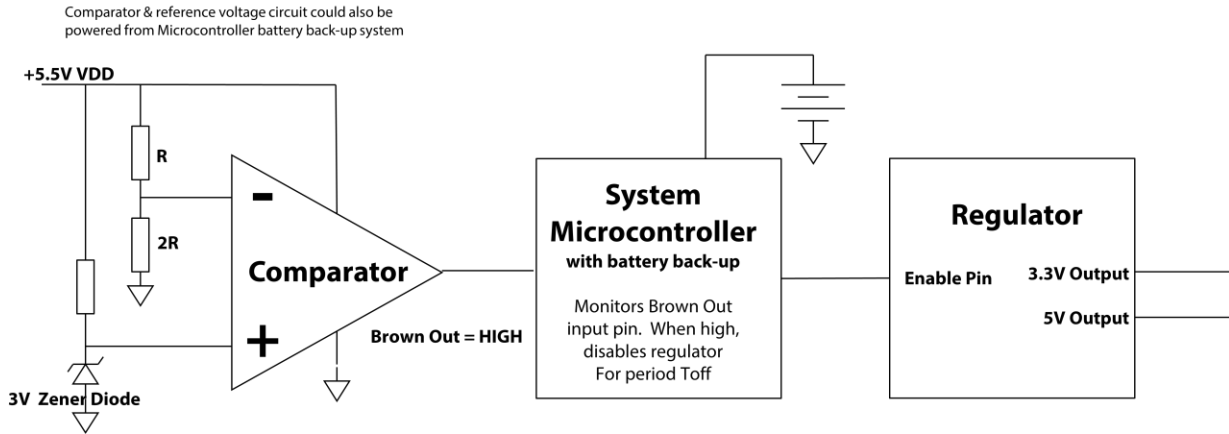


Figure 3 Simple Brown-Out Detection Circuit

Figure 4 shows the VDD power supply voltage of a device broken into four regions.

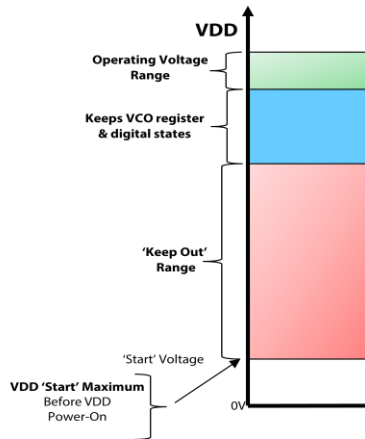


Figure 4 Circuit Power Supply Voltage Ranges

The highest power supply region, shown in green, is the supported operating voltage range stated in the device datasheet. The neighboring blue region shows the voltage range that, although not considered a normal operating voltage, is sufficient for the digital circuits to hold their states. This is called a ‘Keep Alive’ range. Devices operating in the red region (a ‘Keep Out’ range) can have unpredictable behavior because the digital states may be lost or partially corrupted. Finally, the white region shows the maximum limits for stray voltages on the chip pins prior to initialization of the power supply (the ‘Start’ voltage). To ensure proper power-up of the IC, the power supply pin should not linger above this (white) range before power is applied.

Let’s take a closer look at how to transition successfully across the ‘keep-out’ range and see what the maximum ‘Start’ voltage is.

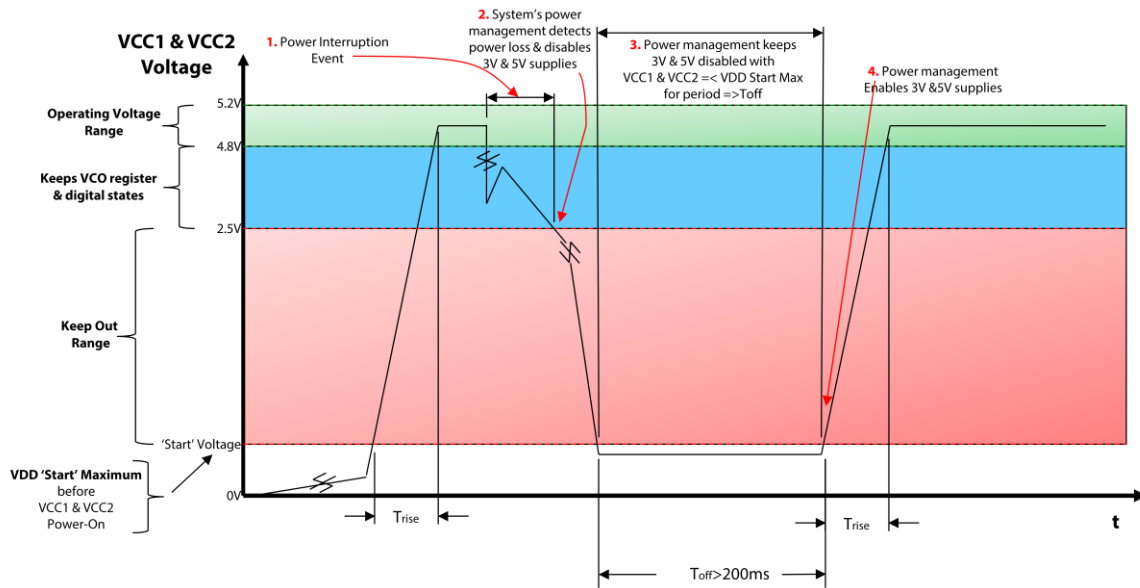


Figure 5 Power Supply Brown-Out Management

Figure 5 shows a common power-up and brown-out management scenario for an IC with a 5V supply. Two time intervals are shown, Trise and Toff. Trise is the power supply rise time while Toff is the period during which the supply rail must remain at or below the 'Start' voltage.

The first Trise event is typically an initial power-up event where the power supply is fully discharged and is coming up from or close to 0V. The sequence following the power-up is broken into four separate steps.

The example in Figure 5 shows a power interruption (or partial power brown out) event characterized by a sudden drop in supply voltage. These power supply drops can sometimes be followed by short-lived momentary recoveries, eventually reaching the lower limit of the 'Keep Alive' region.

The system's power management detects the voltage entering the 'Keep Out' range and disables the IC power supplies and other chips driving the IC including digital sources and the reference source driver. For Hittite devices with dual 3V and 5V power supplies the 3V supply should be brought down with the 5V supply as there is a bias path through to the 5V supply rail from the 3V supply rail when the 5V supply level is below the 3V supply. If left enabled, the 3V rail can bias the 5V rail to as high as 1.2V. A similar effect can occur when the reference source is driving the REFIN port of the device. Large switching levels from the source actually biases the 3V rail which in turn biases the 5V rail to an invalid level.

Power Management keeps the 3V and 5V, reference source driver disabled and external logic signals disabled or held low for a period of time ($T_{off} > 200ms$) after the VDD supply drops below the 'Start' Maximum voltage threshold. Microcontroller SPI signals going to the device (SCK, SEN, SDI, SDO, CE) must be low or floating (high impedance) during this Toff period to avoid unintentional biasing of the device.

Power Management system enables the 5V and 3V supply regulators and reference source driver. The preferred power supply sequence for Hittite PLL+VCOs is 5V supply up first followed by 3V, or coincident application of 5V and 3V. The 3V supply should not be more than 1V above the 5V supply during the power up event. After the 5V and 3V power supplies are stable, the microcontroller should assert a rising edge on SEN or SCK to force the device into the correct SPI mode (applicable to HMC devices that support more than one SPI mode of operation).

Figure 6 shows the maximum allowed 5V 'Start' level relative to Trise. The recommended operation region is the area below the curve. Supply rise times should not be slower than 40ms even with zero volts on the 5V supply at start up.

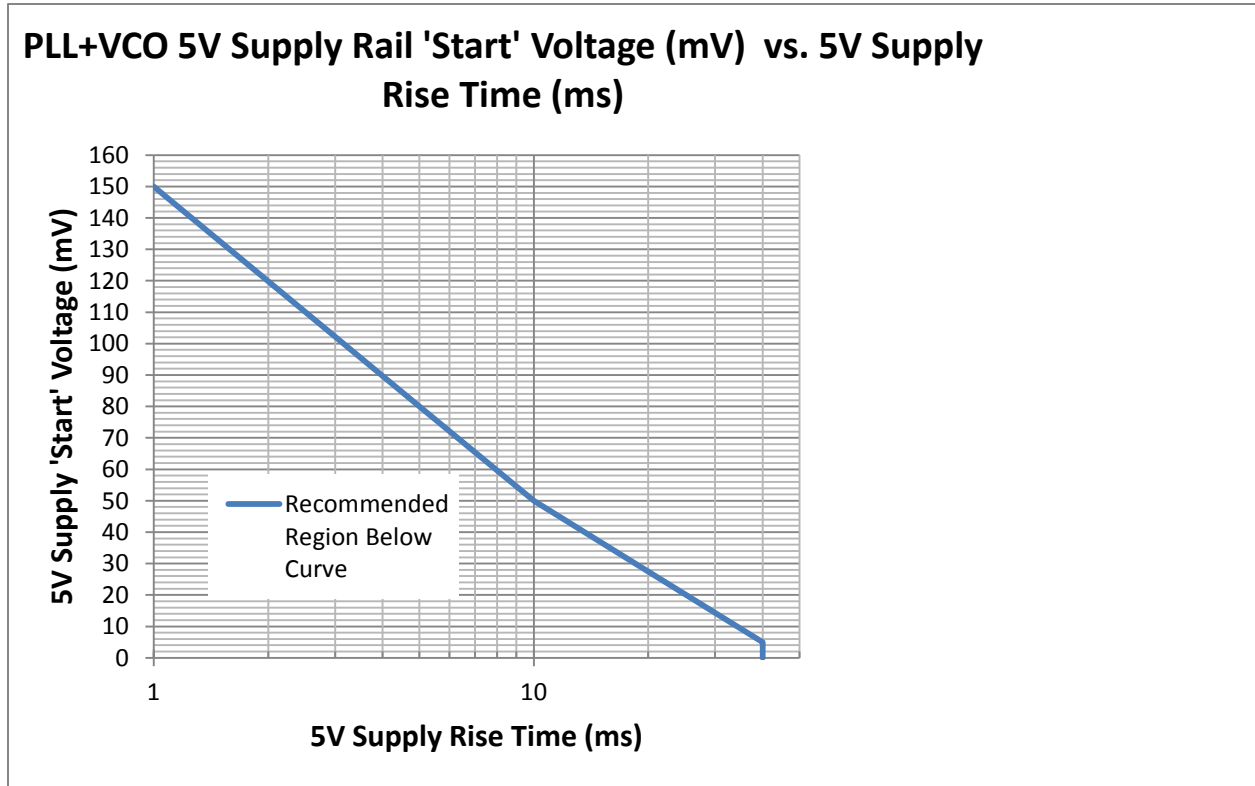


Figure 6 5V Power Supply 'Start' Voltage vs. Rise Time

6 Reference Designs

Figure 7 shows the regulator and PLL+VCO configuration for Hittite's family of RF PLL+VCO products for a 10ms power supply rise time.

Supply rail discharge time can be up to several seconds. Customers wishing to reduce the amount of downtime resulting from a brown-out event can install load resistors on the 3.3V and 5V regulator outputs or use an alternate means to discharge the supplies prior to start up.

Many Hittite PLL+VCOs support two serial programming interface (SPI) Modes. The SPI and other digital signals (SCK, SDI, SDO, SEN, CE) should be low or high impedance prior to VDD. Dual mode SPI selection on the devices is performed after each power-up (VDD application) and is determined by which rising edge occurs first: SEN (HMC Mode) or SCK (Open Mode) rising edge.

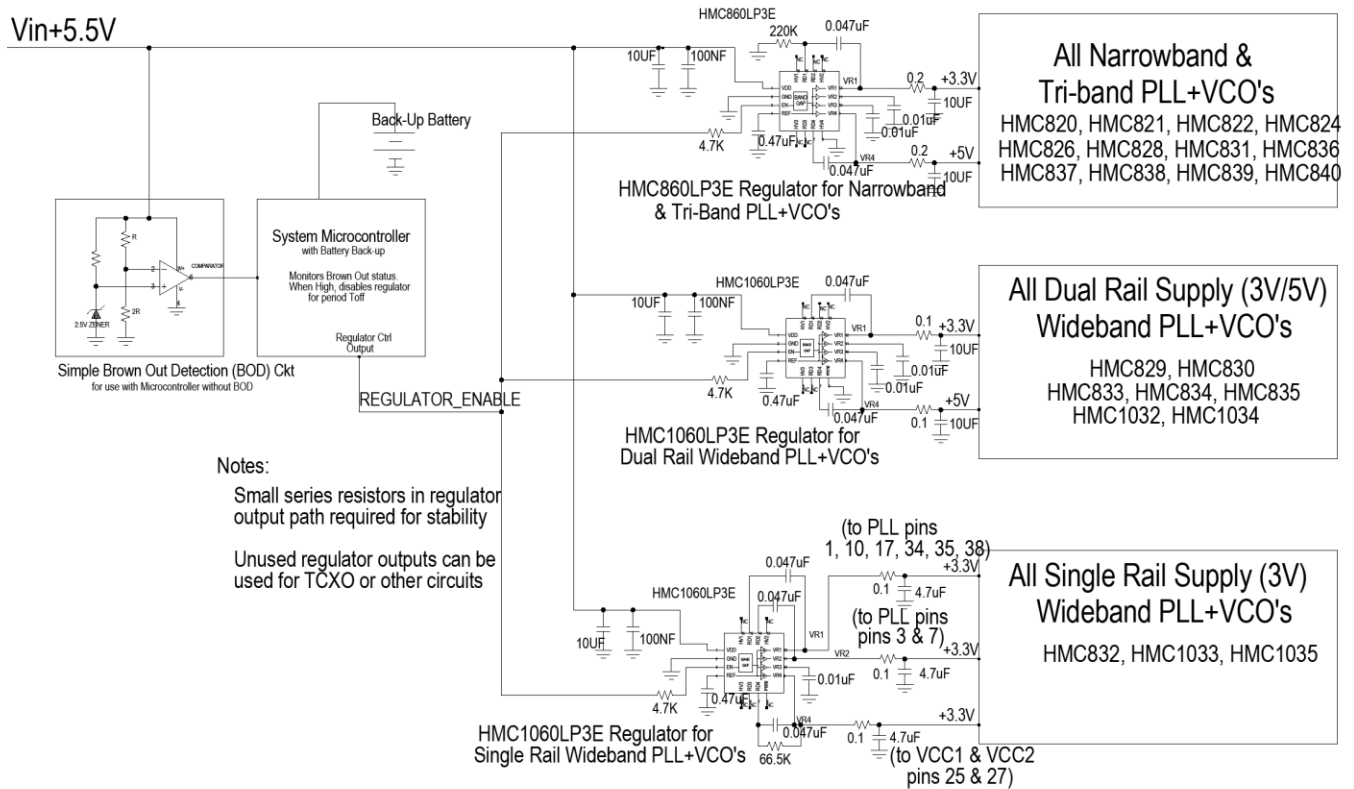


Figure 7 Power Management Reference Design Schematic

7 Conclusion

This application note gives an overview of power management of digital IC's in general and provides guidelines for Hittite PLL with integrated VCO IC's. The guidelines are for good power supply management practices and will ensure proper start-up of the IC's in the case of interrupted or illegal brown out supply conditions.

The following general practices are recommended:

- Stray voltages should be held below start threshold levels before application of power to the IC.
- Power supplies should ramp up with minimum rise times.
- Slower power supply rise times require lower stray voltage on start-up.
- Protection from partial power or brown out events requires special power management.
- Power supplies should be held off for a minimum of 200ms after supplies have discharged below the start threshold levels.
- Discharges to legal start levels may vary for different IC's. Faster discharges may require a small load discharge resistor or other type of supply discharge device.

- g) Interface IC's to the device should have their signals turned off or disabled in the event of a power down event.

8 References

Please refer to www.hittite.com for individual product datasheets.