LINEAR TECHNOLOGY

DESIGN NOTES

A Complete Compact APD Bias Solution for a 10Gbits/s GPON System – Design Note 447

Xin Qi

Introduction

Avalanche photo diode (APD) receiver modules are widely used in fiber optic communication systems. An APD module contains the APD and a signal conditioning amplifier, but is not completely self contained. It still requires significant support circuitry including a high voltage, low noise power supply and a precision current monitor to indicate the signal strength. The challenge is squeezing this support circuitry into applications with limited board space. The LT®3482 addresses this challenge by integrating a monolithic DC/DC step-up converter and an accurate current monitor. The LT3482 can support up to a 90V APD bias voltage, and the current monitor provides better than 10% accuracy over four decades of dynamic range (250nA to 2.5mA).

Recent communication design efforts increasingly focus on the 10Gbits/s GPON system, which demands that the transient response of the APD current monitor is less than 100ns for an input current step of two decades of magnitude. A simple compact circuit using the LT3482 is fast enough to meet this challenging requirement.

An APD Bias Topology with Fast Current Monitor Transient Response

The circuit in Figure 1 shows the LT3482 configured to produce an output voltage ranging from 20V to 45V from a 5V source—capable of delivering up to 2mA of load current. Its operation is straightforward. The LT3482 contains a 48V, 260mA internal switch, which boosts V_{OUT1} to one-half the APD output voltage level. This voltage is doubled through an internal charge pump to generate V_{OUT2}. All boost and charge pump diodes are integrated. V_{OUT2} is regulated by the internal voltage reference and the resistor divider made up of R3 and R4. At this point, V_{OUT2} goes through the integrated high side current monitor (MONIN), which produces a current proportional to the APD current at the MON pin.

The output voltage is available for the APD at the APD pin. The CTRL pin serves to override the internal reference. By tying this pin above 1.25V, the output voltage is regulated with the feedback at 1.25V. By externally setting the CTRL pin to a lower voltage, the feedback and the output voltage follow accordingly.

The $\overline{SHDN}$ pin not only enables the converter when 1.5V or higher is applied, but also provides a soft-start function to control the slew rate of the switch current, thereby minimizing inrush current. The switching frequency can be set to 650kHz or 1.1MHz by tying the FSET pin to ground or to V_{IN}, respectively. Fixed frequency operation allows for an output ripple that is predictable and easier to filter.

To achieve fast transient response, any time-delay component along the signal path should be minimized. Figure 1 shows an APD bias topology with fast current monitor transient response. Unlike the ultralow noise topology

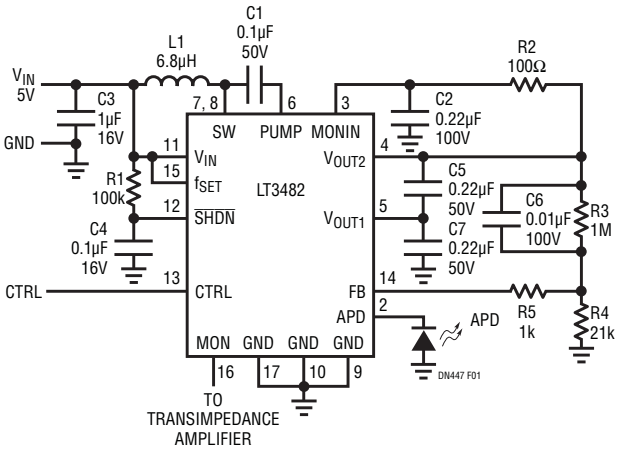

Figure 1. Fast Current Monitor Transient Response ADP Bias Topology

with a filter capacitor at the APD pin, the filter capacitor is moved to the MONIN pin of the LT3482. The output sourcing current from the MON pin is directly fed into a transimpendance amplifier.

A typical measured current monitor transient response consists of the signal generation delay at the APD pin, the built-in current monitor response time and the measurement delay at the MON pin. Thus, every effort should be made to reduce signal generation and the measurement delays.

Figure 2 shows the measurement setup. An NPN transistor in common base configuration is used to generate the fast current step representing the APD load. A function generator provides two negative bias voltages at the PWM node that result in two decades current step at the APD pin. At the MON pin, a wideband transimpedence amplifier is implemented using the LT1815. Operating in a shunt configuration, the amplifier buffers the MON output current and dramatically reduces the effective output impedance at the OUT node. Note that there is an inversion and a DC offset present when this measurment technique is used. A regular oscilloscope probe can then be used to capture the fast transient response at the OUT node.

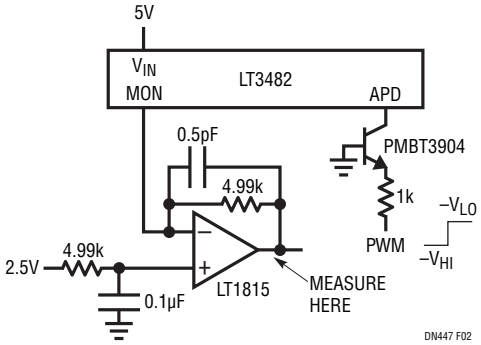

Figure 2. Fast Transient Response Measurement Setup

Figures 3 and 4 show the measured input signal rising transient response and the measured input signal falling transient response, respectively, where the input current levels are 10µA and 1mA. The PWM input signal levels are selected based on the static measurement results. The APD current is accurately mirrored by the LT3482 with an attenuation of five and sourced from the MON pin. With a 2.5V reference voltage, the OUT node voltage swings between 1.5V (= 2.5V – 1mA/5 • 4.99k) and 2.49V (= 2.5V – 10µA/5 • 4.99k) responding to the input signal step. The measurements demonstrate less than 50ns transient response time, which exceeds the stringent speed demand of the 10Gbits/s GPON system.

Conclusion

The LT3482 is a complete space-saving solution to APD receiver module support circuitry design. It offers more than just low bias noise and compact solution size; it also features UltraFast™ current monitor transient speed that addresses the challenges presented in the 10Gbits/s GPON system.

UltraFast is a trademark of Linear Technology Corporation.

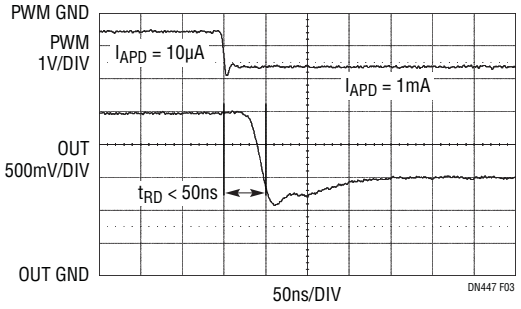

Figure 3. Transient Response on Input Signal Rising Edge (10µA to 1mA)

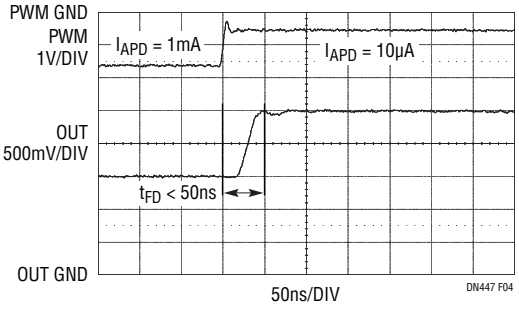

Figure 4. Transient Response on Input Signal Falling Edge (1mA to 10µA)

Data Sheet Download

www.linear.com

For applications help,
call (408) 432-1900, Ext. 3231

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

dn447f LT/TP 0808 392K • PRINTED IN THE USA