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Differential Amplifier with an Ultraprecision Matched Resistor Network

FEATURES

Enables quick evaluation of the LT5401 with a fully differential amplifier

Standalone, fully differential evaluation board with high CMRR vs. frequency (82 dB at 1 MHz)

High gain precision over full operating temperature range (0.01%)

APPLICATIONS

Fully differential amplifiers

EQUIPMENT NEEDED

Dual supply Waveform generator 300 MHz oscilloscope

DOCUMENTS NEEDED

LT5401 data sheet ADA4932-1 data sheet

GENERAL DESCRIPTION

The Analog Devices, Inc., EVAL-LT5401_32FDAZ allows the user to evaluate the performance of the LT5401. The LT5401 is an ultraprecision matching resistor network used to configure the gain of a fully differential amplifier. The on-board LT5401 is paired with a 300 MHz, fully differential amplifier circuit (the ADA4932-1).

The EVAL-LT5401_32FDAZ accepts either a single-ended or a differential input signal.

Optimized power and ground planes ensure low noise and high speed operation. Component placement and power supply bypassing allow maximum circuit flexibility and optimal performance.

Full specifications on the LT5401 and the ADA4932-1 are available in the LT5401 and ADA4932-1 data sheets, respectively. Consult the data sheets in conjunction with this user guide when working with the EVAL-LT5401_32FDAZ.

EVAL-LT5401_32FDAZ PHOTOGRAPH



Figure 1.

EVAL-LT5401_32FDAZ User Guide

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REVISION HISTORY

11/2019—Revision 0: Initial Version

7278-003

EVALUATION BOARD HARDWARE

The on-board LT5401 and ADA4932-1 ensure a common-mode rejection (CMR) of \geq 94 dB, 0.002% gain error, and 1 ppm/°C gain drift over the entire operating temperature range. The LT5401 data sheet provides detailed electrical specifications and applications information.

DIFFERENTIAL INPUT AND OUTPUT

Two input Subminiature Version A (SMA) edge connectors (+IN and –IN) and two output SMA connectors (–OUT and +OUT) provide either a fully differential input and output connection, or a single-ended input to a differential output connection. A single-ended input connection to +IN from a 50 Ω source requires a 50 Ω termination to the –IN input. Any impedance in series with an input or output increases the matching error of the LT5401.

DIFFERENTIAL GAIN CONFIGURATION

Figure 2 shows the LT5401 matched resistors block diagram. The LT5401 IN1 pin connects to the –IN SMA connector of the EVAL-LT5401_32FDAZ, and the LT5401 IN2 pin connects to the +IN SMA connector of the EVAL-LT5401_32FDAZ. These SMA connectors can be driven by either a differential or single-ended voltage source. The LT5401 OUT1 pin connects to the –OUT pin of the ADA4932-1, and the LT5401 OUT2 pin connects to the +OUT pin of the ADA4932-1. These connections are made through the ADA4932-1 –FB pin and +FB pin (see Figure 5).

The possible gain configurations for the EVAL-LT5401_32FDAZ include the following:

- Gain = 0 dB in the default board configuration. The LT5401 T1B pin and T2B pin connect to the differential amplifier inputs through the 0 Ω R5 and R6 resistors.
- Gain = 6 dB. The T1A pin and the T2A pin connect to the differential amplifier inputs. Remove the R5 resistor and R6 resistor, and install 0 Ω on the R3 resistor and R4 resistor.
- Gain = -6 dB. The T1C pin and the T2C pin connect to the differential amplifier inputs. Remove the R5 resistor and R6 resistor, and install 0 Ω on the R7 resistor and R8 resistor.

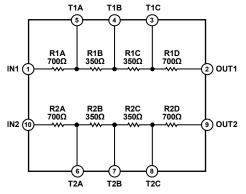
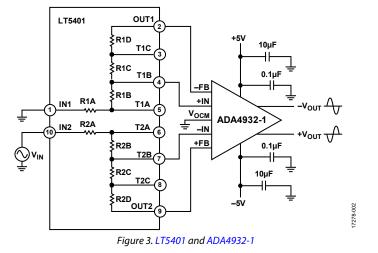


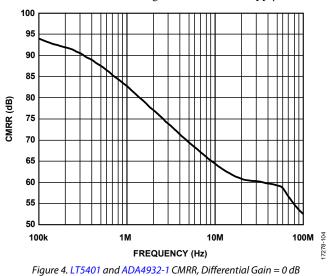
Figure 2. LT5401 Matched Resistors Block Diagram

The default gain configuration of the EVAL-LT5401_32FDAZ is 0 dB (see Figure 3).



COMMON MODE REJECTION RATIO (CMRR)

Figure 4 shows the input CMRR vs. the frequency of the LT5401 with the ADA4932-1. A 0 dB gain and dual 5 V supply are used.

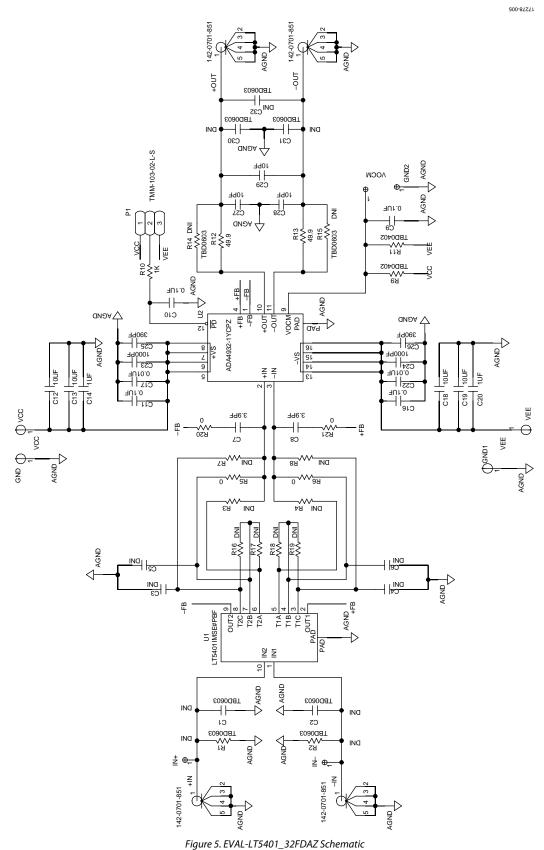


DISABLE

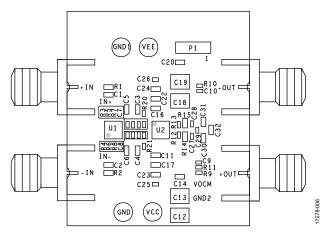
The ADA4932-1 power-down input, Pin 12, is connected to Position 2 of the 3-position P1 header connector.

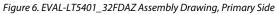
Insert the shunt of the P1 jumper on Position 1 and Position 2 to enable the ADA4932-1. Insert the shunt of the P1 jumper on Position 2 and Position 3 to disable the ADA4932-1 (see P1 in Figure 5).

EVALUATION BOARD SCHEMATIC AND ARTWORK



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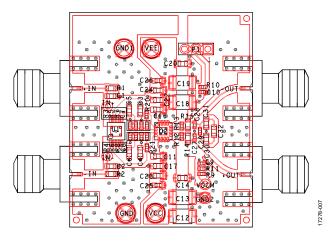


Figure 7. EVAL-LT5401_32FDAZ Layout Pattern, Primary Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 1. Bill of Materials

ltem	Qty	Reference Designator	Description	Manufacturer	Part Number
1	1	Not applicable	EVAL-LT5401_32FDAZ	Analog Devices	08-050344
2	1	U1	LT5401	Analog Devices	LT5401IMSE#PBF
3	1	U2	ADA4932-1	Analog Devices	ADA4932-1YCPZ-R7
4	4	+IN, +OUT, -IN, -OUT	Connectors, SMA, printed circuit board (PCB), 50 Ω end launch jack receptor	CINCH	142-0701-851
5	2	C9, C10	Ceramic capacitors, X7R, C0402	Kemet	C0402C104K4RACTU
6	2	C11, C16	Ceramic capacitors, X7R, C0603	Yageo	CC0603KRX7R9BB104
7	4	C12, C13, C18, C19	Ceramic capacitors, X7R, C1210H106	Murata	GCM32ER71E106KA57L
8	2	C14, C20	Ceramic capacitors, X7R, C0603	AVX	0603YC105KAT2A
9	2	C17, C22	Ceramic capacitors, X7R, C0603	Yageo	CC0603KRX7R9BB103
10	2	C23, C24	Ceramic capacitors, X7R, C0603	TDK	C1608C0G2A102J
11	2	C25, C26	Ceramic capacitors, C0G, C0402	Murata	GCM1555C1H391JA16D
12	3	C27 to C29	Ceramic capacitors, C0G, C0402	AVX	MK0227100FAT2A
13	2	C7, C8	Ceramic capacitors, NP0, C0G	Murata	GJM1555C1H3R9BB01D
14	9	C1 to C6, C30 to C32	User defined capacitors, C0603	Not Applicable	Not Applicable
15	8	R1, R2, R14 to R19	User defined resistors, R0603	Not Applicable	Not Applicable
16	6	R3, R4, R7, R8, R9, R11	User defined resistors, R0402	Not Applicable	Not Applicable
17	1	R10	Thick film resistor, R0402	Panasonic	ERJ-2RKF1001X
18	2	R12, R13	Thick film resistors, R0402	Panasonic	ERJ-2RKF49R9X
19	4	R5, R6, R20, R21	Thick film resistors, R0402	Panasonic	ERJ-2GE0R00X
20	4	VCC, VEE, GND, GND1	Terminal turrets	Mill-Max	2501-2-00-80-00-00-07-0
21	1	P1	Connector header, 3-position	Samtec Inc	TMM-103-02-L-S

ESD Caution ESD (electro

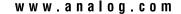
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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