LT7182S PMBus/I²C Reference Manual

OVERVIEW

This reference manual describes the digital communications capabilities of the LT®7182S, including the functionality of each LT7182S PMBus command. Please refer to the following specifications for more information regarding bus protocol details.

- PMBus Specification Revision 1.3.1
- SMBus Specification Revision 3.1

PMBus/SMBus/I²C CAPABILITIES

The LT7182S serial interface is PMBus compliant and can operate at any frequency between 10kHz and 1MHz. The device address is configurable using the EEPROM and/or a configuration resistor on ASEL. The serial interface supports the following protocols defined in the PMBus and SMBus specifications.

- Send Byte, Write Byte, Write Word, Block Write
- Read Byte, Read Word, Block Read
- Alert Response Address
- PAGE_PLUS_READ, PAGE_PLUS_WRITE
- Zone Write
- SMBALERT_MASK Read and Write

The LT7182S pulls the $\overline{\text{ALERT}}$ pin low to indicate conditions that may require attention. Please see the Status section in PMBus Command Details section for more information.

SIMILARITY BETWEEN PMBus, SMBus AND I²C 2-WIRE INTERFACE

The PMBus 2-wire interface is an incremental extension of the SMBus. SMBus is built upon I²C with some minor differences in timing, DC parameters and protocol. The PMBus/SMBus protocols are more robust than simple I²C byte commands because PMBus/SMBus provide timeouts to prevent persistent bus errors and optional packet error checking (PEC) to ensure data integrity. In general, a bus controller device that can be configured for I²C communication can be used for PMBus communication with little or no change to hardware or firmware. Repeat start (restart) is not supported by all I²C controllers but is required for SMBus/PMBus reads. If a general purpose I²C controller is used, please check that repeat start is supported.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.3.1: Section 5: Transport.

For a description of the differences between SMBus and I²C, refer to System Management Bus (SMBus) Specification Version 3.1: Appendix B—Differences Between SMBus and I²C.

COMMUNICATION PROTECTION

All read operations will return a valid PEC if the PMBus controller requests it. If bit 2 of the MFR_CONFIG_ALL_LT7182S command is set, the PMBus write operations will not be acted upon until a valid PEC has been received by the LT7182S. If a PEC is included in a command write, that PEC must be valid or a PEC write error will occur, regardless of the value of bit 2 of the MFR_CONFIG_ALL_LT7182S command.

If a PEC write error occurs, an attempt is made to access unsupported commands, or invalid data is written to supported commands, then the LT7182S ignores the command, sets the CML bit in the STATUS_BYTE and STATUS_WORD commands, sets the appropriate bit in the STATUS_CML command, and pulls the $\overline{\text{ALERT}}$ pin low.

DEVICE ADDRESSING

The LT7182S offers addressing modes that provide flexible ways to control multiple channels at once as well as individually.

Device addressing is the standard way to communicate with a single instance of the LT7182S. The value of the

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device address is set by a combination of the ASEL configuration pin and the MFR_ADDRESS command. Device addressing can be disabled by writing a value of 0x80 to the MFR_ADDRESS. Individual channels are accessed using the PAGE command to select the desired channel, or by using the PMBus PAGE_PLUS command. If MFR_ADDRESS cannot be read from NVM due to an NVM fault, the device address will be set to 0x7C.

Global addressing provides a means to address all LT7182S devices on the bus. The LT7182S global addresses are fixed at 0x5A (7-bit notation) and 0x5B. They cannot be disabled. Commands sent to the 0x5A global address act the same as if PAGE is set to a value of 0xFF. Commands sent are written to both channels simultaneously. Global address 0x5B is paged and allows channel specific command of all LT7182S devices on the bus. Do not read from global addresses, as multiple devices may respond simultaneously. Other ADI device types may respond at one or both of these global addresses.

Rail addressing provides a means to control multiple channels connected together to produce a single output voltage (PolyPhase®). While similar to global addressing, the rail address can be dynamically assigned with the paged MFR_RAIL_ADDRESS command, allowing for any logical grouping of channels that might be required for reliable system control. Do not read from rail addresses since multiple ADI devices may respond.

Zone write addressing provides a means to write to a set of channels. The set of channels may be distributed across multiple devices. Each channel is programmed to be part of a zone by programming the selected zone number to the ZONE_CONFIG command for that page. This configuration only needs to be performed once. After zone configuration, the bus controller uses the ZONE_ACTIVE command to select the active zone. If a channel's configured zone matches the active zone, or the active zone is set to the "All Zone", the channel will respond to subsequent ZONE_WRITE operations. A ZONE_WRITE operation is started when the bus controller uses the ZONE_WRITE address (0x37, 7-bit notation) as the device address in an SMBus write command.

All means of PMBus addressing require the user to employ disciplined planning to avoid addressing conflicts. Communication to LT7182S devices at global and rail addresses should be limited to command write operations.

COMMUNICATION RECOMMENDATIONS

If PMBus commands are received faster than they are being processed, the part may become too busy to handle new commands. If a command is written when the device is busy processing a command, the device will ignore that command, set bit 7 of STATUS_BYTE and pull the $\overline{\text{ALERT}}$ pin low. MFR_COMMON bit 6 will be set to a 1 when the device is ready to accept commands. This bit may be polled before writing commands. Alternatively, clock stretching may be enabled. Clock stretching is enabled by setting bit 1 of MFR_CONFIG_ALL_LT7182S.

NVM commands may take longer to process, including STORE_USER_ALL, MFR_COMPARE_USER_ALL, and MFR_FAULT_LOG_CLEAR. When writing repeated VOUT_MAX or MFR_PWM_MODE_LT7182S commands to both channels simultaneously at bus speeds above 400kHz, the device may also become too busy to respond immediately. In these cases, either poll MFR_COMMON bit 6 or enable clock stretching to avoid a busy condition.

Table 1 list supported PMBus commands and manufacturer specific commands. A complete description of the included PMBus commands can be found in the PMBus Power System Management Protocol Specification. Floating point values listed in the "DEFAULT VALUE" column are half-precision IEEE floating point numbers. If MFR_CONFIG_ALL is used to disable IEEE floating point mode, all floating point commands will read and write values using either Linear11 or ULinear16 format, as indicated by the DATA FORMAT column in Table 1. Please see Table 2 for data format details. All commands from 0xC0 through 0xFF not listed in Table 1 are implicitly reserved by the manufacturer. Users should avoid blind writes within this range of commands to avoid undesired operation of the part. All commands from 0x00 through 0xBF not listed in Table 1 are implicitly not supported by the manufacturer. Attempting to access non-supported or reserved commands may result in a CML command fault event.

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COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
PAGE	0x00	Provides integration with multi-page PMBus devices.	R/W Byte	N	Reg			0x00
OPERATION	0x01	Operating mode control. On/off, margin high and margin low.	R/W Byte	Y	Reg		Y	0x80
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on/off command configuration.	R/W Byte	Y	Reg		Y	0x1E
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				
PAGE_PLUS_WRITE	0x05	Write a command directly to a specified page.	W Block	N				
PAGE_PLUS_READ	0x06	Read a command directly from a specified page.	Block R/W	N				
ZONE_CONFIG	0x07	Assigns current page to specified zone number for ZONE_WRITE operations.	W Word	Y	Reg		Y	0xFEFE
ZONE_ACTIVE	0x08	Selects active zone for ZONE_WRITE operations.	W Word		Reg			0xFEFE
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Send Byte	N				
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xD8
QUERY	0x1A	Asks if a given command is supported, and what data formats are supported.	Block R/W	N	Reg			
SMBALERT_MASK	0x1B	Masks $\overline{\text{ALERT}}$ activity.	Block R/W	Y	Reg		Y	
VOUT_MODE	0x20	Output voltage format and exponent.	R Byte	N	Reg			0x60
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	IEEE/ UL16	V	Y	0.5 0x3800
VOUT_MAX	0x24	Upper limit on the commanded output voltage.	R/W Word	Y	IEEE/ UL16	V	Y	0.537 0x384C
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point.	R/W Word	Y	IEEE/ UL16	V	Y	0.525 0x3833
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point.	R/W Word	Y	IEEE/ UL16	V	Y	0.475 0x379A
VOUT_TRANSITION_RATE	0x27	Rate the output changes when V_{OUT} commanded to a new value.	R/W Word	Y	IEEE/L11	V/ms	Y	0.25 0x3400
FREQUENCY_SWITCH	0x33	Switching frequency of the regulator.	R/W Word	N	IEEE/L11	kHz	Y	1000.0 0x63D0
VIN_ON	0x35	Input voltage at which the unit should start power conversion.	R/W Word	Y	IEEE/L11	V	Y	Ch. 0: 1.5 0x3E00 Ch. 1: 1.4 0x3D9A

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COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
VIN_OFF	0x36	Input voltage at which the unit should stop power conversion.	R/W Word	Y	IEEE/L11	V	Y	Ch. 0: 1.45 0x3DCD Ch. 1: 1.35 0x3D66
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	IEEE/L11	V	Y	0.55 0x3866
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	IEEE/L11	V	Y	0.537 0x384C
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	IEEE/L11	V	Y	0.467 0x3779
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	IEEE/L11	V	Y	0.465 0x3771
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0x00
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	IEEE/L11	A	Y	8.0 0x4800
OT_FAULT_LIMIT	0x4F	Internal overtemperature fault limit.	R/W Word	N	IEEE/L11	C	Y	160.0 0x5900
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an external overtemperature fault is detected.	R/W Byte	N	Reg		Y	0xC0
OT_WARN_LIMIT	0x51	Internal overtemperature warning limit.	R/W Word	N	IEEE/L11	C	Y	140.0 0x5860
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	Y	IEEE/L11	V	Y	–1.0 0xBC00
IIN_OC_WARN_LIMIT	0x5D	Input supply overcurrent warning limit.	R/W Word	Y	IEEE/L11	A	Y	8.0 0x4800
TON_DELAY	0x60	Time from RUN and/or Operation on to output rail turn-on.	R/W Word	Y	IEEE/L11	ms	Y	0.0 0x0000
TON_RISE	0x61	Time from when the output starts to rise until the output voltage reaches the VOUT commanded value.	R/W Word	Y	IEEE/L11	ms	Y	1.0 0x3C00
TON_MAX_FAULT_LIMIT	0x62	Maximum time from the start of TON_RISE for VOUT to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	IEEE/L11	ms	Y	5.0 0x4500
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken by the device when a TON_ MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0x00
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL ramp.	R/W Word	Y	IEEE/L11	ms	Y	0.0 0x0000
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	IEEE/L11	ms	Y	2.0 0x4000
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL completed, for the unit to decay below MFR_DISCHARGE_THRESHOLD.	R/W Word	Y	IEEE/L11	ms	Y	0.0 0x0000

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Table 1. PMBus Command Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R/W Byte	Y	Reg			
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R/W Word	Y	Reg			
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Reg			
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Reg			
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	Y	Reg			
STATUS_TEMPERATURE	0x7D	Internal temperature fault and warning status for READ_TEMERATURE_1.	R/W Byte	N	Reg			
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W Byte	N	Reg			
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R/W Byte	Y	Reg			
READ_VIN	0x88	Measured input supply voltage.	R Word	Y	IEEE/L11	V		
READ_IIN	0x89	Measured input supply current.	R Word	Y	IEEE/L11	A		
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	IEEE/ UL16	V		
READ_IOUT	0x8C	Measured output current.	R Word	Y	IEEE/L11	A		
READ_TEMPERATURE_1	0x8D	Measured internal temperature.	R Word	N	IEEE/L11	C		
READ_FREQUENCY	0x95	Measured PWM switching frequency.	R Word	Y	IEEE/L11			
READ_POUT	0x96	Calculated output power.	R Word	Y	IEEE/L11			
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.3.	R Byte	N	Reg			0x33
MFR_ID	0x99	The manufacturer ID in ASCII.	R Block	N				"ADI"
MFR_MODEL	0x9A	The part number in ASCII.	R Block	N				"LT7182S"
MFR_REVISION	0x9B	Part revision number.	R Block	N				
MFR_SERIAL	0x9E	Unique part serial number.	R Block	N				
IC_DEVICE_ID	0xAD	Identification of the IC in ASCII.	R Block	N				"LT7182S"
IC_DEVICE_REV	0xAE	Revision of the IC.	R Block	N				
MFR_EE_UNLOCK	0xBD	Contact factory.						
MFR_EE_ERASE	0xBE	Contact factory.						
MFR_EE_DATA	0xBF	Contact factory.						

PMBus COMMAND SUMMARY

Table 1. PMBus Command Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
MFR_USER_DATA_00	0xC9	EEPROM word available for user	R/W Word	N	Reg		Y	0x0000
MFR_USER_DATA_01	0xCA	EEPROM word available for user	R/W Word	N	Reg		Y	0x0000
MFR_USER_DATA_02	0xCB	EEPROM word available for user	R/W Word	N	Reg		Y	0x0000
MFR_USER_DATA_03	0xCC	EEPROM word available for user	R/W Word	N	Reg		Y	0x0000
MFR_READ_EXTVCC	0xCD	Measured EXTVCC voltage, when enabled	R Word	N	IEEE/L11	V		
MFR_READ_ITH	0xCE	Measured I_{TH} voltage, when enabled	R Word	Y	IEEE/L11	V		
MFR_CHAN_CONFIG_LT7182S	0xD0	Configuration bits that are channel specific.	R/W Word	Y	Reg		Y	Ch. 0: 0x00D7 Ch. 1: 0x0057
MFR_CONFIG_ALL_LT7182S	0xD1	General configuration bits.	R/W Word	N	Reg		Y	0x0100
MFR_FAULT_PROPAGATE_LT7182S	0xD2	Configuration that determines which faults are propagated to the $\overline{FAULT}$ pin.	R/W Word	Y	Reg		Y	0xE0D7
MFR_PWM_MODE_LT7182S	0xD4	Configuration for the PWM engine.	R/W Word	Y	Reg		Y	0x1DD4
MFR_FAULT_RESPONSE	0xD5	Action to be taken by the device when the $\overline{FAULT}$ pin is externally asserted low.	R/W Byte	Y	Reg		Y	0xC0
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_IOUT since last MFR_CLEAR_PEAKS.	R Word	Y	IEEE/L11	A		
MFR_ADC_CONTROL_LT7182S	0xD8	Configures the update rate of the measurements taken by the ADC.	R/W Byte	N	Reg		Y	0x00
MFR_RETRY_DELAY	0xDB	Retry interval during fault retry mode.	R/W Word	Y	IEEE/L11	ms	Y	10.0 0x4900
MFR_RESTART_DELAY	0xDC	Minimum time the RUN pin is held low by the LT7182S.	R/W Word	Y	IEEE/L11	ms	Y	10.0 0x4900
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT since last MFR_CLEAR_PEAKS.	R/W Word	Y	IEEE/UL16	V		
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since last MFR_CLEAR_PEAKS.	R/W Word	Y	IEEE/L11	V		
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of internal temperature (READ_TEMPERATURE_1) since last MFR_CLEAR_PEAKS.	R/W Word	N	IEEE/L11	C		
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Send Byte	N				
MFR_DISCHARGE_THRESHOLD	0xE4	Output voltage used to determine output has decayed sufficiently to re-enable the channel	R/W Word	Y	IEEE/L11		Y	0.2 0x3266
MFR_PADS_LT7182S	0xE5	Digital status of the I/O pads.	R Word	N	Reg			
MFR_ADDRESS	0xE6	Sets the 7-bit I^2C address byte.	R/W Word	N	Reg		Y	0x4F

PMBus COMMAND SUMMARY

Table 1. PMBus Command Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE
MFR_SPECIAL_ID	0xE7	ID code used by manufacturer.	R Word	N	Reg			0x1C1D
MFR_FAULT_LOG_TIMESTAMP_MSBS	0xE8	Sets the fault log timestamp upper 13 bits, clears lower 32 (read and write first)	R/W 32	N				
MFR_FAULT_LOG_TIMESTAMP_LSBS	0xE9	Sets the fault log timestamp lower 32 bits.	R/W 32	N				
MFR_FAULT_LOG_STORE	0xEA	Force a fault log entry to be written.	Send Byte	N				
MFR_FAULT_LOG_CLEAR	0xEC	Erases all fault log entries, if any.	Send Byte	N				
MFR_FAULT_LOG	0xEE	Read contents of fault log, if any.	R Block	N	Reg			
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with EEPROM.	Send Byte	N				
MFR_CHANNEL_STATE	0xF1	Returns the state of the channel.	R Byte	Y	Reg			
MFR_PGOOD_DELAY	0xF2	Time output voltage must be between UV and OV before PGOOD transitions high	R/W Word	Y	IEEE/L11	ms	Y	1.0 0x3C00
MFR_NOT_PGOOD_DELAY	0xF3	Time output voltage must be below UV or above OV before PGOOD transitions low	R/W Word	Y	IEEE/L11	ms	Y	0.1 0x2E66
MFR_PWM_PHASE_LT7182S	0xF5	Set PWM phase.	R/W Word	Y	IEEE/L11	Degrees	Y	Ch. 0: 0.0 0x0000 Ch. 1: 180.0 0x59A0
MFR_SYNC_CONFIG_LT7182S	0xF6	SYNC pin input/output configuration	R/W Byte	N	Reg		Y	0x00
MFR_PIN_CONFIG_STATUS	0xF7	Pin configuration fault status	R Byte	N	Reg			
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W Byte	Y	Reg		Y	0x80
MFR_DISABLE_OUTPUT	0xFB	Disables regulator outputs until reset	R/W Byte	N	Reg			0x00
MFR_EE_USER_WP	0xFC	Disables commands that write user NVM	R/W Byte	N	Reg		Y	0x00
MFR_RESET	0xFD	Commanded reset without requiring a power down.	Send Byte	N				

Note 1: Commands indicated with Y in the EEPROM column indicate that these commands are stored and restored using the STORE_USER_ALL and RESTORE_USER_ALL commands, respectively.

Note 2: Commands with a default value of NA indicate “not applicable”. Commands with a default value of FS indicate “factory set on a per part basis”.

Note 3: The LT7182S contains additional reserved commands not listed in this table. Reading these commands is harmless to the operation of the IC; however, the contents and meaning of these commands can change without notice.

Note 4: Some of the unpublished commands are read-only and will generate a CML bit 6 fault if written.

Note 5: Writing to commands not published in this table is not permitted.

Note 6: The user should not assume compatibility of commands between different parts based upon command names. Always refer to the manufacturer’s data sheet for each part for a complete definition of a command’s function. ADI strives to keep command functionality compatible between all ADI devices, but differences may be introduced to address specific product requirements.

PMBus COMMAND SUMMARY

Table 2. Abbreviations of Supported Data Formats

	PMBus			
	TERMINOLOGY	**SPECIFICATION REFERENCE**	**DEFINITION**	**EXAMPLE**
L11	Linear11	Rev 1.3.1 Part II 7.3	Floating point 16-bit data: *value = Y • 2^N*, where *N* = b[15:11] and *Y* = b[10:0], both two's compliment binary integers.	b[15:0] = 0x9807 = 7 • 2^{-13} = 8.54 • 10^4
UL16	ULinear16	Rev 1.3.1 Part II 8.4.1.1	Fixed point 16-bit data: *value = Y • 2^−12*, where *Y* = b[15:0], an unsigned integer.	b[15:0] = 0x4C00 = 19456 • 2^{-12} = 4.75
Reg			Per-bit meaning defined in each command description.	PMBus STATUS_BYTE command.
IEEE	IEEE-754 Half Precision Floating Point	Rev 1.3.1 Part II 8.4.4	Floating point 16-bit data: for normal values, $value = (-1)^S \bullet 2^{N-15} \bullet \left(1+\frac{M}{1024}\right)$ where S = b[15], N = b[14:10], M = b[9:0].	$b[15:0] = 0x4580 = (-1)^0 \bullet 2^{17-15} \bullet \left(1+\frac{384}{1024}\right) = 5.5$

PMBus COMMAND DETAILS

ADDRESSING AND WRITE PROTECT

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
PAGE	0x00	Channel (page) selected for any paged command.	R/W Byte	N			0x00
PAGE_PLUS_WRITE	0x05	Write a command directly to a specified page.	W Block	N			
PAGE_PLUS_READ	0x06	Read a command directly from a specified page.	Block R/W Process	N			
ZONE_CONFIG	0x07	Specify zone number for selected page.	R/W Word	Y		Y	0xFEFE
ZONE_ACTIVE	0x08	Sets active zone number.	R/W Word	N			0xFEFE
WRITE_PROTECT	0x10	Protect the device from unintended PMBus modifications.	R/W Byte	N		Y	0x00
MFR_ADDRESS	0xE6	Specify right-justified 7-bit device address.	R/W Byte	N		Y	0x4F
MFR_RAIL_ADDRESS	0xFA	Specify right-justified 7-bit address for channels comprising a PolyPhase output.	R/W Byte	Y		Y	0x80

PMBus COMMAND DETAILS

PAGE

The PAGE command provides the ability to configure, control and monitor both channels through only one physical address, either the device address or global address 0x5B (7-bit address). Each PAGE contains the operating commands for one channel.

Pages 0x00 and 0x01 correspond to channel 0 and channel 1, respectively, in this device.

Setting PAGE to 0xFF applies any following paged commands to both outputs. With PAGE set to 0xFF, the device will respond to read commands as if PAGE were set to 0x00 (channel 0 results).

PAGE_PLUS_WRITE

The PAGE_PLUS_WRITE command provides a way to select the page within a device, send a command and then send the data for the command, all in one communication packet. Commands allowed by the present write protection level may be sent with PAGE_PLUS_WRITE.

The value stored in the PAGE command is not affected by PAGE_PLUS_WRITE. If PAGE_PLUS_WRITE is used to send a non-paged command, the Page Number byte is ignored.

> **Note:** PAGE_PLUS commands cannot be nested. A PAGE_PLUS command cannot be used to read or write another PAGE_PLUS command. If this is attempted, the device will NACK the entire PAGE_PLUS packet and issue a CML fault for Invalid/Unsupported Data.

The PAGE_PLUS_WRITE command cannot be used to write the PAGE command.

If the PAGE_PLUS_WRITE command is sent during a ZONE_WRITE, the page field will be used as the effective ZONE. The page field will override the write zone of ZONE_ACTIVE for this PAGE_PLUS_WRITE only.

PAGE_PLUS_READ

The PAGE_PLUS_READ command provides the ability to select the page within a device, send a command and then read the data returned by the command, all in one communication packet.

The value stored in the PAGE command is not affected by PAGE_PLUS_READ. If PAGE_PLUS_READ is used to access data from a non-paged command, the Page Number byte is ignored.

> **Note:** PAGE_PLUS commands cannot be nested. A PAGE_PLUS command cannot be used to read or write another PAGE_PLUS command. If this is attempted, the device will NACK the entire PAGE_PLUS packet and issue a CML fault for Invalid/Unsupported Data.

The PAGE_PLUS_READ command cannot be used to read the PAGE command.

PMBus COMMAND DETAILS

ZONE_CONFIG

The ZONE_CONFIG command is used to assign the currently selected channel to a specific zone number for ZONE_WRITE operations. Zone configuration only needs to be performed once, but zone numbers may be changed at any time.

A channel's zone may be assigned to any zone number between 0x00 and 0x7F. It may also be set to 0xFE, which means "No Zone". Any channel programmed to "No Zone" will ignore ZONE_WRITE operations.

The ZONE_CONFIG command uses the SMBus word write and word read protocols.

Table 3. ZONE_CONFIG Contents

BITS	MEANING
15-8	Must be 0xFE
7-0	Assigned zone

ZONE_ACTIVE

The ZONE_ACTIVE command sets the active zone for ZONE_WRITE operations. When a ZONE_WRITE is sent by the bus controller, the active zone controls which channels are affected by that write.

The active zone may be set to any zone number between 0x00 and 0x7F. The active zone may also be set to 0xFF, which means "All Zone". If a ZONE_WRITE is sent while the active zone is set to "All Zone", any channel not programmed to "No Zone" via ZONE_CONFIG will be affected by that write.

The ZONE_ACTIVE command must be sent using the ZONE_WRITE address (0x37) as a ZONE_WRITE operation. If the ZONE_ACTIVE command is sent to the global, device, or rail addresses, the invalid command bit will be set in STATUS_CML.

Table 4. ZONE_ACTIVE Contents

BITS	MEANING
15:8	Must be 0xFE
7:0	Active zone

PMBus COMMAND DETAILS

WRITE_PROTECT

The WRITE_PROTECT command is used to control writing to the device. This command does not indicate the status of the WP pin which is defined in the MFR_COMMON command. The WP pin takes precedence over the value of this command.

If the WP pin is high, only the PAGE, OPERATION, MFR_EE_UNLOCK and CLEAR_FAULTS commands are writable. individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.

When WRITE_PROTECT is set to 0x00, writes to all commands are enabled.

PAGE_PLUS_WRITE may be used to write any command that is not write protected. PAGE_PLUS_READ may be used to read any command.

BYTE	MEANING
0x80	Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK and STORE_USER_ALL command.
0x40	Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, STORE_USER_ALL, OPERATION and CLEAR_FAULTS command. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS registers.
0x20	Disable all writes except to the WRITE_PROTECT, OPERATION, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, CLEAR_FAULTS, PAGE, ON_OFF_CONFIG, VOUT_COMMAND and STORE_USER_ ALL. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS registers.
0x10	Reserved, must be 0.
0x08	Reserved, must be 0.
0x04	Reserved, must be 0.
0x02	Reserved, must be 0.
0x01	Reserved, must be 0.

MFR_ADDRESS

The MFR_ADDRESS command byte and the ASEL pin set the 7 bits of the PMBus device address.

Setting this command to a value of 0x80 disables device addressing. The GLOBAL device address, 0x5A and 0x5B, cannot be deactivated. If the ASEL pin is floating or connected to V_{DD18}, the device will use the full MFR_ADDRESS value. If a resistor is connected to the ASEL pin according to the table below, the four LSBs of the device address will be determined by the ASEL resistor value.

Reading MFR_ADDRESS always returns the value loaded from EEPROM or written via PMBus write. The value read from MFR_ADDRESS is not affected by the ASEL pin.

PMBus COMMAND DETAILS

LT7182S does not ignore ASEL, even when bit 6 of MFR_CONFIG_ALL_LT7182S is set to ignore the other resistor configuration pins. The three MSBs 6:4 of the device address are always determined by bits 6:4 of MFR_ADDRESS.

ASEL RESISTOR VALUE (±1%)	VALUE OF PMBus DEVICE ADDRESS LSBs 3:0
Floating or V_{DD18}	EEPROM value of MFR_ADDRESS
124kΩ	0xF
107kΩ	0xE
93.1kΩ	0xD
80.6kΩ	0xC
69.8kΩ	0xB
60.4kΩ	0xA
51.1kΩ	0x9
43.2kΩ	0x8
36.5kΩ	0x7
30.9kΩ	0x6
25.5kΩ	0x5
21.0kΩ	0x4
16.5kΩ	0x3
11.8kΩ	0x2
6.65kΩ	0x1
0Ω (Grounded)	0x0

Table 5. Illegal Addresses

ADDRESS	USE
0x0C	ARA protocol address
0x37	Zone write
0x5A	Global all rail address
0x5B	Global address

Attempting to set this command to illegal values will set a CML invalid data fault. The current value of ASEL will be considered for this error check. During power on, if the MFR_ADDRESS read from NVM and the current value of ASEL make an illegal address, the address will be set to 0x7C.

After changing the device address, leave at least 10µs for the new address to take effect before starting a new PMBus transaction.

The device will always respond to the global addresses 0x5A and 0x5B. Writes to address 0x5A will affect all pages, and reads will target page 0, as if PAGE == 0xFF.

PMBus COMMAND DETAILS

MFR_RAIL_ADDRESS

The MFR_RAIL_ADDRESS command enables direct device address access to the currently selected channel. Writing this command sets the rail address for the currently selected channel. The value of this command should be common to all devices attached to a single power supply rail.

Setting this command to a value of 0x80 disables rail device addressing for the selected channel.

Attempting to set MFR_RAIL_ADDRESS to an illegal address, as defined above in MFR_ADDRESS, will set a CML invalid data fault.

Writing PAGE_PLUS_READ or PAGE_PLUS_WRITE commands to the rail address will set a CML invalid command fault.

Reading from the rail address will result in a CML other fault.

After changing the a rail address, leave at least 10µs for the new address to take effect before starting a new PMBus transaction.

GENERAL CONFIGURATION

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
MFR_CHAN_CONFIG_LT7182S	0xD0	Configuration bits that are channel specific.	R/W Word	Y		Y	Ch. 0: 0x00D7 Ch. 1: 0x0057
MFR_CONFIG_ALL_LT7182S	0xD1	Configuration bits common to all channels.	R/W Word	N		Y	0x0100

PMBus COMMAND DETAILS

MFR_CHAN_CONFIG_LT7182S

This command sets various global configuration bits.

Table 6. MFR_CHAN_CONFIG_LT7182S Contents

BITS	DEFAULT Ch 0	DEFAULT Ch 1	MEANING
15-11	00000	00000	Reserved
10	0	0	0 = PGOOD Pull down is disabled when VOUT_OV_FAULT_LIMIT is exceeded. 1 = PGOOD Pull down remains active when VOUT_OV_FAULT_LIMIT is exceeded.
9	0	0	0 = PGOOD Pull down is disabled during output transitions. 1 = PGOOD Pull down is enabled during output transitions.
8	0	0	0 = Default single phase application or polyphase leader operation. 1 = Polyphase follower mode. All but one channel in polyphase applications should be set to follower mode. Internal compensation cannot be used in polyphase operation. The channel operates in forced continuous conduction mode.
7	1	0	0 = Device will not pull SHARE_CLK down due to PVIN voltage level. 1 = Enable SHARE_CLK pull-down until PVIN exceeds VIN_ON, or if PVIN falls below VIN_OFF.
6	1	1	0 = 250Ω output pull-down is disabled. 1 = 250Ω output pull-down is enabled when off and during TOFF_FALL.
5	0	0	0 = $\overline{\text{FAULT}}$ pin will be logged as a subevent when externally pulled low. 1 = $\overline{\text{FAULT}}$ pin will be logged as an event when externally pulled low.
4	1	1	0 = RUN will pulse low when OPERATION is written to turn off the channel. 1 = RUN will not pulse low when OPERATION is written to turn off the channel.
3	0	0	0 = Disable detection of channel disabled for insufficient time to complete shutdown sequence. 1 = Enable detection of channel disabled for insufficient time to complete shutdown sequence. See note 2 below.
2	1	1	0 = Channel output is remains active if SHARE_CLK is held low. 1 = Channel output is disabled if SHARE_CLK is held low.
1	1	1	0 = If $\overline{\text{FAULT}}$ pin is externally asserted, it will be logged and STATUS_MFR_SPECIFIC bit 0 will be set 1 = If FAULT# pin is externally asserted, it will not be logged and STATUS_MFR_SPECIFIC bit 0 will not be set. As a consequence, the $\overline{\text{ALERT}}$ pin is also not asserted due to $\overline{\text{FAULT}}$ pin external assertion.
0	1	1	0 = VOUT must be below MFR_DISCHARGE_THRESHOLD for the device to allow the channels to be enabled. 1 = Output may be enabled, regardless of VOUT.

Note 1: (bit 4). When this bit is cleared to a 0, the RUN pin will be pulled down whenever the channel is commanded off with the OPERATION command for a duration set by MFR_RESTART_DELAY.

Note 2: (bit 3). A Short Shutdown Cycle event occurs whenever the channel is turned off and commanded back on before the TOFF_DELAY plus TOFF_FALL time has elapsed. If a Short Shutdown Cycle event occurs and bit 3 of MFR_CHAN_CONFIG_LT7182S is set to a 1, the output rail will stop delivering power immediately and restart with a 20µs delay. If the Short Shutdown Cycle event occurs and this bit is set to a 0, the TOFF_DELAY plus TOFF_FALL times will be honored as a normal sequence off event, and the part will restart after an additional 20µs delay.

Note 3: (bit 8) When bit 6 of MFR_CONFIG_ALL_LT7182S is 0, configuration resistors may override the stored NVM value for this bit at power-up.

PMBus COMMAND DETAILS

MFR_CONFIG_ALL_LT7182S

This command sets various global configuration bits.

Table 7. MFR_CONFIG_ALL_LT7182S Contents

BITS	DEFAULT	MEANING
15-9	0000000	Reserved
8	1	0 = Linear11 and ULinear16 formats selected, depending on the command. 1 = IEEE half-precision floating point format selected.
7	0	0 = Fault log is disabled1 = Fault log is enabled
6	0	0 = Configuration resistors will be measured and used to configure the device during initialization1 = CFG pin configuration resistors will be ignored on pins VOUT0_CFG, VOUT1_CFG/POLYPHASE_CONFIG, and SYNC/PWM_CFG. Note that ASEL cannot be ignored and is always measured during initialization and used for device address (see MFR_ADDRESS).
5	0	0 = Enable CML fault for quick command read message. See note 1 below. 1 = Disable CML fault for quick command read message.
4	0	Reserved
3	0	Reserved
2	0	0 = Valid PEC not required1 = Valid PEC required
1	0	0 = Disable PMBus clock stretching. If device is too busy to process a command, the device will NACK the command and set bit 7 in STATUS_BYTE and STATUS_WORD1 = Enable PMBus clock stretching.
0	0	0 = When a channel is enabled, only the status bits affecting that channel will be cleared, including global status bits 1 = All fault and warning status bits will be cleared with either channel is enabled.

Note 1: (bit 5). The PMBus specification indicates that PMBus devices should indicate a fault has occurred if a command starts with the read bit set in the address byte. When bit 5 of MFR_CONFIG_ALL_LT7182S is set, this device will not indicate a fault.

Table 8. On, Off and Margin

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
OPERATION	0x01	Operating mode control. On/off, margin high and margin low.	R/W Byte	Y		Y	0x80
ON_OFF_CONFIG	0x02	RUN pin and PMBus OPERATION command configuration.	R/W Byte	Y		Y	0x1E
MFR_RESET	0xFD	Commanded reset.	Send Byte	N			

PMBus COMMAND DETAILS

OPERATION

The OPERATION command is used to turn the channels on or off in conjunction with the RUN pins, based on the configuration defined in ON_OFF_CONFIG. It is also used to set the output voltage to VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW.

Disabling and then reenabling a channel will cause all latched faults and status bits to be cleared for that channel. Overtemperature and internal reference faults are shared between both channels. Disabling and then reenabling either channel will clear the latched condition for overtemperature and internal reference faults for both channels.

The table below shows the values of OPERATION supported by the LT7182S.

FUNCTION	VALUE
Turn off immediately	0x00
Turn on	0x80
Margin low	0x98
Margin high	0xA8
Sequence off	0x40

ON_OFF_CONFIG

The ON_OFF_CONFIG command configures the combination of RUN pin input and serial bus commands required to turn the channel on and off.

The only bits allowed to be changed are as follows:

3: When high, the channel will only provide output power if the on/off portion of OPERATION is set.

2: When high, the channel will only provide output power if the corresponding RUN pin is high.

0: When high, the channel will perform an immediate shutdown when the RUN pin is de-asserted. Bit 0 only has an effect when bit 2 is also set.

Bits 4 and 1 must both be 1. Setting bits 4 or 1 to 0 will generate a CML fault.

If ON_OFF_CONFIG bits 2 and 3 are both set to 1 (which is the factory default), the channel will only turn on if the RUN pin is high and the OPERATION command is set to enable (on, margin low, or margin high).

PMBus COMMAND DETAILS

MFR_RESET

Causes the device to reset.

PWM CONFIGURATION

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
FREQUENCY_SWITCH	0x33	Controller switching frequency	R/W Word	N	kHz	Y	1000.0
MFR_PWM_MODE_LT7182S	0xD4	Paged PWM config, including PWM mode	R/W Word	Y		Y	0x1DD4
MFR_PWM_PHASE_LT7182S	0xF5	Set PWM phase	R/W Word	Y	Degrees	Y	Ch. 0: 0.0 Ch 1: 180.0
MFR_SYNC_CONFIG_LT7182S	0xF6	SYNC pin config for all pages	R/W Byte	N		Y	0x00

FREQUENCY_SWITCH

The FREQUENCY_SWITCH command selects the internal oscillator frequency in 100kHz steps. The valid range is 400kHz to 4MHz. The FREQUENCY_SWITCH value must be a multiple of 100kHz.

Regardless of the value of FREQUENCY_SWITCH, if external clock is present on the SYNC/PWM_CFG pin, the LT7182S will attempt to synchronize the PWM to the external clock, unless bit 1 or 0 in MFR_SYNC_CONFIG_LT7182S is set. If an external clock is to be used for synchronization, it is recommended to program FREQUENCY_SWITCH to the same frequency as the external clock.

This command has two data bytes encoded in either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

MFR_PWM_MODE_LT7182S

Table 9. MFR_PWM_MODE_LT7182S Contents

BITS	DEFAULT	MEANING		
15:14	0b00	Must be 0.		
13:11	0b011	Error Amplifier Transconductance (GMEA)		
		Value	Standard Mode (MFR_PWM_MODE_LT7182S Bit 1 Set to 0)	High-Performance Low-V_{OUT} Mode (MFR_PWM_MODE_LT7182S Bit 1 Set to 1)
		7	300µS	1.2mS
		6	262.5µS	1.05mS
		5	225µS	900µS
		4	187.5µS	750µS
		3	150µS	600µS
		2	112.5µS	450µS
		1	75µS	300µS
		0	37.5µS	150µS

PMBus COMMAND DETAILS

MFR_PWM_MODE_LT7182S

Table 9. MFR_PWM_MODE_LT7182S Contents

BITS	DEFAULT	MEANING		
10:9	0b10	I_{LIM} Range (Current Limit Selection)		
		Value	**Positive Valley Current Limit $I_{LIM-POS}$ (Typ)**	**Negative Valley Current Limit $I_{LIM-NEG}$ (Typ)**
		3	8.5A	–4.25A
		2	6.5A	–4A
		1	4.5A	–3.4A
		0	3.0A	–2.3A
8:6	0b111	Internal Compensation Capacitor Value C_{ITH}		
		Value	**C_{ITH} Capacitor Value**	
		7	80pF	
		6	70pF	
		5	60pF	
		4	50pF	
		3	40pF	
		2	30pF	
		1	20pF	
		0	10pF	
5:3	0b010	Internal compensation lead resistor value R_{ITH}		
		Value	**R_{ITH} Resistor Value**	
		7	120kΩ	
		6	100kΩ	
		5	80kΩ	
		4	60kΩ	
		3	40kΩ	
		2	20kΩ	
		1	10kΩ	
		0	5kΩ	
2	1	0 = Bit 0 will be used during TOFF_FALL. 1 = Use forced continuous mode during TOFF_FALL regardless of the value of bit 0.		
1	0	0 = Disable high-performance, low-V_{OUT} mode. Full V_{OUT} range available. 1 = Enable high-performance, low-V_{OUT} mode. V_{OUT} limited to 1.375. Maximizes transient response and DC accuracy.		
0	0	0 = Channel operates in forced continuous conduction mode when the output is in regulation at the commanded output voltage, and during TOFF_FALL. 1 = Pulse-skipping mode is enabled.		

PMBus COMMAND DETAILS

When high-performance, low-V_{OUT} mode is enabled, any of VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, or VOUT_MAX that is above 1.375 is set to 1.375. In this mode, attempts to write any of those commands above 1.375 will cause an invalid data CML fault.

When bit 6 of MFR_CONFIG_ALL_LT7182S is 0, configuration resistors may override stored NVM values for this command at power-up.

MFR_PWM_PHASE_LT7182S

The MFR_PWM_PHASE_LT7182S command sets the channel PWM phase in degrees. The value is internally rounded to the nearest 15°. Inputs that round to 360° or greater will cause an invalid data CML fault.

When bit 6 of MFR_CONFIG_ALL_LT7182S is 0, configuration resistors may override stored NVM values for this command at power-up.

MFR_SYNC_CONFIG_LT7182S

Table 10. MFR_SYNC_CONFIG_LT7182S Contents

BITS	DEFAULT	MEANING
7:2	000000	Must be 0.
1	0	0 = SYNC clock input is used. 1 = Ignore SYNC/PWM_CFG clock input. Note that the SYNC/PWM_CFG clock input is always ignored if SYNC output is enabled (bit 0 high). Note that even if bit 1 is set, an external clock on SYNC/PWM_CFG may not be ignored during POR: if an external clock is applied to SYNC/PWM_CFG at POR and the configuration resistor function has not been disabled (that is, bit 6 of the MFR_CONFIG_ALL_LT7182S command is set to its factory-default value of 0 in EEPROM), the LT7182S will configure internal settings as described in the Operation section of the data sheet.
0	0	0 = Disable SYNC output clock1 = Enable SYNC output clock (will run whenever SHARE_CLK is active).

When bit 6 of MFR_CONFIG_ALL_LT7182S is 0, configuration resistors may override stored NVM values for this command at power-up.

INPUT VOLTAGE AND LIMITS

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
VIN_ON	0x35	Input voltage at which channel starts power conversion.	R/W Word	Y	V	Y	Ch. 0: 1.5 Ch. 1: 1.4
VIN_OFF	0x36	Input voltage at which channel stops power conversion.	R/W Word	Y	V	Y	Ch. 0: 1.45 Ch. 1: 1.35
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	Y	V	Y	–1.0

VIN_ON

The VIN_ON command sets the value of the input voltage, in Volts, at which the unit starts power conversion.

Note: The LT7182S regulators will not start unless the internal $INTV_{CC}$ and DRV_{CC} supplies are at least 2.8V, which requires that either $EXTV_{CC}$ or PV_{IN0} be at least 2.9V.

PMBus COMMAND DETAILS

This command has two data bytes encoded in either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

Max 20.0V

Min 1.4V

VIN_OFF

This command sets the value of the input voltage, in Volts, at which the unit should stop power conversion.

This command has two data bytes encoded in either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

Max 20.0V

Min 1.35V

VIN_UV_WARN_LIMIT

The VIN_UV_WARN_LIMIT command sets the value of the input voltage that causes an input voltage low warning.

This alarm is masked until the input exceeds the warning limit at least one time since the LT7182S has been powered.

In response to the VIN_UV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the INPUT bit in the STATUS_WORD
- Sets the V_{IN} UV Warning bit in the STATUS_INPUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin low, unless masked

This command has two data bytes encoded in either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

This condition is detected by the ADC. Typical response time is less than 6.75ms in continuous monitor mode and is less than 100ms in low power mode. Note that this response delay may occur even when the previous ADC measurement is under the new VIN_UV_WARN_LIMIT.

Max 22.0V

Min –1.0V

PMBus COMMAND DETAILS

OUTPUT VOLTAGE AND LIMITS

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
VOUT_MODE	0x20	Output voltage format and exponent.	R Byte	Y			0x60
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	V	Y	0.5
VOUT_MAX	0x24	Upper limit on the commanded output voltage.	R/W Word	Y	V	Y	0.537
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point.	R/W Word	Y	V	Y	0.525
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point.	R/W Word	Y	V	Y	0.475
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	V	Y	0.55
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	V	Y	0.537
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	V	Y	0.467
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	V	Y	0.465
MFR_DISCHARGE_THRESHOLD	0xE4	Voltage threshold that determines output has decayed sufficiently.	R/W Word	Y	V	Y	0.2
MFR_PGOOD_DELAY	0xF2	Time output voltage must be between UV and OV before PGOOD transitions high.	R/W Word	Y	ms	Y	1.0
MFR_NOT_PGOOD_DELAY	0xF3	Time output voltage must be below UV or above OV before PGOOD transitions low.	R/W Word	Y	ms	Y	0.1

VOUT_MODE

The read-only VOUT_MODE command contains a 3-bit mode and a 5-bit parameter that describe the numerical format used by output voltage commands. VOUT_MODE will be one of two values. 0x60 indicates IEEE half-precision floating point format. 0x14 indicates unsigned linear 16 format with a fixed exponent of 2^{-12}.

VOUT_COMMAND

This command sets the output voltage when the OPERATION command has selected VOUT_COMMAND, and uses either ULinear16 or half-precision floating point format as selected by MFR_CONFIG_ALL_LT7182S bit 8.

If OPERATION is set to 0x80 (turn on the output with target voltage of VOUT_COMMAND) and VOUT_COMMAND is a greater than VOUT_MAX, the target output voltage will be limited to VOUT_MAX. When VOUT_COMMAND is commanded to a value greater than VOUT_MAX, a VOUT_MAX warning will occur.

When bit 6 of MFR_CONFIG_ALL_LT7182S is 0, configuration resistors may override stored NVM values for this command at power-up.

Max 5.5V

Min 0.4V

PMBus COMMAND DETAILS

VOUT_MAX

The VOUT_MAX command sets an upper limit on the commanded voltage. It applies to VOUT_COMMAND, VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW. If the output voltage is commanded to a value greater than VOUT_MAX, the target output voltage will be limited to VOUT_MAX. When VOUT_MAX is lower than VOUT_COMMAND, VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW, a VOUT_MAX warning will occur.

This command uses either ULinear16 or half-precision floating point format as selected by MFR_CONFIG_ALL_LT7182S bit 8.

When bit 6 of MFR_CONFIG_ALL_LT7182S is 0, configuration resistors may override stored NVM values for this command at power-up.

Max 5.5V

Min 0.4V

VOUT_MARGIN_HIGH

This command loads the unit with the voltage to which the output is to be regulated when the OPERATION command is set to 0xA8 (Margin High). When OPERATION is set to 0xA8 and VOUT_MARGIN_HIGH is greater than VOUT_MAX, the output voltage will be limited to VOUT_MAX. When VOUT_MARGIN_HIGH is commanded to a value greater than VOUT_MAX, the a VOUT_MAX warning will occur.

This command uses either ULinear16 or half-precision floating point format as selected by MFR_CONFIG_ALL_LT7182S bit 8.

When bit 6 of MFR_CONFIG_ALL_LT7182S is 0, configuration resistors may override stored NVM values for this command at power-up.

Max 5.5V

Min 0.4V

VOUT_MARGIN_LOW

This command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to 0x98 (Margin Low). When OPERATION is set to 0x98 (Margin Low) and VOUT_MARGIN_LOW is greater than VOUT_MAX, the output voltage will be VOUT_MAX. When VOUT_MARGIN_LOW is commanded to a value greater than VOUT_MAX, the VOUT_MAX Warning bit in VOUT_STATUS will be set.

This command uses either ULinear16 or half-precision floating point format as selected by MFR_CONFIG_ALL_LT7182S bit 8.

When bit 6 of MFR_CONFIG_ALL_LT7182S is 0, configuration resistors may override stored NVM values for this command at power-up.

Max 5.5V

Min 0.4V

PMBus COMMAND DETAILS

VOUT_OV_FAULT_LIMIT

This command sets the value of the output voltage measured at the VSENSE pins which causes an output overvoltage fault.

This command uses either ULinear16 or half-precision floating point format as selected by MFR_CONFIG_ALL_LT7182S bit 8.

The value must be greater than VOUT_UV_WARN_LIMIT, VOUT_UV_FAULT_LIMIT and MFR_DISCHARGE_THRESHOLD, or an invalid data error will occur.

When bit 6 of MFR_CHAN_CONFIG_LT7182S is 0, configuration resistors may override stored NVM values for this command at power-up.

Max 6.0V

Min 0.4V

VOUT_OV_WARN_LIMIT

This command sets the value of the output voltage measured at the VSENSE pins which causes and output overvoltage warning.

In response to the VOUT_OV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT OV Warning bit in the STATUS_VOUT command
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin low, unless masked

This command uses either ULinear16 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

The value must be greater than VOUT_UV_WARN_LIMIT, VOUT_UV_FAULT_LIMIT and MFR_DISCHARGE_THRESHOLD, or an invalid data error will occur.

When bit 6 of MFR_CHAN_CONFIG_LT7182S is 0, configuration resistors may override stored NVM values for this command at power-up.

Max 6.0V

Min 0.0V

PMBus COMMAND DETAILS

VOUT_UV_WARN_LIMIT

This command sets the value of the output voltage measured at the VSENSE pins which causes and output undervoltage warning.

In response to the VOUT_UV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT UV Warning bit in the STATUS_VOUT command
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin low, unless masked

This command uses either ULinear16 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

The value must be less than VOUT_OV_WARN_LIMIT and VOUT_OV_FAULT_LIMIT, or an invalid data error will occur.

When bit 6 of MFR_CONFIG_ALL_LT7182S is 0, configuration resistors may override stored NVM values for this command at power-up.

Max 5.5V

Min 0.0V

VOUT_UV_FAULT_LIMIT

This command sets the value of the output voltage measured at the VSENSE pins which causes an output undervoltage fault.

This command uses either ULinear16 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

The value must be less than VOUT_OV_WARN_LIMIT and VOUT_OV_FAULT_LIMIT, or an invalid data error will occur.

When bit 6 of MFR_CONFIG_ALL_LT7182S is 0, configuration resistors may override stored NVM values for this command at power-up.

Max 5.5V

Min 0.36V

PMBus COMMAND DETAILS

MFR_DISCHARGE_THRESHOLD

The MFR_DISCHARGE_THRESHOLD command specifies the output voltage threshold below which the output voltage must decay in order to enable the channel if the discharge threshold feature is enabled (bit 0 of MFR_CHAN_CONFIG_LT7182S is 0). If the discharge threshold is enabled, and the discharge threshold is selected in MFR_FAULT_PROPAGATE_LT7182S, and the channel is commanded on while V_{OUT} is greater than the discharge threshold, the $\overline{FAULT}$ pin will be pulled low until V_{OUT} is below the discharge threshold.

If the discharge threshold is enabled, when automatically retrying after a fault, the device will also wait for V_{OUT} to be below the discharge threshold after waiting MFR_RETRY_DELAY.

The value must be less than VOUT_OV_WARN_LIMIT and VOUT_OV_FAULT_LIMIT, or an invalid data error will occur.

Max 6.0V

Min 0.1V

MFR_PGOOD_DELAY

The MFR_PGOOD_DELAY command sets the time in milliseconds, rounded to the nearest 10µs, that the output voltage must be between VOUT_OV_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT before the PGOOD pin will transition high. If the output voltage moves below the undervoltage limit or above the overvoltage limit before PGOOD transitions high, the delay timer will reset to zero. Note that PGOOD is always held low when the channel is off and during TON_RISE, regardless of whether V_{OUT} is within the limits.

Max 64000ms

Min 0ms

MFR_NOT_PGOOD_DELAY

The MFR_NOT_PGOOD_DELAY command sets the time in milliseconds, rounded to the nearest 10µs, that the output voltage must be between VOUT_OV_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT before the PGOOD pin will be pulled low. If the output voltage is between the undervoltage and overvoltage limits before PGOOD transitions low, the delay timer will reset to zero. Note that this command only applies when the channel is enabled; if the channel is disabled by command, RUN pin, or a fault condition set to disable the output, the PGOOD pin is pulled low immediately. If V_{OUT} is command to change voltage and MFR_CHAN_CONFIG_LT7182S bit 9 is set to 1, then PGOOD will also pull low without delay.

Max 100ms

Min 0ms

PMBus COMMAND DETAILS

INPUT CURRENT LIMITS

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
IIN_OC_WARN_LIMIT	0x5D	Sets the input overcurrent warning limit	R/W Word	Y	A	Y	8.0

IIN_OC_WARN_LIMIT

The IIN_OC_WARN_LIMIT command sets the value of the input current, in amperes, that causes a warning indicating the input current is high.

In response to the IIN_OC_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the INPUT bit in the upper byte of the STATUS_WORD
- Sets the IIN OC Warning bit in the STATUS_INPUT command
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin low, unless masked

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

This condition is detected by the ADC. Typical response time is less than 6.75ms in continuous monitor mode and is less than 100ms in reduced-power monitor mode.

Max 20A

Min 0.0A

OUTPUT CURRENT LIMITS

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
IOUT_OC_WARN_LIMIT	0x4A		R/W Word	Y	A	Y	8.0

IOUT_OC_WARN_LIMIT

This command sets the value of the output current that causes an output overcurrent warning in amperes.

In response to the IOUT_OC_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the IOUT bit in the STATUS_WORD
- Sets the IOUT OC Warning bit in the STATUS_IOUT command
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin low, unless masked

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

PMBus COMMAND DETAILS

This condition is detected by the ADC. Typical response time is less than 6.75ms in continuous monitor mode and is less than 100ms in low power mode.

The IOUT_OC_WARN_LIMIT is ignored during TON_RISE.

Max 20A

Min 0.0A

TEMPERATURE

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
OT_FAULT_LIMIT	0x4F	Overtemperature fault limit.	R/W Word		C	Y	160
OT_WARN_LIMIT	0x51	Overtemperature warning limit.	R/W Word		C	Y	140

OT_FAULT_LIMIT

The OT_FAULT_LIMIT command sets the value of the internal die temperature, in degrees Celsius, which causes an overtemperature fault.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

Max 160°C

Min –60°C

OT_WARN_LIMIT

The OT_WARN_LIMIT command sets the value of the internal die temperature, in degrees Celsius, which causes an overtemperature warning.

In response to the OT_WARN_LIMIT being exceeded, the device:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the OT Warning bit in the STATUS_TEMPERATURE command
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin low, unless masked

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

This condition is detected by the ADC. Typical response time is less than 20ms in continuous monitor mode and is less than 100ms in low power mode.

Max 160°C

Min –60°C

PMBus COMMAND DETAILS

TIMING

Sequencing On

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
VOUT_TRANSITION_RATE	0x27	Rate the output changes when commanded to a new value.	R/W Word	Y	V/ms	Y	0.25
TON_DELAY	0x60	Time from RUN or OPERATION on to output turn-on.	R/W Word	Y	ms	Y	0
TON_RISE	0x61	Time from output turn-on to reach the commanded value.	R/W Word	Y	ms	Y	1.0
TON_MAX_FAULT_LIMIT	0x62	Maximum time from start of TON_RISE for VOUT to cross VOUT_UV_FAULT_LIMIT.	R/W Word	Y	ms	Y	5.0

VOUT_TRANSITION_RATE

When a PMBus device receives either a VOUT_COMMAND, OPERATION, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, or VOUT_MAX command that causes the output voltage to change, VOUT_TRANSITION_RATE sets the rate (in V/ms) at which the output voltage changes. This commanded rate of change does not apply when the unit is commanded on or off.

Values of greater than 0.05V/ms are recommended.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

Max* 25V/ms

Min 0.01V/ms

Note: *While the VOUT_TRANSITION_RATE may be commanded up to 25V/ms, the actual achievable output voltage transition rate may be limited by other factors, including output capacitance, current limit, and compensation.

TON_DELAY

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received until the output voltage starts to rise. The time is internally rounded down to the nearest 10µs.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

Max 64000ms

Min 0s

PMBus COMMAND DETAILS

TON_RISE

The TON_RISE command sets the time, in milliseconds, from the time the output starts to rise to the time the output enters the regulation band. The time is internally rounded to the nearest 10µs. The channel is set to pulse-skipping mode during TON_RISE events. The maximum rise rate of the digital ramp controller is 25V/ms—if the commanded output voltage divided by TON_RISE is more than 25V/ms, the digital control will ramp at this rate. The minimum output voltage rise time may be further limited by analog behavior of the switcher, which is affected by several factors including output capacitance, current limit selection, and loop compensation.

When TON_RISE is commanded to change during TON ramp-up, the device will act on the command as soon as possible. However, the new ramp rate will be calculated for a full ramp from 0 Volts. Because the output is partially ramped and time has already passed, the actual total ramp time will differ from the new value for TON_RISE.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

Max 2000ms

Min 0s

TON_MAX_FAULT_LIMIT

The TON_MAX_FAULT_LIMIT command sets the value, in milliseconds, that determines how long the unit can attempt to power up the output without reaching the output undervoltage fault limit. The time is internally rounded down to the nearest 10µs. A data value of 0ms means that there is no limit and that the unit can attempt to bring up the output voltage indefinitely.

The TON_MAX_FAULT_LIMIT time is started after TON_DELAY has finished and a soft-start sequence is started. The resolution of the TON_MAX_FAULT_LIMIT is 10µs. If the VOUT_UV_FAULT_LIMIT is not reached within the TON_MAX_FAULT_LIMIT time, the response of this fault is determined by the value of the TON_MAX_FAULT_RESPONSE command value.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

Max 64000ms

Min (Disabled) 0s

Sequencing Off

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL	R/W Word	Y	ms	Y	0.0
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts	R/W Word	Y	ms	Y	2.0
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL completed, for output to decay below MFR_DISCHARGE_THRESHOLD	R/W Word	Y	ms	Y	0.0

PMBus COMMAND DETAILS

TOFF_DELAY

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received until the output voltage starts to fall. The time is internally rounded down to the nearest 10µs.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

Max 64000ms

Min 0ms

TOFF_FALL

The TOFF_FALL command sets the time, in milliseconds, from the end of the turn-off delay time until the output voltage is commanded to zero. The time is internally rounded to the nearest 10µs. It is the ramp time of the V_{OUT} DAC.

During V_{OUT} ramp-down, the part will use continuous conduction mode if either MFR_PWM_MODE_LT7182S bit 2 is set to 1, or MFR_PWM_MODE_LT7182S bit 0 is set to 0, otherwise V_{OUT} will decay only due to the external load (and the 250Ω internal pull-down if MFR_CHAN_CONFIG_LT7182S bit 6 is set to 1). For defined TOFF_FALL times, it is recommended to set MFR_PWM_MODE_LT7182S bit 2 to 1. The maximum fall rate of the digital ramp controller is 25V/ms—if the commanded output voltage divided by TOFF_FALL is more than 25V/ms, the digital control will ramp down at this rate. The minimum V_{OUT} fall time may be further limited by analog behavior of the switcher, which is affected by several factors including output load, output capacitance, PWM mode selection (forced continuous vs pulse-skipping), and current limit selection. After the digital ramp-down is completed, the switching regulator is disabled. If the V_{OUT} fall rate is limited by analog behavior, then the regulator will become disabled before the ramp-down is complete, and the output will not be forced all the way to zero. Setting TOFF_FALL to 2ms or greater will ensure that V_{OUT} will be ramped to zero during TOFF_FALL.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

Max 2000ms

Min 0ms

TOFF_MAX_WARN_LIMIT

The TOFF_MAX_WARN_LIMIT command sets the value, in milliseconds, that determines how long the unit can attempt to turn off the output until a warning is asserted. The time is internally rounded to the nearest 1ms. The output is considered off when the V_{OUT} voltage is less than MFR_DISCHARGE_THRESHOLD. The calculation begins after TOFF_FALL is complete. TOFF_MAX_WARN is not enabled if the discharge requirement is disabled (bit 0 of MFR_CHAN_CONFIG_LT7182S set to 1).

PMBus COMMAND DETAILS

In response to the TOFF_MAX_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the TOFF_MAX_Warning bit in the STATUS_VOUT command
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin low, unless masked

The special data value of 0ms means that there is no limit and that the unit can attempt to turn off the output voltage indefinitely.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

For this warning, the V_{OUT} voltage is detected by the ADC. Typical response time is less than 6.75ms in continuous monitor mode and is less than 100ms in low power mode.

Max 64000ms

Min 10.0ms

Disabled 0.0ms

Restarting

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
MFR_RESTART_DELAY	0xDC	Minimum RUN pin off time	R/W Word	Y	ms	Y	10.0

MFR_RESTART_DELAY

This command specifies the minimum RUN off time in milliseconds. This device will pull the RUN pin low for this length of time once a falling edge of RUN has been detected. The time is internally rounded to the nearest 10µs. Note that the restart delay is different than the retry delay. The restart delay pulls run low for the specified time, after which a standard start-up sequence is initiated. While the minimum value for this command is 0.04ms, the minimum pull down time for the RUN pin is TOFF_DELAY + TOFF_FALL + 0.02ms. The output rail can be off longer than the MFR_RESTART_DELAY after the RUN pin is pulled high if the output decay bit 0 is not set in MFR_CHAN_CONFIG_LT7182S and the output takes a long time to decay below MFR_DISCHARGE_THRESHOLD.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

Max 64000ms

Min 0.04ms

PMBus COMMAND DETAILS

FAULT RESPONSE

All Faults

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
MFR_RETRY_DELAY	0xDB	Retry interval during fault retry	R/W Word	Y	ms	Y	10.0

MFR_RETRY_DELAY

This command sets the time in milliseconds between restarts if the fault response is to retry the controller at specified intervals. The time is internally rounded down to the nearest 10µs. This command value is used for all fault responses that require retry. The retry time starts once a fault has been detected by the offending channel. Note that the retry delay time is determined by the longer of the MFR_RETRY_DELAY command or the time required for the regulated output to decay below MFR_DISCHARGE_THRESHOLD. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR_RETRY_DELAY command by asserting bit 0 of MFR_CHAN_CONFIG_LT7182S.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

Max 64000ms

Min 0.02ms

Input Voltage

Input voltage faults only cause a configured fault response when the associated channel is on. Any associated $\overline{\text{FAULT}}$ pin will also only be asserted when the channel is on. However, the $\overline{\text{ALERT}}$ pin will be asserted low unless masked by SMBALERT_MASK.

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken when an input overvoltage fault is detected.	R/W Byte	Y		Y	0xB8

VIN_OV_FAULT_RESPONSE

The VIN_OV_FAULT_RESPONSE command sets the action the device will take in response to an input overvoltage fault.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the INPUT bit in the upper byte of the STATUS_WORD
- Sets the VIN OV Fault bit in the STATUS_INPUT command
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin low, unless masked

PMBus COMMAND DETAILS

Table 11. Data Byte Contents: VIN_OV_FAULT_RESPONSE

BITS	DESCRIPTION	DEFAULT	VALUE	MEANING
7:6	Response For all values of bits [7:6], the device: Sets the VIN OV bit in the status commands Pulls the $\overline{\text{ALERT}}$ pin low, unless masked	10	00	Not supported. Writing this value will generate a CML fault.
			01	Not supported. Writing this value will generate a CML fault.
			10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
			11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	111	000–110	The unit does not attempt to restart. The output remains disabled until the device is commanded off or bias power is removed by removing PV_{IN0} and $EXTV_{CC}$.
			111	The device attempts to restart continuously, without limitation, until it is commanded off (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000	000	Must be 0. Writing this to nonzero will generate a CML fault.

Output Voltage

Output voltage faults only cause a configured fault response when the associated channel is on. Any associated $\overline{\text{FAULT}}$ pin will also only be asserted when the channel is on. However, the $\overline{\text{ALERT}}$ pin will be asserted low unless masked by SMBALERT_MASK.

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken when an output overvoltage fault is detected	R/W Byte	Y		Y	0xB8
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken when an output undervoltage fault is detected	R/W Byte	Y		Y	0x00
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken when a TON_MAX_FAULT event is detected	R/W Byte	Y		Y	0x00

VOUT_OV_FAULT_RESPONSE

The VOUT_OV_FAULT_RESPONSE command sets the action the device will take in response to an output overvoltage fault.

The device also:

- Sets the VOUT_OV bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT OV Fault bit in the STATUS_VOUT command
- Sets the VOUT OV Warning bit in the STATUS_VOUT command
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin low, unless masked

PMBus COMMAND DETAILS

Table 12. Data Byte Contents: VOUT_OV_FAULT_RESPONSE

BITS	DESCRIPTION	DEFAULT	VALUE	MEANING
7:6	Response Default: 10 For all values of bits [7:6], the device: Sets the VOUT OV bit in the status commands Pulls the $\overline{\text{ALERT}}$ pin low, unless masked.	10	00	The device operates in continuous mode while the fault is active, attempting to regulate to the programmed voltage.
			01	The device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the device responds as programmed in the Retry Setting (bits [5:3]).
			10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
			11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting Default: 111	111	000–110	The unit does not attempt to restart. The output remains disabled until the device is commanded off or bias power is removed by removing PV_{IN0} and $EXTV_{CC}$.
			111	The device attempts to restart continuously, without limitation, until it is commanded off (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000		The delay time in 10µs increments. This delay time determines how long the channel continues operating after a fault is detected.

VOUT_UV_FAULT_RESPONSE

The VOUT_UV_FAULT_RESPONSE command sets the action the device will take in response to an output undervoltage fault.

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT UV Fault bit in the STATUS_VOUT command
- Sets the VOUT UV Warning bit in the STATUS_VOUT command
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin low, unless masked
- The UV fault and warn are masked until the following criteria are achieved:
- The TON_MAX_FAULT_LIMIT has been reached
- The TON_DELAY sequence has completed
- The TON_RISE sequence has completed
- The VOUT_UV_FAULT_LIMIT threshold has been reached
- The IOUT_OC_FAULT_LIMIT is not present

PMBus COMMAND DETAILS

The UV fault and warn are masked whenever the channel is not active.

The UV fault and warn are masked during TON_RISE and TOFF_FALL sequencing.

Table 13. Data Byte Contents: VOUT_UV_FAULT_RESPONSE

BITS	DESCRIPTION	DEFAULT	VALUE	MEANING
7:6	Response For all values of bits [7:6], the device: Sets the VOUT UV bit in the status commands Pulls the $\overline{\text{ALERT}}$ pin low, unless masked.	00	00	The device continues operation without interruption
			01	The device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the device responds as programmed in the Retry Setting (bits [5:3]).
			10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
			11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000	000–110	The unit does not attempt to restart. The output remains disabled until the device is commanded off or bias power is removed by removing PV_{IN0} and $EXTV_{CC}$.
			111	The device attempts to restart continuously, without limitation, until it is commanded off (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000	XXX	The delay time in 10µs increments. This delay time determines how long the channel continues operating after a fault is detected.

TON_MAX_FAULT_RESPONSE

The TON_MAX_FAULT_RESPONSE command sets the action the device will take in response to a TON_MAX fault.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the TON_MAX Fault bit in the STATUS_VOUT command
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin low, unless masked
- A value of 0 disables the TON_MAX_FAULT_RESPONSE. It is not recommended to use 0

PMBus COMMAND DETAILS

Table 14. Data Byte Contents: TON_MAX_FAULT_RESPONSE

BITS	DESCRIPTION	DEFAULT	VALUE	MEANING
7:6	Response For all values of bits [7:6], the device: Sets the TON_MAX bit in the status commands Pulls the $\overline{\text{ALERT}}$ pin low, unless masked.	00	00	The device continues operation without interruption.
			01	Not supported. Writing this value will generate a CML fault.
			10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
			11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000	000–110	The unit does not attempt to restart. The output remains disabled until the device is commanded off or bias power is removed by removing PV_{IN0} and $EXTV_{CC}$.
			111	The device attempts to restart continuously, without limitation, until it is commanded off (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000	XXX	Must be 0. Writing this to nonzero will generate a CML fault.

Output Current

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken when an output overcurrent fault is detected	R/W Byte	Y		Y	0x00

Table 15. Data Byte Contents: IOUT_OC_FAULT_RESPONSE

BITS	DESCRIPTION	DEFAULT	VALUE	MEANING
7:6	Response For all values of bits [7:6], the device: Sets the IOUT OC bit in the status commands Pulls the $\overline{\text{ALERT}}$ pin low, unless masked.	00	00	The device continues operation indefinitely while maintaining the output current set by MFR_PWM_MODE_LT7182S without regard to the output voltage (known as constant-current or brick wall limiting).
			01	Not supported. Writing this value will generate a CML fault.
			10	The device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the device responds as programmed in the Retry Setting (bits [5:3]).
			11	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
5:3	Retry Setting	000	000–110	The unit does not attempt to restart. The output remains disabled until the device is commanded off or bias power is removed by removing PV_{IN0} and $EXTV_{CC}$.
			111	The device attempts to restart continuously, without limitation, until it is commanded off (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000	XXX	The delay time in 10µs increments. This delay time determines how long the channel continues operating after a fault is detected.

PMBus COMMAND DETAILS

Temperature

Internal temperature faults only cause a configured fault response when the associated channel is on. Any associated $\overline{\text{FAULT}}$ pin will also only be asserted when the channel is on. However, the $\overline{\text{ALERT}}$ pin will be asserted low unless masked by SMBALERT_MASK.

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
OT_FAULT_RESPONSE	0x50	Action to be taken when an internal overtemperature fault is detected	R/W Byte			Y	0xC0

OT_FAULT_RESPONSE

The OT_FAULT_RESPONSE command sets the action the device will take in response to an internal overtemperature fault.

The device also:

- Sets the MFR bit in the STATUS_WORD
- Sets the OT Fault bit in the STATUS_TEMPERATURE command
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin low, unless masked

Table 16. Data Byte Contents: OT_FAULT_RESPONSE

BITS9	DESCRIPTION	DEFAULT	VALUE	MEANING
7:6	Response For all values of bits [7:6], the device: Sets the OT bit in the status commands Pulls the $\overline{\text{ALERT}}$ pin low, unless masked.	11	00	Not supported. Writing this value will generate a CML fault.
			01	Not supported. Writing this value will generate a CML fault.
			10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
			11	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	000–110	The unit does not attempt to restart. The output remains disabled until the device is commanded off or bias power is removed by removing PV_{IN0} and $EXTV_{CC}$.
			111	Not supported. Writing this value will generate a CML fault.
2:0	Ignored	000	XXX	Ignored

Fault Sharing

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
MFR_FAULT_PROPAGATE_LT7182S	0xD2	Determines which faults are propagated to the $\overline{\text{FAULT}}$ pin	R/W Word	Y		Y	0xE0D7
MFR_FAULT_RESPONSE	0xD5	Action to be taken when the $\overline{\text{FAULT}}$ pin is asserted low	R/W Byte	Y		Y	0xC0

PMBus COMMAND DETAILS

MFR_FAULT_PROPAGATE_LT7182S

The MFR_FAULT_PROPAGATE_LT7182S command selects the conditions that can cause the $\overline{\text{FAULT}}$ pin to be asserted low. When the $\overline{\text{FAULT}}$ pin is asserted low due to a fault condition, it will remain asserted until:

- The channel is disabled and then enabled (by RUN or OPERATION, depending on ON_OFF_CONFIG), clearing the fault condition
- MFR_RETRY_DELAY expires when the fault condition is no longer present for faults that are configured with a retry response

A fault is only propagated to the $\overline{\text{FAULT}}$ pin if the corresponding fault response command is configured to disable the channel and the corresponding bit is set to 1 in MFR_FAULT_PROPAGATE_LT7182S.

Table 17. MFR_FAULT_PROPAGATE_LT7182S Contents

BITS	DEFAULT	CONDITION	DESCRIPTION
15	1	V_{OUT} turned on while discharging	Enables propagation of the V_{OUT} discharge condition. This is used when bit 0 of MFR_CHAN_CONFIG_LT7182S is 0 (discharge requirement enabled). If V_{OUT} turned on while VSENSE is above MFR_DISCHARGE_THRESHOLD, VOUT will be disabled until VSENSE decays below that threshold.
14	1	Short Shutdown Cycle	Enables propagation of the Short Shutdown Cycle condition if bit 3 of MFR_CHAN_CONFIG_LT7182S is set.
13	1	TON max fault	
12	0	Reserved	
11:8	0	Reserved	
7	1	Overtemperature fault	
6	1	Internal voltage reference fault	
5	0	Reserved	
4	1	Input OV fault	
3	0	Reserved	
2	1	I_{OUT} OC fault	
1	1	V_{OUT} UV fault	
0	1	V_{OUT} OV fault	

MFR_FAULT_RESPONSE

This command determines the device's response to the $\overline{\text{FAULT}}$ pin being pulled low.

VALUE	MEANING
0xC0	The device will stop delivering power as fast as possible in response to the $\overline{\text{FAULT}}$ pin being pulled low
0x00	The device continues operation without interruption

PMBus COMMAND DETAILS

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the MFR bit in the STATUS_WORD
- Sets bit 0 in the STATUS_MFR_SPECIFIC command if bit 1 of MFR_CHAN_CONFIG_LT7182S is not set
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin low, unless masked. The the $\overline{\text{ALERT}}$ pin pulled low can be disabled by setting bit 0 of MFR_CHAN_CONFIG_LT7182S.

IDENTIFICATION

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
CAPABILITY	0x19	PMBus optional communication protocols supported.	R Byte	N			0xD8
PMBUS_REVISION	0x98	PMBus revision supported. Currently 1.3.	R Byte	N			0x33
MFR_ID	0x99	Returns “ADI”	R String	N			ADI
MFR_MODEL	0x9A	Returns “LT7182S”	R String	N			LT7182S
MFR_REVISION	0x9B	Manufacturer revision number	R Block	N			
MFR_SERIAL	0x9E	Unit-specific unique serial number	R Block	N			
IC_DEVICE_ID	0xAD	Returns “LT7182S”	R Block	N			LT7182S
IC_DEVICE_REV	0xAE	Manufacturer revision number	R Block	N			
MFR_SPECIAL_ID	0xE7	Manufacturer code	R Word	N			0x1C1D

STATUS

Figure 1 summarizes the internal LT7182S status registers accessible by PMBus command. These contain indication of various faults, warnings and other important operating conditions. As shown, the STATUS_BYTE and STATUS_WORD commands summarize contents of other status registers.

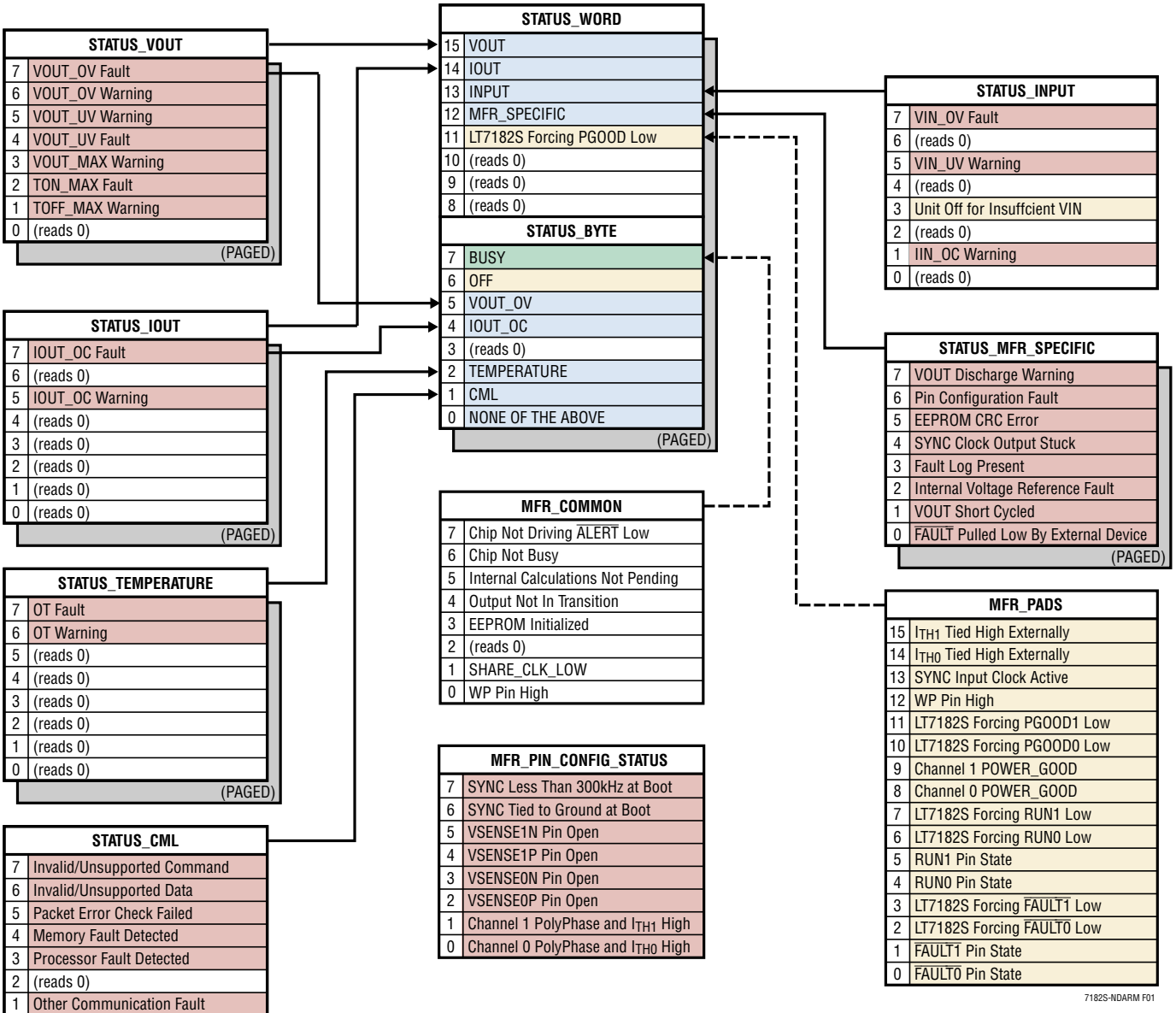
The NONE_OF_THE_ABOVE bit in STATUS_BYTE indicates that one or more of the bits in the most-significant nibble of STATUS_WORD are also set.

Unless masked by SMBALERT_MASK, any asserted bit in a status register (including any fault or warning) also pulls the $\overline{\text{ALERT}}$ pin low.

With some exceptions, the SMBALERT_MASK command can be used to prevent the LT7182S from pulling the $\overline{\text{ALERT}}$ pin low for bits in these registers on a bit-by-bit basis. These mask settings apply to STATUS_WORD and STATUS_BYTE in the same fashion as the STATUS bits themselves. For example, if $\overline{\text{ALERT}}$ is masked for all bits in channel 0 STATUS_VOUT, then $\overline{\text{ALERT}}$ is effectively masked for the VOUT bit in STATUS_WORD for PAGE 0.

Status information contained in MFR_COMMON and MFR_PADS can be used to further debug or clarify the contents of STATUS_BYTE or STATUS_WORD as shown, but the contents of MFR_COMMON and MFR_PADS do not directly affect the state of the $\overline{\text{ALERT}}$ pin.

PMBus COMMAND DETAILS



DESCRIPTION	MASKABLE	GENERATES ALERT	BIT CLEARABLE
General Fault or Warning Event	Yes	Yes	Yes
General Non-Maskable Event	No	Yes	Yes
Dynamic	No	No	No
Status Derived from Other Bits	No	Not Directly	No

Figure 1. LTC7182S Status Register Summary

PMBus COMMAND DETAILS

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
CLEAR_FAULTS	0x03	Clear all fault bits	Send Byte	N			
SMBALERT_MASK	0x1B	Mask $\overline{\text{ALERT}}$ pin	Block R/W	Y		Y	
STATUS_BYTE	0x78	One-byte summary of unit's faults and warnings	R/W Byte	Y			
STATUS_WORD	0x79	One-word summary of unit's faults and warnings	R/W Word	Y			
STATUS_VOUT	0x7A	Output voltage faults and warnings	R/W Byte	Y			
STATUS_IOUT	0x7B	Output current faults and warnings	R/W Byte	Y			
STATUS_INPUT	0x7C	Input supply faults and warnings	R/W Byte	Y			
STATUS_TEMPERATURE	0x7D	Internal temperature faults and warnings	R/W Byte	N			
STATUS_CML	0x7E	Communications, memory and logic faults and warnings	R/W Byte	N			
STATUS_MFR_SPECIFIC	0x80	Manufacturer-specific faults and warnings	R/W Byte	Y			
MFR_PADS_LT7182S	0xE5	Digital status of I/O pads	R Word	N			
MFR_COMMON	0xEF	Manufacturer status bits common across multiple Analog Devices parts	R/W Byte	N			
MFR_CHANNEL_STATE	0xF1	Returns the state of the channel	R Byte	Y			
MFR_PIN_CONFIG_STATUS	0xF7	Indicates source of pin config fault	R Byte	N			

CLEAR_FAULTS

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status commands simultaneously. This command also deasserts the $\overline{\text{ALERT}}$ pin. If the fault is still present when the bit is cleared, the fault bit will remain set and the host notified by asserting the $\overline{\text{ALERT}}$ pin low.

The CLEAR_FAULTS command does not clear the $\overline{\text{FAULT}}$ pin, nor does CLEAR_FAULTS cause a unit that has latched off for a fault condition to restart. Units that have shut down for a fault condition are restarted only when:

- The output is commanded to turn off and then to turn back on via the the RUN pin and/or OPERATION command, or
- MFR_RESET command is issued, or
- PV_{IN0} and $EXTV_{CC}$ bias power are removed and reapplied to the device.

Overtemperature and internal reference faults are shared between both channels. Disabling and then reenabling either channel will clear the latched condition for overtemperature and internal reference faults for both channels.

CLEAR_FAULTS can take up to 10µs to process. If a fault occurs within that time frame it may be cleared before the status register is set.

PMBus COMMAND DETAILS

SMBALERT_MASK

The SMBALERT_MASK command can be used to prevent chosen status bits from asserting $\overline{\text{ALERT}}$ low as they are asserted. Only supported bits can be masked.

The bits in the mask byte align with bits in the specified status register. For example, if the STATUS_TEMPERATURE command code is sent in the first data byte, and the mask byte contains 0x40, then a subsequent Overtemperature Warning would still set bit 6 of STATUS_TEMPERATURE but not assert $\overline{\text{ALERT}}$ low. All other supported STATUS_TEMPERATURE bits would continue to assert $\overline{\text{ALERT}}$ low if set.

SMBALERT_MASK cannot be applied to the derived bits in STATUS_BYTE or STATUS_WORD. Bit 7, the busy fault bit, of STATUS_BYTE may be masked. STATUS_WORD is not supported for SMBALERT_MASK.

Providing an unsupported command code to SMBALERT_MASK will generate a CML for Invalid/Unsupported Data.

Table 18. Factory Default SMBALERT_MASK Settings

STATUS REGISTER	MASK VALUE	MASKED BITS
STATUS_VOUT	0x00	None
STATUS_IOUT	0x80	IOUT_OC Fault
STATUS_TEMPERATURE	0x00	None
STATUS_CML	0x00	None
STATUS_INPUT	0x02	IIN_OC Warning
STATUS_MFR_SPECIFIC	0x01	fault pulled low by external device

STATUS_BYTE

The STATUS_BYTE command returns a one-byte summary of the most critical faults. Bit 7 may be cleared by writing a 1 to its position.

Table 19. STATUS_BYTE Contents

BIT	NAME	DESCRIPTION
7	BUSY	A fault was declared because the device was unable to respond to a command.
6	OFF	This bit is set if the channel is not providing power to its output, regardless of the reason, including simply not being enabled.
5	VOUT_OV	An output overvoltage fault has occurred.
4	IOUT_OC	An output overcurrent fault has occurred.
3	UNSUPPORTED	Not supported (device returns 0).
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communication, memory or logic fault has occurred.
0	NONE OF THE ABOVE	A fault or warning not listed in bits[7:1] has occurred.

PMBus COMMAND DETAILS

STATUS_WORD

The STATUS_WORD command returns a two-byte summary of the channel's fault condition. The low byte of the STATUS_WORD is the same as the STATUS_BYTE command. Bit 7 may be cleared by writing a 1 to its position.

Table 20. STATUS_WORD Contents

BIT	NAME	DESCRIPTION
15	VOUT	An output voltage fault or warning has occurred.
14	IOUT	An output current fault or warning has occurred.
13	INPUT	An input voltage fault or warning has occurred.
12	MFR_SPECIFIC	A fault or warning specific to the LT7182S has occurred.
11	POWER NOT GOOD	This bit is set when the PGOOD pin is low.
10:8	UNSUPPORTED	Not supported (device returns 0).

STATUS_VOUT

The STATUS_VOUT command returns one byte of V_{OUT} status information. An individual bit may be cleared by writing a 1 to its position.

Table 21. STATUS_VOUT Contents

BIT	NAME	DESCRIPTION
7	VOUT OV FAULT	V_{OUT} overvoltage fault.
6	VOUT OV WARNING	V_{OUT} overvoltage warning.
5	VOUT UV WARNING	V_{OUT} undervoltage warning.
4	VOUT UV FAULT	V_{OUT} undervoltage fault.
3	VOUT_MAX WARNING	Warning that part was commanded to exceed VOUT_MAX.
2	TON_MAX FAULT	TON_MAX fault.
1	TOFF_MAX WARNING	TOFF_MAX warning.
0	UNSUPPORTED	Not supported (device returns 0).

STATUS_IOUT

The STATUS_IOUT command returns one byte of I_{OUT} status information. An individual bit may be cleared by writing a 1 to its position.

Table 22. STATUS_IOUT Contents

BIT	NAME	DESCRIPTION
7	IOUT OC FAULT	I_{OUT} overcurrent fault.
6	UNSUPPORTED	Not supported (device returns 0).
5	IOUT OC WARNING	I_{OUT} overcurrent warning.
4:0	UNSUPPORTED	Not supported (device returns 0).

PMBus COMMAND DETAILS

STATUS_INPUT

The STATUS_INPUT command returns one byte of input voltage status information. An individual bit may be cleared by writing a 1 to its position.

Table 23. STATUS_INPUT Contents

BIT	NAME	DESCRIPTION
7	VIN OV FAULT	V_{IN} overvoltage fault.
6	UNSUPPORTED	Not supported (device returns 0).
5	VIN UV WARNING	V_{IN} undervoltage warning.
4	UNSUPPORTED	Not supported (device returns 0).
3	UNIT OFF FOR LOW INPUT VOLTAGE	Unit is off due to insufficient input voltage.
2	UNSUPPORTED	Not supported (device returns 0).
1	IIN OC WARNING	Input overcurrent warning.
0	UNSUPPORTED	Not supported (device returns 0).

STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns one byte of sensed internal temperature status information. An individual bit may be cleared by writing a 1 to its position.

Table 24. STATUS_TEMPERATURE Contents

BIT	NAME	DESCRIPTION
7	OT FAULT	Internal overtemperature fault.
6	OT WARNING	Internal overtemperature warning.
5:0	UNSUPPORTED	Not supported (device returns 0).

STATUS_CML

The STATUS_CML command returns one byte of status information regarding PMBus communication, internal memory and logic. An individual bit may be cleared by writing a 1 to its position.

Table 25. STATUS_CML Contents

BIT	DESCRIPTION
7	Invalid or unsupported command received.
6	Invalid or unsupported data received.
5	Packet error check failed.
4	Memory fault detected.
3	Contact factory.
2	Not supported (device returns 0).
1	Other communication fault.
0	Other memory or logic fault.

PMBus COMMAND DETAILS

STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC commands returns one byte with the manufacturer specific status information. Bits 2 through 5 are not page specific. An individual bit may be cleared by writing a 1 to its position, with the exception of the fault log present bit. That bit can only be cleared by the MFR_FAULT_LOG_CLEAR command.

Table 26. STATUS_MFR_SPECIFIC Contents

BIT	DESCRIPTION
7	V_{OUT} turned on when output voltage above discharge threshold.
6	Pin configuration fault. (See MFR_PIN_CONFIG_STATUS for more information).
5	NVM fault.
4	Sync stuck low while SYNC pin is configured as a clock output (MFR_SYNC_CONFIG_LT7182S bit 0 is set to 1).
3	Fault log Present.
2	Internal voltage reference fault.
1	Short Shutdown Cycle Event Occurred.
0	$\overline{FAULT}$ pin pulled low by external device

MFR_PIN_CONFIG_STATUS

During initialization, the LT7182S checks for various illegal pin configurations. If a pin configuration fault is detected, the LT7182S pulls down the FAULT and PGOOD pins, sets STATUS_MFR_SPECIFIC bit 6, and the regulator outputs are locked off until the part is reset. The MFR_PIN_CONFIG_STATUS commands returns one read-only byte indicating what type of pin configuration fault has been detected.

Table 27. MFR_PIN_CONFIG_STATUS Bit Descriptions

BIT	DESCRIPTION
7	A frequency of less than 300kHz is detected on SYNC/PWM_CFG pin during initialization. This may occur if a higher frequency clock starts in the middle of the initialization process. If an external clock is to be applied SYNC/PWM_CFG, it must start before LT7182S initialization begins, or after initialization is complete.
6	SYNC/PWM_CFG pin is hard-tied to ground during initialization and $R_{CONFIGs}$ are not set to ignore (MFR_CONFIG_ALL_LT7182S bit 6 is 0)
5	VSENSE1N pin was detected open-circuit during initialization.
4	VSENSE1P pin was detected open-circuit during initialization.
3	VSENSE0N pin was detected open-circuit during initialization.
2	VSENSE0P pin was detected open-circuit during initialization.
1	Channel 1 is set for polyphase follower (MFR_CHAN_CONFIG_LT7182S bit 8 set high) while internal compensation is selected (I_{TH1} pin tied high).
0	Channel 0 is set for polyphase follower (MFR_CHAN_CONFIG_LT7182S bit 8 set high) while internal compensation is selected (I_{TH0} pin tied high).

PMBus COMMAND DETAILS

MFR_PADS_LT7182S

This read-only command returns the digital status of the listed pins.

Table 28. MFR_PADS_LT7182S Contents

BIT	DESCRIPTION
15	I_{TH1} tied high externally (internal compensation selected)
14	I_{TH0} tied high externally (internal compensation selected)
13	Sync input clock active
12	WP
11	Device driving PGOOD1 low
10	Device driving PGOOD0 low
9	PGOOD1
8	PGOOD0
7	Device driving RUN1 low
6	Device driving RUN0 low
5	RUN1
4	RUN0
3	Device driving $\overline{\text{FAULT1}}$ low
2	Device driving $\overline{\text{FAULT0}}$ low
1	$\overline{\text{FAULT1}}$
0	$\overline{\text{FAULT0}}$

MFR_COMMON

The MFR_COMMON command contains bits that are common to all Analog Devices digital power and telemetry products. This command cannot cause the $\overline{\text{ALERT}}$ pin to be asserted.

Table 29. MFR_COMMON Contents

BIT	DESCRIPTION
7	Chip not driving $\overline{\text{ALERT}}$ low
6	Chip not busy
5	Calculations not pending
4	Output not in transition
3	NVM initialized
2	Reserved (device returns 0)
1	SHARE_CLK timeout
0	WP pin status

PMBus COMMAND DETAILS

MFR_CHANNEL_STATE

The MFR_CHANNEL_STATE command returns the state of the channel.

Table 30. MFR_CHANNEL_STATE Values

VALUE	DESCRIPTION
0, 7	Off
2	Waiting for TON_DELAY
3	Power-on ramp up (TON_RISE)
4, 5	On
6	Waiting for TOFF_DELAY
8	Power-off ramp down (TOFF_FALL)

TELEMETRY

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
READ_VIN	0x88	Measured input supply voltage.	R Word	Y	V		
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	V		
READ_IIN	0x89	Calculated input supply current.	R Word	Y	A		
READ_IOUT	0x8C	Measured output current.	R Word	Y	A		
READ_TEMPERATURE_1	0x8D	Measured internal temperature.	R Word	N	C		
READ_FREQUENCY	0x95	Frequency of top gate.	R Word	Y	kHz		
READ_POUT	0x96	Calculated output power.	R Word	Y	W		
MFR_READ_EXTVCC	0xCD	Measured $EXTV_{CC}$ pin voltage.	R Word	N	V		
MFR_READ_ITH	0xCE	Measured I_{THx} pin voltage.	R Word	Y	V		
MFR_IOUT_PEAK	0xD7	Maximum READ_IOUT	R Word	Y	A		
MFR_ADC_CONTROL_LT7182S	0xD8	ADC configuration	R/W Byte	N		Y	0x00
MFR_VOUT_PEAK	0xDD	Maximum READ_VOUT	R Word	Y	V		
MFR_VIN_PEAK	0xDE	Maximum READ_VIN	R Word	Y	V		
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum READ_TEMPERATURE_1	R Word	Y	C		
MFR_CLEAR_PEAKS	0xE3	Clears all recorded peak values	Send Byte	Y			

READ_VIN

The READ_VIN command returns the measured input voltage.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

PMBus COMMAND DETAILS

READ_VOUT

The READ_VOUT command returns the measured output voltage.

This command uses either ULinear16 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

READ_IIN

The READ_IIN command returns the input current.

The input current for a channel is calculated internally using Equation 1:

$$I_{IN} = \left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT}\right) + \left(V_{IN} \bullet \text{SwitchingFrequency} \bullet V_{IN}\ \text{Gain Trim SW}\right) \qquad (1)$$

For $I_{IN}[0]$, if $EXTV_{CC}$ LDO is not enabled, V_{CC} current is calculated using Equation 2 and added to Equation 1 result.

$$I_{VCC} = (\text{Switching Frequency [ch0] + Switching Frequency [ch1]}) \bullet KI_{VCC} + I_{VCC}\ \text{STBY} \qquad (2)$$

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

READ_IOUT

The READ_IOUT command returns the measured output current.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

READ_TEMPERATURE_1

The READ_TEMPERATURE_1 command returns the internal device temperature.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

READ_FREQUENCY

The READ_FREQUENCY command returns the top switch switching frequency in kHz.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

PMBus COMMAND DETAILS

READ_POUT

The READ_POUT command returns average output power. The output power is calculated based on the most recent correlated output voltage and output current readings.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

MFR_READ_EXTVCC

The MFR_READ_EXTVCC command returns the measured voltage on the EXTVCC pin.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

MFR_READ_ITH

The MFR_READ_ITH command returns the measured voltage on either the I_{TH0} pin or the I_{TH1} pin, depeding on the selected page.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

MFR_IOUT_PEAK

The MFR_IOUT_PEAK command reports the highest output current measured.

This command is cleared using the MFR_CLEAR_PEAKS command.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

MFR_ADC_CONTROL_LT7182S

The MFR_ADC_CONTROL_LT7182S command controls adjustable features of the telemetry loop.

Bit 1 enables lower-frequency telemetry measurements in order to reduce input supply current. When this bit is set, the telemetry runs with a typical period of 100ms (compared to a typical period of 6.5ms when this bit is zero).

Bit 0 enables the debug telemetry measurements: $EXTV_{CC}$, I_{TH0}, I_{TH1}. When those are enabled, the sampling rate of the other measurements will decrease.

PMBus COMMAND DETAILS

Table 31. MFR_ADC_CONTROL_LT7182S Contents

BIT	DEFAULT	DESCRIPTION
1	0	Enable low frequency telemetry (100ms typical period, 3mA typical supply current reduction)
0	0	Debug telemetry measurements: standard + $EXTV_{CC}$, I_{TH0}, I_{TH1}

MFR_VOUT_PEAK

The MFR_VOUT_PEAK command reports the highest output voltage measured.

This command is cleared using the MFR_CLEAR_PEAKS command.

This command uses either ULinear16 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

MFR_VIN_PEAK

The MFR_VIN_PEAK command reports the highest input voltage measured.

This command is cleared using the MFR_CLEAR_PEAKS command.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

MFR_TEMPERATURE_1_PEAK

The MFR_TEMPERATURE_1_PEAK command reports the highest internal temperature measured.

This command is cleared using the MFR_CLEAR_PEAKS command.

This command uses either Linear11 or half-precision floating point format, as selected by MFR_CONFIG_ALL_LT7182S bit 8.

MFR_CLEAR_PEAKS

The MFR_CLEAR_PEAKS command clears the MFR_*_PEAK data values. These values are also cleared at reset or powerup.

NVM COMMANDS

All EEPROM commands are disabled if the internal die temperature exceeds 170°C. They are re-enabled when the die temperature falls below 150°C.

Most EEPROM access commands will take milliseconds to complete.

PMBus COMMAND DETAILS

Table 32. Store/Restore

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
STORE_USER_ALL	0x15	Store user operating memory to NVM.	Send Byte				
RESTORE_USER_ALL	0x16	Restore user operating memory from NVM.	Send Byte				
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with NVM.	Send Byte				
MFR_USER_DATA_00	0xC9	EEPROM word available for the user	R/W Word			Y	0x0000
MFR_USER_DATA_01	0xCA	EEPROM word available for the user	R/W Word			Y	0x0000
MFR_USER_DATA_02	0xCB	EEPROM word available for the user	R/W Word			Y	0x0000
MFR_USER_DATA_03	0xCC	EEPROM word available for the user	R/W Word			Y	0x0000
MFR_DISABLE_OUTPUT	0xFB	Disables regulator outputs until reset	R/W Byte				0x00
MFR_EE_USER_WP	0xFC	Disables commands that write user NVM	R/W Byte	N		Y	0x00

STORE_USER_ALL

The STORE_USER_ALL command instructs the device to copy the contents of the Operating Memory to nonvolatile EEPROM memory (NVM). All commands desginated as NVM-backed commands will be stored in NVM by this command.

Executing this command if the die temperature exceeds 150°C is not recommended and the data retention of 10 years cannot be guaranteed. If the die temperature exceeds 170°C, the STORE_USER_ALL command is disabled. The command is re-enabled when the IC temperature drops below 150°C.

RESTORE_USER_ALL

The RESTORE_USER_ALL command provides a means by which the user can perform a reset of the device.

MFR_COMPARE_USER_ALL

The MFR_COMPARE_USER_ALL command instructs the PMBus device to compare current command contents with what is stored in nonvolatile memory. If the compare operation detects differences, a CML bit 0 fault will be generated.

MFR_COMPARE_USER_ALL commands are disabled if the die exceeds 170°C and are not re-enabled until the die temperature drops below 150°C.

PMBus COMMAND DETAILS

MFR_USER_DATA_00, MFR_USER_DATA_01, MFR_USER_DATA_02, MFR_USER_DATA_03

The MFR_USER_DATA_xx commands may be used by the user to store any data. Each of these commands stores one 16-bit word. This data is written to the EEPROM when the STORE_USER_ALL command is written.

MFR_DISABLE_OUTPUT

When written to 0xff, this command disables the regulator outputs until reset. This allows anything to be programmed into ON_OFF_CONFIG, OPERATION, etc. without powering up the output. This is intended to allow all NVM-stored commands to be configured and written to EEPROM with STORE_USER_ALL without powering up the output. This command can be read to determine the state of the output disable function.

MFR_EE_USER_WP

When written to 0xFF, this command disables the commands that can be used to write the user NVM space: STORE_USER_ALL, MFR_EE_ERASE, MFR_EE_DATA writes. This command can only be written to 0xFF. Once written to NVM with STORE_USER_ALL, these commands will remain disabled including when power is removed and reapplied.

FAULT LOGGING

If a fault condition occurs that is configured to turn off the regulator output, an event is written in the fault log in EEPROM. Any preceeding warning or fault that is not configured to turn off the output is written as a subevent when an event is written. A timestamp is written with each event and subevent. The fault log stores up to three fault-off events. The fault log may be read by the MFR_FAULT_LOG command. The fault log is cleared from EEPROM by writing the MFR_FAULT_LOG_CLEAR command. The fault log function is enabled by default and may be disabled by clearing bit 7 of MFR_CONFIG_ALL.

If $INTV_{CC}$ UV is detected while writing the fault log, the PMBus port and ADC loop will be immediately disabled to save power.

Automatic fault logging is never disabled due to overtemperature.

COMMAND NAME	CODE	DESCRIPTION	TYPE	PAGED	UNITS	NVM	DEFAULT
MFR_FAULT_LOG_TIMESTAMP_MSBS	0xE8	Sets the fault log timestamp upper 13 bits, clears lower 32 (read and write first)	R/W 32	N			
MFR_FAULT_LOG_TIMESTAMP_LSBS	0xE9	Sets the fault log timestamp lower 32 bits	R/W 32	N			
MFR_FAULT_LOG_STORE	0xEA	Force a fault log entry to be written	Send Byte	N			
MFR_FAULT_LOG_CLEAR	0xEC	Erases all fault log entries, if any	Send Byte	N			
MFR_FAULT_LOG	0xEE	Read contents of fault log, if any	R Block	N		Y	

PMBus COMMAND DETAILS

MFR_FAULT_LOG_TIMESTAMP_MSBS, MFR_FAULT_LOG_TIMESTAMP_LSBS

The MFR_FAULT_LOG_TIMESTAMP_MSBS command sets the most significant 13 bits of the fault log timestamp, and the MFR_FAULT_LOG_TIMESTAMP_LSBS command sets the least significant 32 bits of the fault log timestamp. The timestamp has units of SHARE_CLK pulses (typically approximately 10µs).

The most significant 13 bits (MSBS) must be written before the least significant 32 bits (LSBS) are written. Writing the MSBS causes the LSBS to be cleared to 0. This guarantees that the 45-bit timestamp counter can be written atomically.

The MSBS must also be read before the LSBS are read. Reading the MSBS causes the LSBS to be captured and prepared to be read. This guarantees that the 45-bit timestamp counter can be read atomically.

MFR_FAULT_LOG_STORE

The MFR_FAULT_LOG_STORE command forces a fault log to be written to EEPROM just as if a fault event occurred.

MFR_FAULT_LOG_CLEAR

The MFR_FAULT_LOG_CLEAR command will erase the stored fault log, if any. It will also clear bit 3 in the STATUS_MFR_SPECIFIC command.

MFR_FAULT_LOG

The MFR_FAULT_LOG command will return the current fault log contents. The fault log is composed of events, which each contain event fields and two preceding subevents. Subevents are events that do not cause a fault-off condition (for example warning or PV_{IN} < VIN_OFF, etc). Subevents are logged to volatile memory until a fault occurs, at which time the fault event and associated subevents are logged to nonvolatile memory.

As with all PMBus block read commands, the least significant byte will be seen on the bus first.

The external assertion of the $\overline{\text{FAULT}}$ pin will be captured as an event if bit 5 of MFR_CHAN_CONFIG_LT7182S is set. Otherwise, it will be captured as a subevent.

The timestamp field has units of SHARE_CLK pulses (typically approximately 10µs).

PMBus COMMAND DETAILS

In the event structure, the paged faults, paged warnings, unpaged faults, and unpaged warnings reflect the underlying fault and warning conditions that were present when the event was recorded. Status registers, such as `status_vout`, may have bits set from prior fault or warning conditions that are no longer present.

Table 33. Fault Log Structure

ENTRY	ITEM	PMBus BYTE NUMBER
3	Subevent	147–140
	Subevent	139–132
	Event	131–111
2	Subevent	110–103
	Subevent	102–95
	Event	94–74
1	Subevent	73–66
	Subevent	65–58
	Event	57–37
0	Subevent	36–29
	Subevent	28–21
	Event	20–0

EVENT STRUCTURE

PMBus BYTE NUMBER	FIELD	STRUCTURE BIT NUMBER
20–14	Reserved (some of this is parity)	167:112
13	Reserved	111:106
	Event CRC check: 0 if match	105
	Subevents CRC check: 0 if match	104
12	Temperature (unsigned, offset +70°C above die temperature)	103:96
11	Channel 1 State	95:92
	Channel 0 State	91:88
10–8	Paged Warnings	87:74
	Unpaged Warnings	73
7	Paged Faults	72:55

PMBus COMMAND DETAILS

PMBus BYTE NUMBER	FIELD	STRUCTURE BIT NUMBER
6	Unpaged Faults	54:53
5–1	Timestamp	52:8
0	Ordinal (see Table 36 and Table 37)	7:3
	Page (unpaged will be 2)	2:1
	Valid Bit: 1 if valid	0

Table 34. Subevent Structure

PMBus BYTE NUMBER	FIELD	STRUCTURE BIT NUMBER
7	Reserved	63:61
	Channel 1 State	60:57
6	Channel 0 State	56:53
5–1	Timestamp	52:8
0	Ordinal (see Table 36 and Table 37)	7:3
	Page (unpaged will be 2)	2:1
	Valid Bit	0

Table 35. Ordinal Table for Unpaged Events and Subevents

ORDINAL	EVENT	TYPE
5	Overtemperature Warning	Warnings
2	Thermal Shutdown	Faults that caused a fault off
1	Reference Fault	
0	No fault event. Fault event recorded by MFR_FAULT_LOG_STORE.	

Table 36. Ordinal Table for Paged Events and Subevents

ORDINAL	EVENT	TYPE
25	V_{OUT} overvoltage warning	Warning
24	V_{OUT} undervoltage warning	
23	I_{OUT} overcurrent warning	
21	V_{IN} undervoltage warning	
20	I_{IN} overcurrent warning	
19	TOFF_MAX_WARN_LIMIT exceeded when turning off an output	
17	PV_{IN} fell below VIN_OFF	N/A
16	V_{OUT} overvoltage fault, response set to continue operation	Faults
15	V_{OUT} undervoltage fault, response set to continue operation	
14	I_{OUT} overcurrent fault, response set to continue operation	
13	TON_MAX_FAULT_LIMIT exceeded when turning on an output, response set to continue operation	

PMBus COMMAND DETAILS

Table 36. Ordinal Table for Paged Events and Subevents

ORDINAL	EVENT	TYPE
12	$\overline{\text{FAULT}}$ pin externally pulled low	Faults that caused a fault off
9	PV_{IN} overvoltage fault	
7	V_{OUT} overvoltage fault, response set to disable output	
6	V_{OUT} undervoltage fault, response set to disable output	
5	I_{OUT} overcurrent fault, response set to disable output	
4	TON_MAX_FAULT_LIMIT exceeded when turning on an output, response set to disable output	
2	Short shutdown cycle fault	
0	No fault event. Fault event recorded by MFR_FAULT_LOG_STORE.	N/A

Table 37. Channel State Ordinal Table

ORDINAL	STATE
8	Sequencing off and ramping down output
7	RESET
6	Sequencing off and waiting for TOFF_DELAY
5	On
4	Waiting for TON_MAX_FAULT or output to rise above VOUT_UV_FAULT_LIMIT
3	Sequencing on and ramping up output
2	Sequencing on and waiting for ON_DELAY
1	Faulted off and waiting for retry delay
0	Off

Table 38. Unpaged Fault Bit Descriptions

BIT	DESCRIPTION
1	Thermal Shutdown
0	Reference Fault

Table 39. Paged Faults Event Field

ITEM	BITS
Paged Fault Bits Page 1	17:9
Paged Fault Bits Page 0	8:0

Table 40. Paged Fault Bit Descriptions

BIT	DESCRIPTION
8	V_{IN} Overvoltage Fault
7	V_{IN} Off (Not a fault condition)
6	V_{OUT} Overvoltage Fault
5	V_{OUT} Undervoltage Fault

PMBus COMMAND DETAILS

Table 40. Paged Fault Bit Descriptions

BIT	DESCRIPTION
4	I_{OUT} Overcurrent Fault
3	Reserved
2	$\overline{FAULT}$ pin Asserted
1	Short Shutdown Cycle Fault
0	Pin Config Fault

Table 41. Unpaged Warning Bit Descrptions

BIT	DESCRIPTION
0	Overtemperature Warning

Table 42. Paged Warnings Event Field

ITEM	BITS
Paged Warning Bits Page 1	13:7
Paged Warning Bits Page 0	6:0

Table 43. Paged Warning Bit Descrptions

BIT	DESCRIPTION
6	V_{OUT} Overvoltage Warning
5	V_{OUT} Undervoltage Warning
4	I_{OUT} Overcurrent Warning
3	Reserved
2	V_{IN} Undervoltage Warning
1	I_{IN} Overcurrent Warning
0	Reserved

EXAMPLE EVENT

This is an example of a fault event caused by a V_{OUT} overvoltage fault. If MFR_FAULT_LOG were read after this event was recorded, an example stream of bytes on the bus would be:

0x39, 0x70, 0x11, 0x01, 0x00, 0x00, 0x00, 0x20, 0x00, 0x00, 0x01, 0x05, 0xAA, 0x03, … and 7 more bytes that should be ignored.

The table below breaks this byte stream into bit fields in the event structure.

PMBus COMMAND DETAILS

Table 44.

PMBus BYTE NUMBER	FIELD	STRUCTURE BIT NUMBER (LSB FIRST)	DATA	MEANING
20–14	Reserved	167:112		These bits should be ignored
13	Reserved	111:106		These bits should be ignored
	Event CRC check	105	1	Event CRC is valid
	Subevents CRC check	104	1	Subevent CRC is valid
12	Temperature	103:96	0xAA	Die temperature was 100°C when the fault occurred
11	Channel 1 State	95:92	0	Channel 1 was off when the fault occurred
	Channel 0 State	91:88	5	Channel 0 was on when the fault occurred
10–8	Paged Warnings	87:74	0x40, 0x00	V_{OUT} overvoltage warning on channel 0
	Unpaged Warnings	73	0	No unpaged warnings
7	Paged Faults	72:55	0x40, 0x00, 0x00	V_{OUT} overvoltage fault on channel 0
6	Unpaged Faults	54:53	0	No unpaged faults
5–1	Timestamp	52:8	0x70, 0x11, 0x01, 0x00, 0x00, 0x00	70,000µs
0	Ordinal	7:3	7	Indicates a V_{OUT} overvoltage fault
	Page	2:1	0	Indicates the event was caused by some fault on channel 0
	Valid Bit	0	1	Entry is valid