DEMO MANUAL DC2067A

# LT8710 Synchronous Inverting DC/DC Converter 

## DESCRIPTIOn

Demonstration circuit 2067A is a synchronous inverting converter (CUK topology) featuring the LT®8710 switching controller. It regulates a $-5 \mathrm{~V}, 6 \mathrm{~A}$ output from a 4.5 V to 28 V input source, and operates at 300 kHz switching frequency.

The LT8710 features simple negative or positive output voltage programming. The DC2067 programs a-5V output with a single resistor.
At light load, the LT8710 can operate at forced continuous conduction mode (CCM) or discontinuous conduction mode (DCM), set by its MODE pin. The DC2067A selects DCM, which maintains high efficiency at light load.
The DC2067A can be modified from a CUK converter to other topology. Synchronous SEPIC and synchronous BOOST schematics are provided in the data sheet. Please consult the factory or LT8710 data sheet for details regarding how to customize the DC2067A or how to design different topologies for custom specifications.

There are some optional components on the DC2067A to facilitate modifications; see Full Schematic Diagram for component designation.

1. The optional N-FET (MN2) or P-FET (MP2) could be added to increase power delivery and improve thermal dissipation.
2. The optional RC snubber (R4, C1) across the flying capacitor could help to damp the feedback control loop for some applications using two separate inductors.
3. The optional input capacitors (CIN5, CIN6) or output capacitors (CO5, CO6) could be installed to reduce voltage ripple for some low voltage and/or high current applications.
4. The optional RC (R24,C19) snubbercould be installed to damp the switch node spike and reduce the EMI noise.
5. The optional current sensing resistor filters (located near CSP and CSN pins, ISP and ISN pins) might be required in certain applications with excessive switching noise.
The LT8710 data sheet gives a complete description of the part, operation and application information. The data sheet must be read in conjunction with this quick start guide for demo circuit 2067A.
Design files for this circuit board are available at http://www.linear.com/demo
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PGRFORMANCE SUMMARY
Specifications are at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| PARAMETER | CONDITIONS | MIN | TYP | MAX |
| :--- | :--- | :---: | :---: | :---: |
| Input Voltage |  | 4.5 | 12 | 28 |
| UnIput Voltage | $\mathrm{V}_{\text {IN }}=4.5 \mathrm{~V}$ to $28 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=0 \mathrm{~A}$ to 6 A | -5 | -5.15 | V |
| Maximum Output Current |  | -4.85 | V |  |
| Output Voltage Ripple | $\mathrm{V}_{\text {IN }}=4.5 \mathrm{~V}$ to $28 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=6 \mathrm{~A}(20 \mathrm{MHz}$ BW $)$ |  | A |  |
| Typical Switching Frequency |  | 25 | mV P-P |  |
| Efficiency | $\mathrm{V}_{\text {IN }}=5 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=6 \mathrm{~A}$ | 300 | kHz |  |
|  | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=6 \mathrm{~A}$ | 85 | $\%$ |  |
|  | $\mathrm{~V}_{\text {IN }}=24 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=6 \mathrm{~A}$ | 88.5 | $\%$ |  |

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## PUICK START PROCEDURE

Demonstration circuit 2067A is easy to set up to evaluate the performance of the LT8710. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. With the power off, connect the input power supply to the board through VIN and PGND terminals. Connect the load to the terminals VOUT and PGND on the board. Make sure that the input power supply has sufficient current rating at minimum input voltage for the required output load.
2. Turn on the power at the input.

Note: Make sure that the inputvoltage does not exceed 28V.
3. Check for the proper output voltages. The output should be regulated at $-5.0 \mathrm{~V}( \pm 3 \%)$.
If there is no output, temporarily disconnect the Ioad to make sure that the load is not set too high.
4. Once the proper output voltage is established, adjust the input voltage and load current within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters.

Note: When measuring the input or output voltage ripples, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across the VIN and PGND, or VOUT and PGND terminals. See Figure 2 for proper scope probe technique.
5. The DC2067A is equipped with an output capacitor CO1 (270 1 F) that approximates typical system rail capacitance. If the system board already has capacitance of similar value, CO1 can be removed. The input capacitor CIN1 is used to help with filtering when the board is connected to lab power supply with long leads. The capacitor CIN1 can be removed if the input power source is close and has low source impedance.

## PUICK START PROCEDURE



Figure 1. Proper Measurement Equipment Setup


Figure 2. Proper Scope Probe Placement for Measuring Input or Output Ripple


Figure 3. Typical Efficiency Curve

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## PUICK START PROCEDURE

N-FET Temperature Rise vs Input Voltage


Figure 4. N-FET (MN1) Temperature Rise vs Input Voltage


Figure 5. Output Voltage Ripple at $12 \mathrm{~V}_{\mathrm{IN}}$ and $6 \mathrm{~A}_{\mathrm{OUT}}, 20 \mathrm{MHz}$ Bandwidth

## DEMO MANUAL DC2067A

## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| Required Circuit Components |  |  |  |  |
| 1 | 6 | C2, C3, C4, CIN2, CIN3, CIN4 | CAP., X7R, 10 ${ }^{\text {F }}$ F, 50V, 10\% 1210 | MURATA, GRM32ER71H106KA12L |
| 2 | 1 | C5 | CAP., X7R, 0.47山F, 16V, 10\% 0805 | MURATA, GRM21BR71C474KA01L |
| 3 | 2 | C11, C14 | CAP., X7R, 2.2 $2 \mathrm{~F}, 16 \mathrm{~V}, 10 \%, 0805$ | MURATA, GRM21BR71C225KA12L |
| 4 | 1 | C13 | CAP., X7R, 4.7 FF, 50V, 10\%, 1206 | TDK, C3216X7R1H475K |
| 5 | 1 | C15 | CAP., X7R, 4.7nF, 16V, 10\%, 0603 | MURATA, GRM188R71C472A01D |
| 6 | 1 | C16 | CAP., COG, 100pF, 50V, 5\%, 0603 | TDK, C1608COG1H101J |
| 7 | 1 | C17 | CAP., X7R, 470nF, 16V, 10\%, 0603 | MURATA, GRM188R71C474KA88D |
| 8 | 1 | C18 | CAP., X7R, 47nF, 16V, 10\%, 0603 | TDK, C1608X7R1C473K |
| 9 | 1 | CIN1 | ALUMINUM CAP., 330^F, 35V, | NIPPON, EMZA350ADA331MJA0G |
| 10 | 1 | C01 | OS-CON, 270^F, 10V, E7 SIZE | SANYO/PANASONIC, 10SVPC270M |
| 11 | 3 | CO2, C03, CO4 | CAP., X5R, 100 ${ }^{\text {F }}$, 6.3V, 20\% 1210 | MURATA, GRM32ER60J107ME20L |
| 12 | 1 | D1 | DIODE, PMEG4030EP, SOD128 | NXP, PMEG4030EP |
| 13 | 1 | D2 | DIODE, SCHOTTKY 30V 500MA SOD323F | NXP, PMEG3005EJ+115 |
| 14 | 1 | L1 | IND, $2.2 \mu \mathrm{H}$ | WÜRTH, 74485540220 |
| 15 | 1 | MN1 | N-CH FET, POWERPAK SO-8 | FAIRCHILD, FDMS86500L |
| 16 | 1 | MP1 | P-CH FET, DPAK | FAIRCHILD, FDD4141 |
| 17 | 1 | R1 | RES., SENSE, $0.002 \Omega, 1 \mathrm{~W}, 1 \%$ RL3720W | SUSUMU, RL3720WT-R002-F |
| 18 | 1 | R3 | RES., SENSE, $0.006 \Omega, 1 \mathrm{~W}, 1 \%$ RL3720W | SUSUMU, RL3720WT-R006-F |
| 19 | 8 | R5, R6, R7, R9 ,R12, R15, R16, R18 | Res., Chip, 0, 0.1W, 0603 | VISHAY, CRCW06030000Z0EA |
| 20 | 1 | R5, R6, R7, R9, R12, R15, R16, R19 | Res., Chip, 499』, 0.1W, 1\%, 0603 | VISHAY, CRCW0603499RFKEA |
| 21 | 1 | R13 | Res., Chip, 60.4k, 0.1W, 1\%, 0603 | VISHAY, CRCW060360K4FKEA |
| 22 | 1 | R17 | Res., Chip, 12.7k, 0.1W, 1\%, 0603 | VISHAY, CRCW060312K7FKEA |
| 23 | 2 | R19, R23 | Res., Chip, 100k, 0.1W, 1\%, 0603 | VISHAY, CRCW0603100KFKEA |
| 24 | 1 | R20 | Res., Chip, 10k, 0.1W, 1\%, 0603 | VISHAY, CRCW060310KOFKEA |
| 25 | 1 | R21 | Res., Chip, 118k, 0.1W, 1\%, 0603 | VISHAY, CRCW0603118KFKEA |
| 26 | 1 | R22 | Res., Chip, 12.1k, 0.1W, 1\%, 0603 | VISHAY, CRCW060312K1FKEA |
| 27 | 1 | U1 | IC, DC/DC CONVERTER, TSSOP-20 | LINEAR TECH., LT8710EFE\#PBF |
| 28 | 1 |  | FAB, PRINTED CIRCUIT BOARD | DEMO CIRCUIT 2067A REV 4 |

## Additional Demo Board Circuit Components

| 1 | 0 | C1 (OPT) | CAP., 2220 |  |
| :---: | :--- | :--- | :--- | :--- |
| 2 | 0 | C20, CIN5, CIN6, CO5, CO6 (OPT) | CAP., 1210 |  |
| 3 | 0 | C6, C7, C8, C9, C10 (OPT) | CAP., 0603 |  |
| 4 | 0 | C12 (OPT) | CAP., 1206 |  |
| 5 | 0 | C19 (OPT) | CAP., 0805 |  |
| 6 | 0 | MN2 (OPT) | N-CH FET, POWERPAK S0-8 |  |
| 7 | 0 | MP2 (OPT) | P-CH FET, DPAK |  |
| 8 | 0 | R2 (OPT) | RES., SENSE, RL3720W |  |
| 9 | 0 | R4, R24 (OPT) | RES., 1210 |  |
| 10 | 0 | R10, R11, R14 (OPT) | RES., 0603 |  |

## Hardware-For Demo Board Only

| 1 | 14 | E1-E14 | TESTPOINT, TURRET, 0.094" PBF | MILL-MAX, 2501-2-00-80-00-00-07-0 |
| :---: | :---: | :--- | :--- | :--- |
| 2 | 1 | JP1 | 3-PIN 0.079 SINGLE ROW HEADER | SULLINS, NRPN031PAEN-RC |
| 3 | 1 | XJP1 | SHUNT, 0.079" CENTER | SAMTEC, 2SN-BK-G |
| 4 | 4 | MH1-MH4 | STAND-OFF, NYLON 0.50" | KEYSTONE, 8833(SNAP 0N) |

## DEMO MANUAL DC2067A

## simple schematic diagram



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## fULL SCHEMATIC DIAGRAM (OPTIONAL COMPONEחTS SHOWN)



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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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