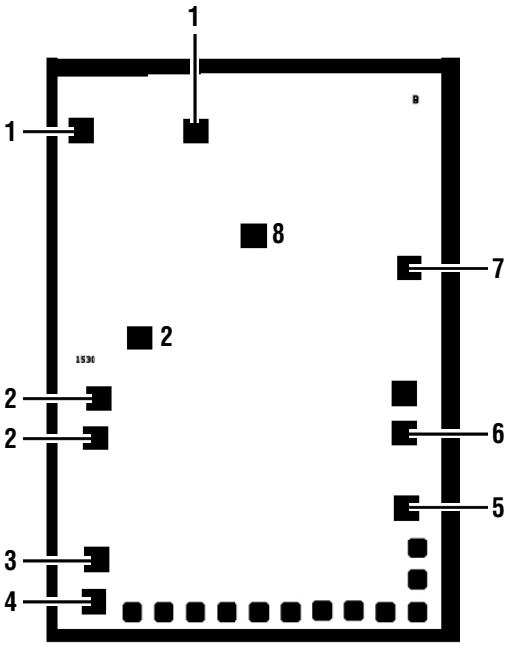
LTC1530
High Power Synchronous Switching Regulator Controller



101mils × 70mils,
12mils thick.
Backside metal: Alloyed gold layer
Backside potential: Connect to GND

PAD FUNCTION

1. P_{VCC}
2. GND
3. V_{SENSE}
4. COMP
5. I_{MAX}
6. I_{FB}
7. G2
8. G1

DIE CROSS REFERENCE

LTC® Finished Part Number	Order Part Number
LTC®1530 LTC1530	LTC1530DICE LTC1530DWF*

Please refer to ADI standard product data sheet for other applicable product information.
***DWF = DICE in wafer form.**

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
PV_{CC} 14V
Input Voltage
I_{FB} (Note 2) ..... PV_{CC} + 0.3V
I_{MAX} ..... –0.3V to 14V
I_{FB} Input Current (Notes 2, 3) ..... –100mA

DICE/DWF ELECTRICAL TEST LIMITS T_A = 25°C. PV_{CC} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	MAX	UNITS
PV_{CC}	Supply Voltage	(Note 6)			13.2	V
V_{UVLO}	Undervoltage Lockout Voltage	(Note 7)			3.75	V
V_{SENSE}	Internal Feedback Voltage	(Note 4)		1.223	1.247	V
I_{PVCC}	Quiescent Current	COMP = 0.5V, V_{FB} = 5V			1.4	mA
	Shutdown Supply Current	COMP = 0 (Note 8)			80	µA
f_{OSC}	Internal Oscillator Frequency			250	350	kHz
G_{ERR}	Error Amplifier Open-Loop DC Gain	(Note 5)		40		dB
g_{mERR}	Error Amplifier Transconductance	(Note 5)		1.6	2.8	millimho
I_{MAX}	I_{MAX} Sink Current	V_{IMAX} = 5V		170	230	µA
V_{SHDN}	Shutdown Threshold Voltage	Measured at COMP Pin (Note 7)		100		mV
t_r, t_f	Driver Rise and Fall Time				140	ns
t_{NOL}	Driver Nonoverlap Time			30		ns
DC_{MAX}	Maximum G1 Duty Cycle			81		%

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: If I_{FB} is taken below GND, it is clamped by an internal diode. This pin handles input currents ≤ 100mA below GND without latch-up. In the positive direction, it is not clamped to PV_{CC}.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: The LTC1530 is tested in an op amp feedback loop which regulates V_{SENSE} based on V_{COMP} = 2V for the error amplifier.

Note 5: The Open-loop DC gain and transconductance from the V_{FB} pin to the COMP pin are G_{ERR} and g_{mERR} respectively.

Note 6: The total voltage from the PV_{CC} pin to the GND pin must be ≥8V for the current limit protection circuit to be active.

Note 7: G1 and G2 begin to switch once PV_{CC} is ≥ the undervoltage lockout threshold voltage.

Note 8: The LTC1530 enters shutdown if COMP is pulled low.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-1530

ANALOG DEVICES