## DESCRIPTION

Demonstration circuit board DC106 provides a constant frequency, 4-output, low noise switching regulator. The outputs include: $5 \mathrm{~V} / 3 \mathrm{~A}, 3.3 \mathrm{~V} / 3 \mathrm{~A}, 12 \mathrm{~V} / 200 \mathrm{~mA}$ and $2.9 \mathrm{~V} / 3 \mathrm{~A}$. Refer to the LTC ${ }^{\circledR} 1438 /$ LTC1439 and LTC1538-AUX/ LTC1539 data sheets for other possible configurations. The 5 V and 3.3 V outputs are complete synchronous buck switching regulators. The 12 V is derived from a secondary winding and is regulated irrespective of the load on the primary 5 V output using a secondary feedback control inputto the first controller. The 2.9 V output is derived from the 3.3 V output using an internal linear regulator controller. The transient response and peak current rating of 3 A
is consistent with Intel P54LM requirements. The controllers operate at a constant frequency of 200 kHz , thereby providing low noise operation. This constant frequency prevents any unpredictable or audible radiation. The controller can operate ata $99 \%$ duty cycle for very low dropout conditions. Internal power-on reset and a second uncommitted comparator are included to facilitate a complete system power solution. The demonstration board operates on an input supply of from 5.2 V to 28 V , however, 12 V output power is limited at low input voltages. Gerber files for this circuit board are available. Call the LTC factory.

PGRFORMANCE SUMMARY (continued on page 2) Operating Temperature Range $0^{\circ} \mathrm{C}$ to $50^{\circ} \mathrm{C}$.

| Input Voltage/Current Range | Input Voltage Limited by External MOSFET Drive and Breakdown Requirements | 5.2 V to 28 V | 8 A Max |
| :--- | :--- | :---: | :---: |
| Output | Output Voltage, Controller 1 (J11-J12) | $5 \mathrm{~V} \pm 0.1 \mathrm{~V}$ | 3 A |
|  | Output Voltage, Controller 2 (J7-J8) | $3.3 \mathrm{~V} \pm 0.08 \mathrm{~V}$ | 3 A |
|  | Output Voltage, Auxiliary Regulator (J2-J5) | $2.9 \mathrm{~V} \pm 0.10 \mathrm{~V}$ | 3 A |
|  | Output Voltage, Controller 1 Synchronous Secondary (J10-J9); $\mathrm{V}_{1 \mathrm{~N}}>=7 \mathrm{~V}$ | $12 \mathrm{~V} \pm 0.60 \mathrm{~V}$ | 0.2 A |

Specifications on this data sheet are preliminary only, and subject to change without notice.
Contact the manufacturer before finalizing a design using this part.

## TYPICAL PGRFORMANCE CHARACTERISTICS AND BOARD PHOTOS




Back


## DEMO MANUAL DC106 <br> DESIGN-READY SWITCHERS

PERFORMARMCE SUMMARRY (continued from page 1) Operating Temperature Range $0^{\circ} \mathrm{C}$ to $50^{\circ} \mathrm{C}$.

| PARAMETER | CONDITIONS | OUTPUT 1 | OUTPUT 2 | OUTPUT 3 | OUTPUT 4 | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage |  | $5 \mathrm{~V} \pm 0.1$ | $3.3 \mathrm{~V} \pm 0.08$ | $12 \mathrm{~V} \pm 0.6$ | $2.9 \mathrm{~V} \pm 0.05$ | V |
| Output Rated Current |  | 3 | 3 | 0.2 | 3 | A |
| Line Regulation | Measured at Rated Current | 0.013 | 0.002 | 0.16 | 0.007 | \%/V |
| Load Regulation | 10\% to 100\% of Rated Current | 0.65 | 0.52 | 3.3 | 0.14 | \% |
| Short-Circuit Current |  | 1.1 | 2.9 | N/A | N/A | A |
| Ripple Voltage at Rated Current | Measured at Rated Current | 40 | 40 | 100* | 20 | mV |
| Transient Response <br> Load Step Settling Time <br> Load Step Undershoot Transient Load Step Overshoot Transient | 10\% to $100 \%$ load $100 \%$ to $10 \%$ load $10 \%$ to $100 \%$ load $100 \%$ to $10 \%$ load | $\begin{gathered} 100 \\ 200 \\ 3.6 \\ 4 \end{gathered}$ | $\begin{gathered} 50 \\ 100 \\ 2.5 \\ 4.2 \end{gathered}$ | $\begin{aligned} & 150 \\ & 150 \\ & 1.3 \\ & 1.2 \end{aligned}$ | $\begin{aligned} & 10 \\ & 80 \\ & 1.0 \\ & 2.7 \end{aligned}$ | $\mu \mathrm{S}$ <br> $\mu \mathrm{S}$ <br> $\%$ <br> $\%$ |
| General |  |  |  |  |  |  |
| PARAMETER | CONDITIONS |  |  |  | TYPICAL | UNITS |
| $\mathrm{V}_{\text {IN }}$ Range | All Outputs in Regulation |  |  |  | 7 to 28 | V |
| Supply Current in Shutdown | All Outputs Shut Down, $\mathrm{V}_{\text {IN }}=15 \mathrm{~V}$ (LTC1439) <br> All Outputs Shut Down, $\mathrm{V}_{\text {IN }}=15 \mathrm{~V}$ (LTC1539) |  |  |  | $\begin{aligned} & 16 \\ & 70 \end{aligned}$ | $\mu \mathrm{A}$ $\mu \mathrm{A}$ |
| Supply Current | All Outputs On, $\mathrm{V}_{\text {IN }}=15 \mathrm{~V}$ <br> All Outputs $0 n, V_{I N}=28 \mathrm{~V}$ |  |  |  | $\begin{aligned} & 450 \\ & 280 \end{aligned}$ | $\mu \mathrm{A}$ |
| Operating Frequency |  |  |  |  | 200 | kHz |

*5V output loaded with 1 A

## PACKAGE DIAGRAM

|  |  |  |
| :---: | :---: | :---: |
| RUN/SS1 1 | 36 PLL LPF | LTC1439CGW LTC1539CGW |
| SENSE ${ }^{+1} 2$ | 35 PLLIN |  |
| SENSE' 1 | 34 boost 1 |  |
| $\mathrm{V}_{\text {Prog } 1} 4$ | 33 TGL1 |  |
| $1_{\text {TH1 }} 5$ | 32 SW 1 |  |
| POR2 6 | 31 TGS1 |  |
| Cosc 7 | 30 VIN |  |
| SGND 8 | 29 BG1 |  |
| LBI 9 | 28 INT V ${ }_{\text {CC }}$ |  |
| LBO 10 | 27 PGND |  |
| SFB1 11 | 26 BG2 |  |
| $1{ }_{\text {TH2 } 2} 12$ | 25 EXTV $V_{C C}$ |  |
| $\mathrm{V}_{\text {PROG2 }} 13$ | 24 TGS2 |  |
| $V_{\text {OSENSE2 }} 11$ | 23 SW2 |  |
| SENSE-2 15 | 22 TGL2 |  |
| SENSE 216 | 21 BOOST2 |  |
| RUN/SS2 17 | 20 AUXON |  |
| AUX DR 18 | 19 AUXFB |  |
| 36-L | SOP |  |

## LTC1439/LTC1539 Pinout

## SCHEMATIC DIAGRAM



## DEMO MANUAL DC106 <br> DESIGN-READY SWITCHERS

PARTS LIST

| REFERENCE DESIGNATOR | QUANTITY | PART NUMBER | DESCRIPTION | VENDOR |
| :---: | :---: | :---: | :---: | :---: |
| C1, C21, C22, C25, C26 | 5 | TPSE226M035R0300 | 224F 35V 20\% Tantalum Capacitor | AVX |
| C2, C6, C10, C13, C15 | 5 | 08055A102MAT1A | 1000pF 50V 20\% NPO Capacitor | AVX |
| C3 | 1 | 08055A560KAT1A | 56pF 50V 10\% NPO Capacitor | AVX |
| C4 | 1 | TPSD336M020R0200 | 334F 20V 20\% Tantalum Capacitor | AVX |
| C5 | 1 | TPSE337M006R0100 | 330 F F 6.3 V 20\% Tantalum Capacitor | AVX |
| C7 | 1 | 08055A471KAT1A | 470pF 50V 10\% NPO Capacitor | AVX |
| C8, C9 | 2 | 08055A221KAT1A | 220pF 50V 10\% NPO Capacitor | AVX |
| C11, C14, C20, C23, C27 | 5 | 08055C104MAT1A | $0.1 \mu \mathrm{~F} 0 \mathrm{~V} 20 \%$ X7R Capacitor | AVX |
| C12 | 1 | 08055C682MAT1A | 6800pF 50V 20\% X7R Capacitor | AVX |
| C16, C19, C28, C29 | 4 | TPSD107M010R0080 | 100 F F 10V 20\% Tantalum Capacitor | AVX |
| C17 | 1 | 08055A220KAT1A | 22pF 50V 10\% NPO Capacitor | AVX |
| C18 | 1 | 08055C103MAT1A | 0.01 ${ }^{\text {F }} 50 \mathrm{~V}$ 20\% X7R Capacitor | AVX |
| C24 | 1 | TAJB475M016R | 4.7 $\mathrm{F}^{\text {F 16V 20\% Tantalum Capacitor }}$ | AVX |
| D1, D3 | 2 | MBRS140T3 | 40V 1A Schottky Diode | Motorola |
| D2, D4, D6 | 3 | CMDSH-3TR | 30V 0.1A Schottky Diode | Central |
| D5, D7 | 2 | MMBD914LT1 | 100V General Diode | Motorola |
| L2 | 1 | CDRH127-100MC | 10 $\mu \mathrm{H} 20 \%$ 7A Inductor | Sumida |
| M1 | 1 | Si9436DY | Dual N-Channel MOSFET | Siliconix |
| M4, M5 | 2 | Si4412DY | N-Channel MOSFET | Siliconix |
| M7 | 1 | IRLL014TR | N-Channel MOSFET | IR |
| Q1 | 1 | MMBT2907ALT1 | 2907A PNP Transistor | Motorola |
| Q2 | 1 | FZT849TA | FZT849TA NPN Transistor | Zetex |
| R1 | 1 | CR21-270J-T | 27 $\Omega$ 1/10W 5\% Chip Resistor | AVX |
| R2, R18, R19 | 3 | CR21-101J-T | 100 1 1/10W 5\% Chip Resistor | AVX |
| R3 | 1 | CR21-1003F-T | 100k 1/10W 1\% Chip Resistor | AVX |
| R4 | 1 | CR21-1132F-T | 11.3k 1/10W 1\% Chip Resistor | AVX |
| R5 | 1 | CR21-472J-T | 4.7k 1/10W 5\% Chip Resistor | AVX |
| R6 | 1 | LR2512-01-R020-F | $0.02 \Omega$ 1W 1\% Chip Resistor | IRC |
| R7 | 1 | CR21-2213F-T | 221k 1/10W 1\% Chip Resistor | AVX |
| R8 | 1 | CR21-3163F-T | 316k 1/10W 1\% Chip Resistor | AVX |
| R9 | 1 | CR21-473J-T | 47k 1/10W 5\% Chip Resistor | AVX |
| R10 | 1 | LR2010-01-R033-F | 0.033 $1 / 2 \mathrm{~W}$ 1\% Chip Resistor | IRC |
| R11, R17, R20, R21 | 4 | CR21-100J-T | 10л 1/10W 5\% Chip Resistor | AVX |
| R12 | 1 | CR21-102J-T | 1k 1/10W 5\% Chip Resistor | AVX |
| R13, R15 | 2 | CR21-103J-T | 10k 1/10W 5\% Chip Resistor | AVX |
| R16 | 1 | CR21-335J-T | 3.3M 1/10W 5\% Chip Resistor | AVX |
| T1 | 1 | LPE-6562-A236; Gapped SMT E-Core | 9.5 $\mu \mathrm{H}$ 3.5A 1:1.42 Inductor | Dale |
| T1 (Alternate Supplier) |  | 501-0655; Gapped SMT Toroid | 9.5uH 3.5A 1:1.41 Inductor | BH Electronics |
| U1 | 1 | LTC1439CGW/LTC1539CGW | LTC1439/LTC1539 36-Pin SSOP IC | LTC |

## mAnUFACTURER TELEPHCG $\in$ DIRECTORY

| MANUFACTURER | USA | EUROPE | JAPAN | HONG KONG | SINGAPORE | TAIWAN |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| AVX | $(207) 282-5111$ | $(0252) 336868$ |  | 3633303 |  |  |
| BH Electronics | $(612) 894-9590$ |  |  |  |  |  |
| Central | $(516) 435-1110$ | 49816143963 |  |  |  |  |
| Dale | $(605) 665-9301$ | 49928771434 |  |  | 657472767 |  |
| IR | $(310) 322-3331$ | 44883713215 |  | $(852) 8037380$ |  |  |
| IRC | $(512) 992-7900$ |  |  |  |  |  |
| Siliconix (TEMIC) | $(408) 970-5700$ | $490713167-0$ |  | $(852) 23-789-789$ |  |  |
| LTC | $(408) 432-1900$ |  |  |  |  |  |
| Motorola | (602) $244-5768$ | 4989921030 |  | $(852) 4808333$ |  |  |
| Sprague | (207) $324-4140$ | 3347540575 |  | $(852) 7979893$ | 654751826 | 88627719582 |
| Sumida | $(708) 956-0666$ |  | 8806688 | 2963388 | $02-726-2177-9$ |  |
| Zetex | (516) $543-7100$ | 44616275105 |  |  |  |  |

## QUICK START GUIDE

This demonstration board is easily set up to evaluate the performance of the LTC1439 or LTC1539. Please follow the procedure outlined below for proper operation.

- Refer to Figure 2 below for board orientation and proper measurement equipment setup.
- Set the three DIP switches, (SW1A, B, and C) to the left position (switches closed).
- Connect the desired loads between the $\mathrm{V}_{\text {OUT1 }}, \mathrm{V}_{\text {OUT2, }}$ $V_{\text {OUT3, }} V_{\text {OUT4 }}$ and their closest PGND terminals on the board. The loads can be up to 3 A for $\mathrm{V}_{\text {OUT1 }}, \mathrm{V}_{\text {OUT2 }}$, and $V_{\text {OUT4; }}$; and 200 mA for $\mathrm{V}_{\text {OUT3 }}$. Soldered wires should be used when the load current exceeds 1A in order to achieve proper testing results.
- Connect the input power supply to the $\mathrm{V}_{\mathrm{IN}}$ and the adjacent PGND terminals at the top of the board. It is safest to start with a voltage less than 6V to verify all of the connections without inadvertently forcing too much voltage on one of the tantalum output capacitors. Once
the output voltage and loading conditions have been verified, it will be safe to increase the input supply to the maximum allowed value of 28V. Do NOT increase $\mathrm{V}_{\text {IN }}$ over 28 V or the MOSFETs MAY BE DAMAGED.
- Switch the desired output(s) on by moving SW1 A, B, or C to the right position ( $5 \mathrm{~V}, 3.3 \mathrm{~V}$, and 2.9 V respectively). The 12 V output will be properly generated when the 5 V output is turned on and when the input supply voltage is a minimum of 7 V . The 2.9 V output can only be produced when the $5 \mathrm{~V}, 3.3 \mathrm{~V}$, and 2.9 V output switches are turned on due to this particular demonstration board design.
- Measure $V_{\text {OUT1 }}, V_{\text {OUT2 }}$ and $V_{\text {OUT4 }}$ to verify output voltages of $5 \mathrm{~V} \pm 0.1 \mathrm{~V}, 3.3 \mathrm{~V} \pm 0.08 \mathrm{~V}$ and $2.9 \mathrm{~V} \pm 0.05 \mathrm{~V}$ respectively at load currents of 1 A each.
- Verify the input supply voltage is at a minimum of 7 V . Measure $\mathrm{V}_{\text {OUT3 }}$ to verify the output voltage of 12 V $\pm 0.6 \mathrm{~V}$ over the allowed load current range of 0 mA to 200 mA .


## operation

The circuit shown in the Schematic Diagram generates 5V, $3.3 \mathrm{~V}, 12 \mathrm{~V}$ and 2.9 V . It provides 5 V at currents up to 3 A . The 2.9 V output is derived from the 3.3 V output using a low dropout linear regulator using the on-chip auxiliary controller. The total current available at the 2.9 V and 3.3 V outputs combined is 6 A with a maximum of 3 A for the 2.9 V output. The 12 V output can deliver up to several hundred milliamps. Figure 2 illustrates the correct measurement setup in order to verify the typical numbers found in the Performance Summary table. The use of small spring-clip leads is very convenient for small-signal bench testing but should not be used at the current and impedance levels associated with this switching regulator. Soldered wire connections are required to properly evaluate the performance of this demonstration board.

In addition to the input and output pins, a 10-pin male connector, J1, allows the user to examine other functions included on the LTC1439/LTC1539 system demonstration board. Three pins, 5V RUN (J1-Pin 9), 3.3V RUN (J1Pin 2) and 2.9V RUN (J1-Pin 3) operate in parallel with the


Figure 2. Proper Measurement Setup
manual switches on the board to allow electronic ON/OFF switching of the voltage outputs.

A power-on reset (POR, J1-Pin6) output can be externally pulled up to an external supply of less than 12 V . The LTC1439 keeps the POR output low in shutdown and for 65536 oscillator clock periods after the first controller's output is within $5 \%$ of its final value. The LTC1539 has the

# DEMO MANUAL DC106 <br> DESIGN-READY SWITCHERS 

## operation

same POR functionality with the exception that the second controller's output is monitored rather than the first.

The Low-Battery Input, (LBI, J1-Pin 5) and the Low-Battery Output, (LBO, J1-Pin 4) are available as connections to a separate comparator. LBI is tied to the noninverting input of the comparator whose other input is tied to the internal $1.19 \mathrm{~V}, 1 \%$ accurate voltage reference. The comparator is active in shutdown (5V RUN and 3.3V RUN inputs low) on the LTC1539 but is shut down on the LTC1439.

The 5V Standby (J1-Pin 7) is also active in shutdown on the LTC1539 but inactive for the LTC1439. This 5V, 4\% accurate standby supply can be very useful in an application which requires power for a "wake-up" function such as a keyboard controller. The cost of leaving these functions alive in the LTC1539 is a typical shutdown current of $70 \mu \mathrm{~A}$, an increase of $50 \mu \mathrm{~A}$ over the LTC1439. The LTC1439 turns off all internal functionality (except for holding POR low) to minimize supply current in shutdown.
The first controller generates the 5 V and 12 V outputs using a $9 \mu \mathrm{H}$ primary and a secondary winding with a turns ratio of $1: 1.42$. The technique used to generate the 12 V is superior to using a simple rectifying diode in terms of regulation accuracy and efficiency. Synchronous MOSFETs M1B and M7 are driven in parallel. The primary output voltage storage capacitor is used to provide power during the synchronous MOSFET's active period by transforming the well-controlled 5 V output by the turns ratio and stacking this output on top of the 5 V output. A well-coupled transformer and low $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ MOSFETs provide an output which is controlled to within $\pm 5 \%$ over all primary and secondary loading conditions. A 12 V secondary output load current is normally limited to an amount less than that which is being drawn from the primary winding. This is not the case with the design here! A secondary feedback input to the first controller senses the 12 V output voltage via a resistive divider, compares this to the internal 1.19 V reference, and forces synchronous MOSFET operation on the primary 5 V controller as required to maintain a minimum output voltage. The resistive divider is set for a value of less than 12 V to guarantee that synchronous operation will only be forced as required by the 12 V load when the primary is unloaded. The demonstration board design sets
this value to be 11.7 V -comfortably below the 12.2 V which is generated during continuous inductor current operation. The secondary winding approach also requires that the synchronous switch have adequate on-time duration as set by the $\mathrm{V}_{\text {IN }} / \mathrm{V}_{\text {OUT }}$ voltage ratio for the primary regulator. This particular design requires approximately 7 V minimum input voltage to properly generate the 12 V at its maximum rated load. A secondary winding from a 3.3V output would work down to 5.4 V input but would be slightly less efficient and accurate. The design does not use the Adaptive Power ${ }^{\text {TM }}$ mode to prevent a higher secondary output voltage generated due to the increased voltage across the primary when the Schottky rectifier, D1, is conducting. Foldback current limit is provided by D5 to protect the bottom MOSFET from overheating during short-circuit conditions.

The 3.3 V output uses a $10 \mu \mathrm{H}$ inductor and a $0.02 \Omega$ sense resistor to provide up to 6 A for the combined 3.3 V and 2.9 V loads. R20, R21, C10 and C9 provide HF decoupling from the output for the current and voltage sensing of the output. The loop compensation components have been optimized for the higher current output level and the transient response performance. A slightly larger inductor can be substituted in order to reduce the ripple current requirements on the input and output capacitors. Foldback current limit is provided by D7 and R12 to protect the bottom MOSFET from overheating during short-circuit conditions.

The 2.9 V output is generated from the 3.3 V output using an internal auxiliary regulator controller. The significant base current required by the output NPN pass device, Q2, is taken from the 5 V switcher output. This approach provides a reasonably efficient, high performance linear regulator solution for Intel P54LM applications. The output accuracy is set by the internal, $1 \%$ accurate reference and an external resistive divider. The external divider allows flexibility in output voltage as well as remote voltage sensing, a requirement in high current applications. While additional low ESR capacitance is required at the load in order to capitalize on the full performance potential of the regulator, care must be taken to make sure that the overall loop is stable. Additional suggestions for stability include: a resistor in series with C12 to provide a

## operation

zero in the forward response to reduce phase shift at high frequencies ( $50 \Omega$ to $500 \Omega$ ); changing the value of feedforward capacitor, C 17 ( 5 pF to 50 pF ), to minimize any peaking in the fed-back response; and increasing R1 ( $20 \Omega$ to $100 \Omega$ ) to reduce the open-loop gain of the amplifier (making sure Q1 can still provide enough base current for Q2). $500 \mu \mathrm{~F}$ of low ESR tantalum capacitance is recommended for CPU power applications. Extremely low ESR ceramic capacitors are not recommended due to the particular NPN emitter follower output stage design.
The power to drive the output power MOSFETs is taken from the IC's INT $V_{\text {CC }}$ pin. The voltage at this pin is normally derived from the $\mathrm{V}_{\text {IN }}$ supply using an internal, low dropout linear regulator. The power MOSFET's gate currents alone can be in the range of 0 mA to 50 mA depending upon the oscillator frequency, the MOSFETs used and the particular output loading condition. The "gate charge" current times the voltage drop between VIN and the INT $V_{C C}$ output voltage can result in significant power loss and thermal demands upon the IC. It is for this reason that an additional input pin, EXT $\mathrm{V}_{\text {CC }}$, is provided. When the voltage applied to the EXTV $V_{C C}$ pin is greater than 4.8 V the internal regulator is turned off and an internal switch is closed between the INT $V_{C C}$ and EXT $V_{C C}$ pins. The current normally delivered by the INT V $C$ S supply is now provided by the voltage source applied to the EXT V $\mathrm{CC}_{C}$ pin. Efficiency and thermal dissipation are improved significantly. The 5V output of the IC's switching controller or another external supply of 5 V to 9 V can be used to provide the EXT V ${ }_{\text {CC }}$ power. Connecting the EXT $V_{\text {CC }}$ pin to the 5 V switcher output takes full advantage of the high efficiency of the DC/DC converter and reduces the IC's required thermal dissipation, truly a win-win situation! At high input voltage using large output MOSFETs, this may be the only way to stay within the worst-case IC package power dissipation limits.

An uncommitted comparator referenced to 1.19 V is available at terminals $\mathrm{J} 1-\mathrm{P} 4$ and $\mathrm{J} 1-\mathrm{P} 5$, and an open-drain power-on reset output for channel 2 for the LTC1439 (channel 1 for the LTC1539) is available at terminal J1-P6. Refer to the LTC1439 and LTC1539 data sheets for further information on these functions.

## LTC1439 AND LTC1539 EFFICIENCY MEASUREMENT

The measurement of efficiency depends upon the operating conditions of all four regulators so care and thought must be given when doing so. Efficiency figures ideally should be taken with only the minimum required circuitry operating on an individual regulator. Since there is much common circuitry operating when more than one regulator is running, overall efficiency numbers will actually increase when the two switching regulators are active. The increase is not significant at high output currents, but can become very significant at low output currents when the IC supply current becomes an appreciable part of the total system supply current.

## IC FUNCTIONAL DESCRIPTION

The LTC1439/LTC1539 switching regulators accomplish high efficiency DC/DC voltage conversion while maintaining constant frequency using a current mode architecture. The externally adjustable free-running oscillator frequency can be phase-locked to an external input, or it can be logically switched using the PLL FLTR pin. High efficiency, maintained at lower currents even when operating at constant frequency, is made possible by using a new Adaptive Power architecture employing two automatically switched output stages. The high current output stage uses a better-than-90\% efficient synchronous regulator with the ability to disable the synchronous MOSFET during each period if the current in the output inductor (transformer) reverses. The low current output stage uses a constant frequency nonsynchronous switch technique using a second, smaller switching MOSFET. Adaptive Power operation is featured in demonstration circuit DC096B.

Adaptive Power operation is not employed in the DC106B circuit, rather, the smaller MOSFET is eliminated, resulting in Burst Mode ${ }^{\text {TM }}$ operation. Subharmonics of the oscillator switching frequency will be present at low current levels, and an assessment needs to be made as to any potential interference problems.

## DEMO MANUAL DC106 <br> DESIGN-READY SWITCHERS

PCB LAYOUT AnD FILm all as viewed from topside.


Top Silkscreen


Top Copper Layer


Third Copper Layer


Bottom Silkscreen


PGND-SGND Ground Plane


Bottom Copper Layer

