# $\mathcal{C Y}$ LIMER 

## DESCRIPTIOn

Logic and computing devices draw more current as supply voltages continue to drop. Using a linear regulator to generate the required voltage is inefficient at high currents. The LTC ${ }^{\circledR} 1628$ dual, current mode, PolyPhase ${ }^{\text {TM }}$ controller is capable of driving two synchronous buck converters 180 degrees out of phase to obtain two high current outputs. Because of input ripple current cancellation, the size and cost of the input capacitors is much smaller than in a single-phase configuration. This results in a dramatic reduction in the number of input capacitors required.

Demo board DC271 is designed to provide a maximum output current of 12A per main output. The input voltage range is 5 V to 24 V and the typical output voltages are 5 V and 3.3 V or lower. If an external, low power, 5 V supply is available, the main input voltage of DC271 can be below 5 V , for example, 3.3 V . The maximum input voltage can also be increased to beyond 24 V if 30 V capacitors are used for input filtering. With an overwinding on the buck inductor, a third low power voltage output, typically 12V, can

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## TYPICAL PGRFORMANCE CHARACTERISTICS AND BOARD PHOTO



Figure 1. Measured Efficiency at Different Loads (FCB = 0, Forced Continuous Conduction Mode)

Component Side


## DEMO MANUAL DC271 <br> NO-DESIGN SWITCHER

## DESCRIPTIO

also be obtained. This demo board always supplies 3.3V at 10 mA . If the input voltage is higher than 6 V , the power supply also provides a 5 V low power output. To facilitate the evaluation of different MOSFETs and capacitors, the layout of DC271 allows the use of MOSFETs inS0-8, DPAK
or D2PAK, and OS-CON, tantalum or multilayer ceramic input and output capacitors. The output is easily configured for different voltages. Test results are presented for outputs of 5 V and 3.3 V with a 12 V input. Gerber files for this circuit board are available. Contact the LTC factory.

## PERFORMANCE SUMmARY

| PARAMETER |  | CONDITIONS | VALUE |
| :---: | :---: | :---: | :---: |
| Input Voltage |  |  | 5 V to 24V |
| Output Voltages |  |  | 0.8 V to 5 V (Configured for 5V, 3.3V) |
|  |  |  | 0.8V to 5V (Configured for 3.3V, 2.5V) |
|  |  | Standby | $3.3 \mathrm{~V} \pm 0.15 \mathrm{~V}$ |
|  |  | $\mathrm{V}_{\text {IN }}>6 \mathrm{~V}$, Standby | $5 \mathrm{~V} \pm 0.2 \mathrm{~V}$ |
|  |  | Auxiliary | Optional Overwinding Output |
| Output Currents | $V_{01}$ | Maximum, Room Temperature | 12A Max for $5 \mathrm{~V}_{\text {OUT }}$ and $3.3 \mathrm{~V}_{\text {OUT }}$ |
|  | $\mathrm{V}_{02}$ |  | 12A Max for 3.3V OUt, 15A Max for 2.5V $\mathrm{VOUT}^{\text {O }}$ |
|  | $\mathrm{INTV}_{\text {cc }}$ |  | 10mA Max |
|  | 3.3V ${ }_{\text {OUT }}$ |  | 10mA Max |
|  | AUXOUT |  | Optional Overwinding Output |
| Load Regulation of $\mathrm{V}_{01}$ and $\mathrm{V}_{02}$ |  | Zero to Full Load | <20mV |
| Output Ripple at $\mathrm{V}_{01}$ and $\mathrm{V}_{02}$ |  | Full Load, Peak-to-Peak, $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}$ | <60mV P-p Typ |
| Transient Response at $\mathrm{V}_{01}$ and $\mathrm{V}_{02}$ |  | Load Switch Between 5A and 10A, $50 \mu \mathrm{~s}$ Rise and Fall Time, $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}$ | < 70mV Peak Typ |
| Efficiency |  | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}$, Room Temperature | 93\% for 5V $\mathrm{V}_{\text {Out }} 12 \mathrm{~A}$ |
|  |  | $90 \%$ for $3.3 \mathrm{~V}_{\text {OUT }} 12 \mathrm{~A}$ |
|  |  | $87 \%$ for $2.5 \mathrm{~V}_{\text {OUT }} 15 \mathrm{~A}$ |

## PACKAGE DIAGRAM



SCHEMATIC DIAGRAM

Figure 2. LTC1628 Dual-Phase Multioutput High Current Converter Schematic

## DEMO MANUAL DC271

NO-DESIGN SWITCHER
PARTS LIST

| REFERENCE DESIGNATOR | QUANTITY | PART NUMBER | DESCRIPTION | VENDOR | TELEPHONE |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C1, C7, C32 | 3 | 08055C102MAT1A | 1000pF 50V X7R Capacitor | AVX | (843) 946-0362 |
| C2, C5, C6, C9, C21, C37, C41, C42 | 8 | 0805ZC105KAT1A | $1 \mu \mathrm{~F}$ 10V X7R Capacitor | AVX | (843) 946-0362 |
| C3 | 1 | TAJB155M035 CASE-A | $1.5 \mu \mathrm{~F} 16 \mathrm{~V}$ Tantalum Capacitor | AVX | (207) 282-5111 |
| C4, C18, C20, C26 | 4 | 0805YC104MAT1A | 0.1 $\mu \mathrm{F}$ 16V X7R Capacitor | AVX | (843) 946-0362 |
| C8, C38, C39, C40 | 4 | 08055C103KAT1A | $0.1 \mu \mathrm{~F} 50 \mathrm{~V}$ X7R Capacitor | AVX | (843) 946-0362 |
| C10, C11, C44 | 3 | 25SP56M CODE F | $56 \mu \mathrm{~F} 25 \mathrm{~V}$ Electrolytic Capacitor | Sanyo | (619) 661-6835 |
| C12, C19 | 2 | EMK107F474ZA | $0.47 \mu \mathrm{~F} 16 \mathrm{~V}$ Y5V Capacitor | Taiyo Yuden | (408) 573-4150 |
| C13, C14, C15, C22, C23, C24 | 6 | T510X477K006AS CASE-D | 470 $\mu \mathrm{F}$ 6.3V Tantalum Capacitor | Kemet | (408) 986-0424 |
| C16 | 1 | T494A226M010AS CASE-A | $22 \mu \mathrm{~F}$ 10V Tantalum Capacitor | Kemet | (408) 986-0424 |
| C17 | 1 | 1206YG225ZAT 1026 | $2.2 \mu \mathrm{~F} 16 \mathrm{~V}$ Y5V Capacitor | AVX | (843) 946-0362 |
| C25, C31, C33, C34 | 4 | 08055A471MAT1A | 470pF 50V NPO Capacitor | AVX | (843) 946-0362 |
| C27, C29 | 2 | 08055C682MAT1A | 6800pF 50V X7R Capacitor | AVX | (843) 946-0362 |
| C28, C30 | 2 | 08055A101MAT1A | 100pF 50V NPO Capacitor | AVX | (843) 946-0362 |
| C35, C36 | 2 | LMK325BJ106MN 1210 | 10رF 10V Ceramic Capacitor | Taiyo Yuden | (408) 573-4150 |
| C43, C45 to C58 | 0 |  | Optional |  |  |
| D1 | 1 | BAT54CTA SOT-23 | Diode Switchmode Rectifier | Zetex | (631) 543-7100 |
| D2 | 1 | BAT54TA SOT-23 | Diode Switchmode Rectifier | Zetex | (631) 543-7100 |
| D3 | 1 | BAT54ATA S0T-23 | Diode Switchmode Rectifier | Zetex | (631) 543-7100 |
| D4, D5 | 2 | MBRS340 SMC | 40V, 3A Schottky Diode | Fairchild | (408) 822-2126 |
| E1 to E18 | 18 | 2501-2 PAD. 092 | Turret Pad | MILL-MAX | (516) 922-6000 |
| J1 to J6 | 6 | KFH-032-10 | Test Pin Stud | PEM |  |
| J1 to J6 | 6 | \#10-32 | Brass Nut | Any |  |
| J1 to J6 | 0 | \#10 | Lug Ring | Keystone | (718) 956-8900 |
| J1 to J6 | 0 | \#10 | Tin Plated Brass Washer | Any |  |
| JP1, JP2, JP3, JP6, JP7 | 5 | 2802S-03-G1 | 3-Pin 1 Row 0.079"cc Header | Comm-Con | (626) 301-4200 |
| JP1 to JP7 | 7 | CCIJ2MM-138G | 0.079"cc Shunt | Comm-Con | (626) 301-4200 |
| JP4, JP5 | 2 | 2802S-02-G1 | 2-Pin 1Row 0.079"cc Header | Comm-Con | (626) 301-4200 |
| L1, L2 | 2 | CEPH149-1R6MC | $1.6 \mu \mathrm{H}$ SMT Inductor | Sumida | (847) 956-0667 |
| Q1 to Q4, Q6 to Q9 | 8 | FDS6670A | N-Channel MOSFET | Fairchild | (408) 822-2126 |
| R1, R3 | 2 | CR10-105JM 0805 | 1M 1/10W 5\% Chip Resistor | TAD | (714) 255-9123 |
| R2, R4, R22, R25 | 4 | CR10-120JM 0805 | 12, 1/10W 5\% Chip Resistor | TAD | (714) 255-9123 |
| R5, R6, R12, R15, R28, R31 | 0 |  | Optional |  |  |
| R7 | 1 | CR10-5R1JM 0805 | 5.1 $\Omega$ 1/10W 5\% Chip Resistor | TAD | (714) 255-9123 |
| R8, R26, R32 | 3 | CR10-100JM 0805 | 10л 1/10W 5\% Chip Resistor | TAD | (714) 255-9123 |
| R9 | 1 | CR10-103JM 0805 | 10k 1/10W 5\% Chip Resistor | TAD | (800) 508-1521 |
| R10 | 1 | CR10-432JM 0805 | 4.3k 1/10W 5\% Chip Resistor | TAD | (800) 508-1521 |
| R13, R14 | 2 | LRF2512-01-R003-J | 0.003 1 1W 5\% Chip Resistor | IRC | (361) 992-7900 |
| R16, R17 | 1 | CR10-473JM 0805 | 47k 1/10W 5\% Chip Resistor | TAD | (800) 508-1521 |
| R18 | 1 | CR10-1502FM 0805 | 15k 1/10W 1\% Chip Resistor | TAD | (800) 508-1521 |
| R19 | 1 | CR10-3012FM 0805 | 30.1k 1/10W 1\% Chip Resistor | TAD | (800) 508-1521 |
| R20 | 1 | CJ10-0R0JM 0805 | $0 \Omega 1 / 10 \mathrm{~W} 5 \%$ Chip Resistor | TAD | (800) 508-1521 |
| R23, R27 | 2 | CR10-4751FM 0805 | 4.75k 1/10W 1\% Chip Resistor | TAD | (800) 508-1521 |
| R29 | 1 | CR10-3652FM 0805 | 36.5k 1/10W 1\% Chip Resistor | TAD | (800) 508-1521 |
| R30 | 1 | CR10-2492FM 0805 | 24.9k 1/10W 1\% Chip Resistor | TAD | (800) 508-1521 |
| U1 | 1 | LTC1628CG | IC | LTC | (408) 432-1900 |

## ФUICK START GUIDE

The circuit is very simple as far as the basic input and output connections are concerned. However, due to the high current nature of this design, care must be exercised or unreliable results will be obtained. The first consideration is the wire gauge for input and output power connections. The load current of 12 A will require at least 3 strands of AWG 18 wire or equivalent for the output power and ground connections. The input wire size is 1 to 3 strands of AWG 18 or equivalent, depending on the input voltage. There is one pair of connector terminals for the inputs of the DC271 and one pair for each output. It is important that all these connections be tightened and secured before applying power to the circuit.
The lab supply used for the input source of DC271 must be capable of supplying a current estimated at $1.2 \cdot\left(\mathrm{~V}_{01} \cdot I_{01}+\mathrm{V}_{02} \cdot I_{02}\right) / V_{\text {IN }}$. To prevent interaction between the lab supply and the demo board, additional low impedance electrolytic capacitors at the output of the lab supply are recommended. This is particularly important for transient load testing, especially at low input voltages.
Since foldback current limiting is built into the LTC1628, some caution must be exercised when testing the DC271. If a constant-current mode electronic load is used, the initial current must be set to a low value (1A recommended) to bring up the circuit. Otherwise, the circuit may not be able to start because the I-V characteristics of the electronic load will trigger the foldback current limit function within the LTC1628 and, shortly thereafter, the shutdown mechanism. Also, pay attention to the current rating of the electronic load. Some electronic loads cannot provide the rated current when the voltage is 3 V or lower. For low voltage, high current applications, the resistance of the output cables of DC271 must be minimized to obtain the highest possible load current from the electronic load. Older style, Darlington-based electronic loads may not be useful for 3.3 V or lower outputs.

When the input voltage is below 5 V , another 5 V lab supply capable of 500 mA must be used to power the LTC1628. Otherwise, the MOSFETs will not have sufficient gate drive voltage. This lab supply should be connected to the EXTV ${ }_{\text {CC }}$ and SGND terminals on the demo board with a pair of twisted wires. The maximum allowable voltage applied on EXTV ${ }_{C C}$ is 7 V . In this case, turn on the main power supply first before turning on the 5 V supply during start-up.
The remote sense pins, SENSE1 ${ }^{+}$and SENSE2 ${ }^{+}$, should be connected directly to the positive terminal of each output.
Attach the voltmeters directly to the input and output connectors to measure the input voltage and output voltage, respectively. Always use current shunts to measure the output current (and the input current if the input voltage is below 12 V ). Put one in each power path and do not remove either during the efficiency measurements (refer to Figure 3).
Before turning on the circuit, preset the input voltage to the desired voltage and the load to 1A. After the circuit is powered up, increase the load to the desired level.
The maximum current of each output is about 12A. Smaller current sense resistors will allow higher output currents.

The demo board is shipped with the following settings:

| JP1(FCB) | 0 |
| :--- | :--- |
| JP2(STBYMD) | Open |
| JP3(FLTCPL) | INTV $C$ C |
| JP4(V $\left.\mathrm{V}_{02}\right)$ | Open, Configure for 3.3V Output |
| JP5(V $\left.\mathrm{V}_{01}\right)$ | Open, Configure for 5V Output |
| JP6(RUN1) | Open |
| JP7(RUN2) | Open |

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## ФUICK STAßT GUIDE



Figure 3. Test Diagram

## OPGRATION

DC271 receives the input power from $\mathrm{V}_{\text {IN }^{+}}$and $\mathrm{V}_{\text {IN }}{ }^{-}$and supplies load to $\mathrm{V}_{01}{ }^{+}$and $\mathrm{V}_{01}{ }^{-}, \mathrm{V}_{02}{ }^{+}$and $\mathrm{V}_{02}{ }^{-}$. An external bias supply of 5 V may be connected to EXTV ${ }_{\text {cc }}$ to boost the light load efficiency. If an overwinding is used on the buck inductor (L1) in the $\mathrm{V}_{\text {OUT1 }}$ output circuit, a third output voltage, typically 12 V , may be made available at the AUXOUT $\pm$ terminals. The 3.3 V out pin supplies 3.3 V at 10 mADC and 50 mA PEAK. If the input voltage is above 6 V , the INTV ${ }_{\text {CC }}$ pin will supply a 5 V reference output.

## Configuration of Different Operating Modes

The RUN1 and RUN2 pins can be used for soft-start and run control of $\mathrm{V}_{\text {OUT1 }}$ and $\mathrm{V}_{\text {OUT2 }}$, respectively, depending on the state of the FLTCPL pin. Pulling the RUN pin below 1.3 V will shut down the corresponding output. For normal operation, leave the RUN pins open or connect them to INTV ${ }_{\text {CC. }}$. Soft-start capacitors are included on DC271. For a longer soft-start time, additional capacitance may be connected to the RUN pins. The FCB pin controls the lightload operating modes of the synchronous buck circuits: forced continuous conduction, Burst Mode ${ }^{\text {TM }}$ operation and Burst Mode operation disable. Refer to Table 1 and the

LTC1628 data sheet. The STBYMD pin determines which circuitry remains active when the controllers are shut down and/or provides a common control point to shut down both controllers. Refer to the LTC1628 data sheet for details. The FLTCPL pin determines whether the two controllers operate individually or in combination. See Table 2 for details.

Table 1. Low Current Operating Modes

| FCB | $<0.8 \mathrm{~V}$ | 0.8 V to INTV $_{\text {CC }}-0.5 \mathrm{~V}$ | INTV $_{\text {CC }}$ |
| :--- | :--- | :--- | :--- |
| Low Current | Continuous | Burst Mode | Burst Mode |
| Operating | Conduction | Operation | Operation Disable |
| Mode | Mode |  | (Discontinuous <br> Conduction Mode) |

## Frequency Setting

Applying a different voltage on the FREQ pin can alter the switching frequency. Refer to the LTC1628 data sheet for details. R10 on the schematic diagram (Figure 2) can be varied to obtain the desired switching frequency. The suggested values are from 0 k to 5.6 k , corresponding to a frequency range of 150 kHz to 300 kHz .
Burst Mode is a trademark of Linear Technology Corporation

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## OPERATION

Table 2. Fault Coupling Pin

| FLTCPL | $\mathbf{0}$ | INTV $_{\text {CC }}$ |
| :--- | :--- | :--- |
| Relationship <br> Between <br> Two Controllers | Two Controllers <br> Operate Individually | Two Controllers <br> Operate in Combination |
| FCB | Only Applies <br> on Controller 1 | Applies on Both <br> Controllers |
| Overcurrent <br> Latch Off | Only Latch Off the <br> Controller Having the <br> Overcurrent Condition | Latch Off Both Controllers <br> When Either Has an <br> Overcurrent Condition |

## Output Voltage Setting

JP4 and JP5 can be used to set different output voltages.
Table 3. Output Voltage Settings

| Output Voltages | Jumpers | Open | Closed |
| :--- | :---: | :---: | :---: |
| $V_{01}$ | JP5 | 5 V | 3.3 V |
| $V_{02}$ | JP4 | 3.3 V | 2.5 V |

R18 and R30 on the schematic can be changed to obtain the desired output voltage:

$$
\begin{equation*}
\mathrm{R} 30(18)=4.75 \mathrm{k}\left(1.25 \mathrm{~V}_{01(2)}\right)-1 \tag{1}
\end{equation*}
$$

## Sense Resistor

The current sense resistor is selected according to the channel current. The starting resistance value is estimated to be

$$
\begin{equation*}
\mathrm{R}_{\mathrm{CS}}=\frac{\mathrm{V}_{\mathrm{SENSE}(\mathrm{MAX})}}{\left(\mathrm{l}_{\mathrm{LDC}}+\Delta \mathrm{l}_{\mathrm{L} / 2}\right)} \tag{2}
\end{equation*}
$$

where $I_{L D C}$ is the maximum $D C$ inductor current, $\Delta l_{L}$ is the maximum peak-to-peak inductor ripple current and $V_{\text {SENSE(MAX) }}$ is the maximum current sense threshold at the operating duty cycle. Refer to the LTC1628 data sheet for the plot of "Maximum Current Sense Threshold vs Duty Factor." The power rating can be estimated to be
$P_{C S}=\left(\operatorname{lLDC}^{2}+\frac{1}{12} \Delta l_{L}^{2}\right) R_{C S}$
The final sense resistor value may be varied based on current limit requirement.

## MOSFETs

The selection of MOSFETs is determined by the output current, input voltage and switching frequency. Low $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ MOSFETs are usually used for high current output applications because they reduce conduction loss; however they also tend to introduce high switching-related losses at high switching frequencies because of the large gate charge and parasitic capacitances. For a given current requirement and selected switching frequency, both $R_{D S(O N)}$ and gate charge $\left(Q_{G}\right)$ should be evaluated to minimize the sum of the conduction losses, driving losses and switching loss. For a high input voltage, the high dV/dt applied on the Miller capacitance of the bottom MOSFET may cause false turn-on of the bottom MOSFET when the top MOSFET turns on. The resulting shootthrough current may damage the top MOSFET. Therefore, MOSFETs with a low ratio of Miller capacitance charge to the prethreshold gate charge should be used for the bottom switches.

For the specified applications, a number of MOSFETs can be good choices: Si4410, Si4420, Si4884 and Si4874 (Siliconix), FDS6680A and FDS6670A (Fairchild) and IRF7807, IRF7811, IRF7805 and IRF7809 (International Rectifier) may be used.

In the breadboard tests, two FDS6670s were used for the top switch and two FDS6670As were used for the bottom switch. One catch diode (MBRS340T3) was used for each buck circuit to bypass the body diode of the bottom MOSFET during the switching transitions. The purpose of this catch diode is to minimize the conduction loss and the reverse recovery losses related to the MOSFET body diode.

## Inductors

The selection of inductors is driven by the load current amplitude and the switching frequency. The LTC1628 senses the inductor current with a low value current sense resistor. Therefore, the inductor ripple current must be large enough to produce a reasonable AC sense voltage. It is estimated that an inductor value of around $1.5 \mu \mathrm{H}$ will be suitable for a 3.3 V or 5 V output at a frequency range between 200 kHz and 300 kHz . A number of off-the-shelf

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## operation

surface mount inductors are available for the specified applications: P1608, PE53691 (Pulse Engineering), ETQP6F1R3L (Panasonic) and CEPH149-1R6MC (Sumida). Any inductor of the desired value and current capability should work correctly.

## Capacitors

The selection of the input capacitors is driven by the RMS value of the input ripple current. Large capacitor ripple currents introduce high power losses due to the ESR of the capacitor and tend to reduce the capacitor life. Low ESR capacitors must be used. The layout of the input capacitors on this demo board allows the use of OS-CON capacitors or a combination of multilayer ceramic capacitors and Iow ESR aluminum electrolytic capacitors. The data presented here was obtained with Sanyo OS-CON capacitors (25SP56M $56 \mu \mathrm{~F} / 25 \mathrm{~V}$ ), whose maximum allowable ripple current is rated at about $3.26 A_{\text {RMS }}$. The maximum input RMS ripple current is estimated to be about $8.3 \mathrm{~A}_{\text {RMS }}$ for a 7 V to 24 V input range, 3.3 V (0A to 15 A ) and 5 V ( 0 A to 15 A ) outputs. Therefore, a minimum of 3 OS-CON capacitors are needed. Figure 4 plots the maximum input ripple currents with respect to the input voltage. It is apparent that the conventional single-phase configuration will increase the worst case input ripple current to $13.2 A_{\text {RMS }}$, a $60 \%$ increase. A conventional single-phase controller requires a minimum of five OS-CON capacitors. Hence, the LTC1628 based dualphase circuit saves two OS-CON capacitors.


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Figure 4. Maximum Input Ripple Current vs Input Voltage in a 2-Output Power Supply: 7 V to $24 \mathrm{~V}_{\text {IN }}, 3.3 \mathrm{~V}_{\text {OUt1 }}$ at 0 A to $15 \mathrm{~A}, 5 \mathrm{~V}_{0 \mathrm{OT} 2}$ at 0 A to 15 A

To minimize output switching ripple voltage and meet load transient requirements, low ESR capacitors are usually required on the output. Good candidates for the output capacitor are low ESR tantalum capacitors (Kemet T510, etc.), POSCAPs (Sanyo), OS-CONs (Sanyo) and SPs (Panasonic). A combination of multilayer ceramic capacitors and Iow ESR aluminum electrolytic capacitors is also an option. The layout of DC271 allows the evaluation of all these types of capacitors. Test data was obtained with KEMET (T510X477M006AS 470(F/6.3V), ultralow ESR ( $30 \mathrm{~m} \Omega$ ) surface mount tantalum capacitors. There are three tantalum capacitors on each output. More capacitors (optional) may be added to meet stricter noise and load transient requirements.

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## TEST RESULTS

Figure 5 shows measured waveforms of the switch-node voltages. The two buck stages are interleaved 180 degrees out of phase to reduce the input ripple current.
Efficiency was measured under different loading conditions for each output. The input voltage was measured at the input terminals and the output voltage was measured at the output terminals (refer to test diagram shown in Figure 3). The switching frequency was 250 kHz , the input voltage was 12 V and both channels were operated in forced continuous conduction mode ( $\mathrm{FCB}=0$ ). Figure 1 shows the measured efficiency for three different output voltages. The efficiencies are $93 \%$ for $5 \mathrm{~V} / 12 \mathrm{~A}$ and $90 \%$ for $3.3 \mathrm{~V} / 12 \mathrm{~A}$ output. The light load efficiencies can be improved by enabling Burst Mode operation.


Figure 5. Typical Waveforms of Switch-Node Voltages (Drain-to-Source Voltage of Synchronous Switch)

Load transient testing was also performed with the load switching between 5A and 10A for each output. The rise and fall times were $50 \mu \mathrm{~s}$. Test results are shown in Figures 6 a and 6 b . Both the overshoot and undershoot are
below 60 mV for the 3.3 V output and around 70 mV for the 5 V output. For load steps with very high di/dt, larger output capacitors with lower ESR would be required. The demo board allows the installation of additional output capacitors to meet more stringent load transient requirements.

(a) 3.3V Output Voltage

(b) 5V Output Voltage

Figure 6. Load Transient Response Waveforms with Load Switching between 5 A and 10A. Voltage Scale: $50 \mathrm{mV} / \mathrm{DIV}$, Time Scale: 500 $\mathrm{Hs} / \mathrm{DIV}$

## PCB LAYOUT AND FILm



Paste Mask Top


Solder Mask Top


Solder Mask Bottom

## PCß LAYOUT AnD film



Copper Layer 1 (Top)


Copper Layer 3


Copper Layer 2


Copper Layer 4 (Bottom)

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## PC FAB DRAWING



