# DEMO BOARD MENU DC302

# QUICK START GUIDE

## 1 DESCRIPTION

DC302 is a VRM for powering mobile CPU. It has two inputs (7.5-24V, and 3.3V) and three outputs (Vcc-cpu-core at 15Amax, Vcc-cpu-IO at 2.5Amax, and Vcc-cpu-CLK at 1.5Amax). It is recommended that this demo board be evaluated on demo board DC296A, which provides the input, output and control interfaces for the VRM. DC296A is also equipped with the dynamic load tester, which allows the user to program the load step amplitude. Refer to DC296 demo board menu for more information.

DC302 adopts LTC1708PG to provide core and IO supplies. Each LTC1708 is capable of regulating two out-of-phase synchronous buck circuits. The 2-phase technique minimizes the input ripple current, and therefore, reducing the size of input capacitors and extending battery life. Unlike other designs using low efficiency LDO to generate IO supply, this design adopts the synchronous buck circuit to maximize the efficiency. High performance LDO LT1782MS8-2.5 is used to generate 2.5V clock supply from 3.3V input. Tiny MS8 footprint helps minimize the overall footprint of power supply.

## 2 QUICK START GUIDE

The following procedure is recommended for testing DC302.

1. Mount DC302 onto DC296.

2. Connect an adjustable 24V/4A power supply to the +V_IN pin and a 3.3V/0.5A power supply to +V_3 (3.3V) pin on DC296.

3. Connect output loads to the CORE, I/O, and CLK pins. If a constant-current mode electronic load is used for CORE output, preset load current to 0.2A. Otherwise, the I-

V charateristics of electronic load may interfere with the foldback current limit of LTC1708PG and preventing circuits from the normal start-up.

4. Apply input voltage between 7.5V and 24V. CORE output current may increase to full load after the CORE voltage reaches the steady state.

5. To evaluate the efficiency of DC302, it is recommended that the input and output voltages be measured across the input and output capacitors of DC302 directly.

6. The regulation of each output should be tested on DC296 output terminals.

7. To test load transient performances, apply +/-12V supply to the +12V and –12V Pins on DC296. Make sure that no dc load is applied on CORE output before switching SW1 to the ON position. The load step amplitude may be adjusted by dialing potentiometer R6 on DC296. The load step current can be monitored from BNC connector J1.

## 3 TEST RESULTS:

Table 1 shows a typical efficiency results on CPU CORE and IO supplies. The efficiency is measured to be greater than 83% when the CORE supply draws 9.4A at 1.35V and the input voltage is between 10V and 15V. The efficiency can be further improved by powering LTC1708PG from the 5V input and by operating the circuits at lower switching frequencies.

**Table 1 Measured Efficiency**

| Vin (V) | VCC_CPU_CORE (V) | ICC_CPU_CORE (A) | VCC_CPU_IO (V) | ICC_CPU_IO (A) | Efficiency (%) |
|---|---|---|---|---|---|
| 20 | 1.6 | 14.1 | 1.5 | 2.5 | 80% |
| 16 | 1.6 | 14.1 | 1.5 | 2.5 | 82% |
| 15 | 1.35 | 9.4 | 1.5 | 2.5 | 83% |

| | | | | | |
|---|---|---|---|---|---|
| 10 | 1.35 | 9.4 | 1.5 | 2.5 | 85% |

Table 2 shows the load regulation of CORE output. The maximum dc voltage variation against load and line change is less than +30mV/-100mV.

**Table 2 Output Regulation Table (Vin=7.5V~24V)**

| VID4-0 | ICC_CPU_CORE (A) | VCC_CPU_CORE (V) |
|---|---|---|
| 01101 | 0.2 | 1.35V +/-0.01V |
| 01101 | 9.4 | 1.29V +/-0.02V |
| 01000 | 0.2 | 1.60V +/-0.01V |
| 01000 | 14.1 | 1.50V +/-0.02V |

Figure 1 shows the output voltage during a 14A load step transient at Vin=20V, Vo=1.6V. The maximum output voltage variation is less than 120mVp-p. By combining this result with Table 2, the output voltage regulation range under any condition is within the specs.

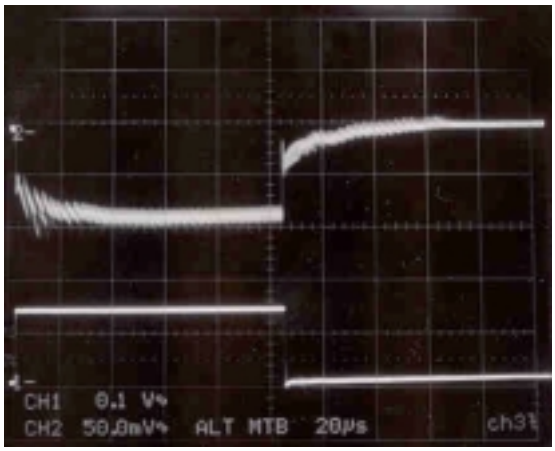


**Figure 1 Load Transient Waveform of Core Output (Vin=20V, Vo=1.6V, Io step: 0.2~14.1A)**

**Top Trace: VCC_CPU_CORE (50mV$_{AC}$/div), Bottom Trace: ICC_CPU_CORE (10A/div), Time Scale: 20us/div**