# LTC1741, LTC1742, LTC1743, LTC1745, LTC1746, LTC1747 or LTC1748

## DESCRIPTION

Demonstration circuit 520 features a family of 12/14 BIT 25 to 80 MSPS ADCs featuring one of the following devices: LTC1741, LTC1742, LTC1743, LTC1745, LTC1746, LTC1747 or LTC1748 high speed, high dynamic range ADCs.

There are several versions of the 520B demo board supporting the LTC174x series of A/D converters listed in Table 1. Depending on the required resolution, sample rate and input frequency, the DC520 is supplied with the appropriate A/D and with an optimized input circuit. The circuitry on the analog inputs is optimized for analog input frequencies above 40MHz or below 40MHz.

Design files for this circuit board are available. Call the LTC factory.



**Table 1. DC520B Variants**

| DC520 VARIANTS | ADC PART NUMBER | RESOLUTION | MAXIMUM SAMPLE RATE | INPUT FREQUENCY |
|---|---|---|---|---|
| 520B-A | LTC1748 | 14-Bit | 80Msps | Ain < 40MHz |
| 520B-B | LTC1748 | 14-Bit | 80Msps | Ain > 40MHz |
| 520B-C | LTC1745 | 12-Bit | 25Msps | Ain < 40MHz |
| 520B-D | LTC1746 | 14-Bit | 25Msps | Ain < 40MHz |
| 520B-E | LTC1747 | 12-Bit | 80Msps | Ain < 40MHz |
| 520B-F | LTC1747 | 12-Bit | 80Msps | Ain > 40MHz |
| 520B-G | LTC1742 | 14-Bit | 65Msps | Ain < 40MHz |
| 520B-H | LTC1742 | 14-Bit | 65Msps | Ain > 40MHz |
| 520B-I | LTC1741 | 12-Bit | 65Msps | Ain < 40MHz |
| 520B-J | LTC1741 | 12-Bit | 65Msps | Ain > 40MHz |
| 520B-K | LTC1743 | 12-Bit | 50Msps | Ain < 40MHz |

**Table 2. Performance Summary ($T_A$ = 25°C)**

| PARAMETER | CONDITION | VALUE |
|---|---|---|
| Minimum Supply Voltage | Depending on sampling rate and the A/D converter provided, this supply must provide up to 400mA. | 4.75V |
| Maximum Supply Voltage | | 5.25V |
| Analog input range | Depending on Sense Pin Voltage | ±1V to ±1.6V |
| Logic Input Voltages | Minimum Logic High | 2.4V |
| | Maximum Logic Low | 0.8V |
| Logic Output Voltage (ALVCH16373 output buffer) | Minimum Logic High @ -12mA | 2.4 |
| | Maximum Logic Low @ 12mA | 0.7 |
| Sampling Frequency (Convert Clock Frequency) | See Table 1 | |
| Convert Clock Level | 50 Ohm Source Impedance, AC coupled or ground referenced (Convert Clock input is transformer coupled on board.) | $2V_{P-P}$ Sine Wave |
| Resolution | See Table 1 | |
| Input frequency range | See Table 1 | |
| SFDR | See Applicable Data Sheet | |
| SNR | See Applicable Data Sheet | |

# QUICK START PROCEDURE

Demonstration circuit 520 is easy to set up to evaluate the performance of any of the LTC174x family of A/D converters - LTC1741, LTC1742, LTC1743, LTC1745, LTC1746, LTC1747 or LTC1748. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

### SETUP

If a DC718 QuickDATS Data Acquisition and Test System was supplied with the DC520 demonstration circuit, follow the DC718 Quick Start Guide to install the required software and for connecting the DC718 to the DC520 and to a PC running Windows98, 2000 or XP.

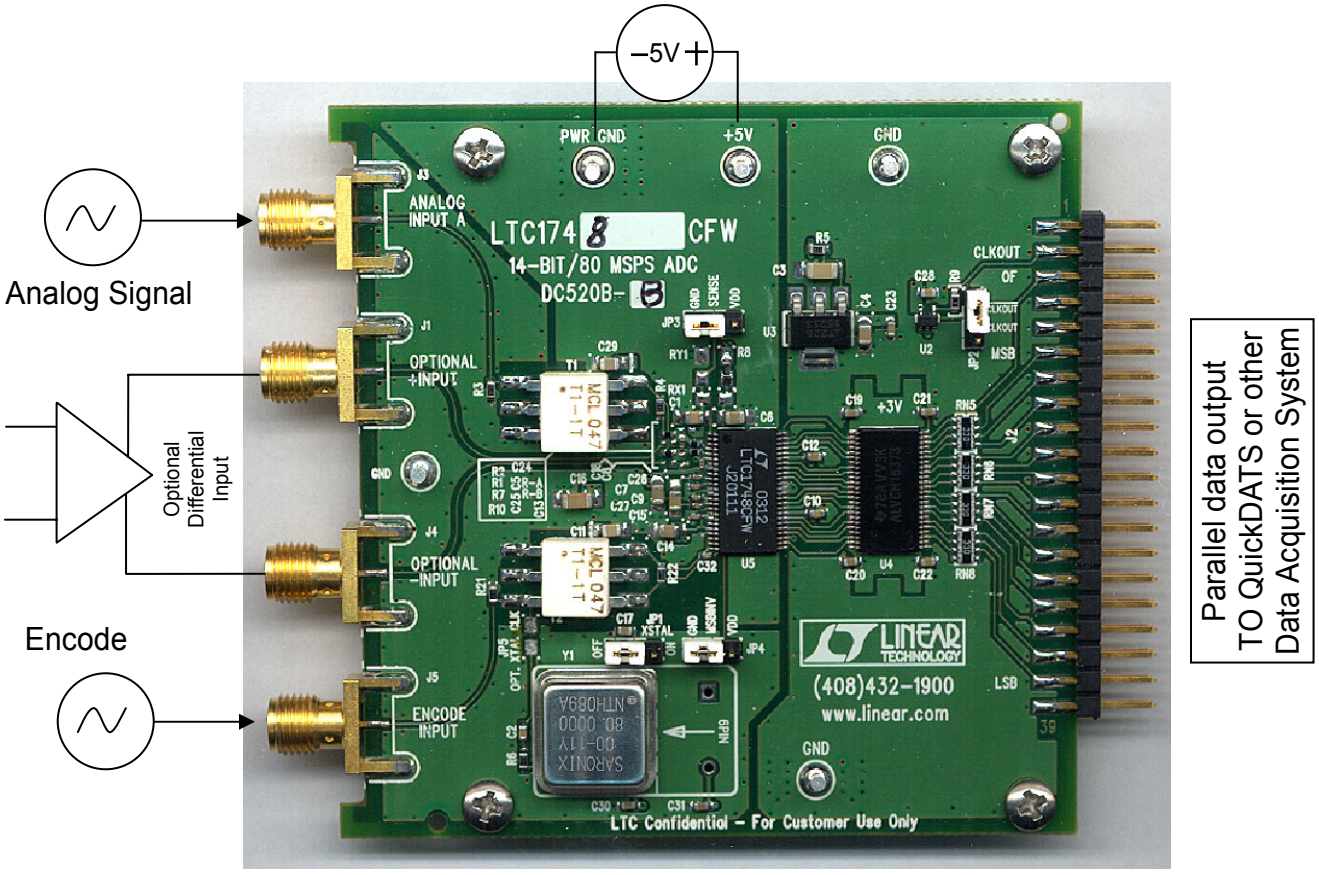



**Figure 1. DC520 Setup**

## DC520 DEMONSTRATION CIRCUIT BOARD JUMPERS

The DC520 demonstration circuit board should have the following jumper settings for use with an external Encode Clock:

JP1: XTAL OFF if using an external clock.

JP2: Set to CLKOUT (not CLKOUT bar for QuickDATS compatibility.)

JP3: SENSE to GND selects the 2Vpp input range
SENSE to VDD selects the 3.2Vpp input range

JP4: Connect MSBINV to GND (For 2's compliment output format for PScope compatibility.)

If you are using the on board crystal oscillator to supply the encode clock:

❑ Disconnect any cable connected to the Encode Input J5.

❑ Set JP1 to ON.

❑ Place a wire jumper across JP5 located between Y1 and T2.

**NOTE:** If the crystal is not disconnected and tri-stated when using an external clock and conversely if an external clock source is connected while using the on board crystal oscillator, large spurs will be present in the FFT.

**APPLYING POWER AND SIGNALS TO THE DC520 DEMONSTRATION CIRCUIT BOARD:**

If a DC718 is used to acquire data from the DC520, the DC718 must FIRST be connected to a powered USB port or provided an external 6-9V BEFORE Applying +5V across the pins marked "+5V" and "PWR GND" on the DC520. The DC520 demonstration circuit requires up to 400mA depending on sampling rate and A/D converter supplied.

The data collection board is powered by the USB cable and does not require an external power supply unless it must be connected to the PC through an un-powered hub in which case it must be supplied an external 6-9V on turrets G7(+) and G1(-) or the adjacent power jack.

**ENCODE CLOCK**

**NOTE: THIS IS NOT A LOGIC LEVEL INPUT**. Apply an encode clock to the SMA connector on the DC520 demonstration circuit board marked "ENCODE INPUT". Refer to Table 2 for recommended level, impedance and coupling. Do not connect to a signal source with a DC offset. This input is connected to ground through the primary of transformer T2. For the very best noise performance, the ENCODE INPUT must be driven with a very low jitter source. When using a sinusoidal generator, the amplitude should be as large as possible, up to $2V_{P-P}$. Using band pass filters on the clock and the analog input will improve the noise performance.

Apply the analog input signal of interest to the SMA connector on the DC520 demonstration circuit board marked "ANALOG INPUT A". Do not connect to a signal source with a DC offset. This input is connected to ground through the primary of transformer T1. Optional direct differential inputs are provided via J1 and J4. To use the optional differential inputs requires removing and adding several components on the DC520. Refer to the DC520 schematic for further information.

At this point a conversion clock output is available on pin 3 of J2 and Data samples are available on Pins 11-37 for 14 BITS or (15-37 for 12 BITS) which can be collected via a logic analyzer, cabled to a development system through a SHORT 2 to 4 inch long 40 pin ribbon cable or collected by the DC718 QuickDATS using the *DATS System Software* provided or down loaded from the Linear Technology Corporation website at http://www.linear.com/software/. If a DC718 was provided, follow the DC718 Quick Start Guide and the instructions below.

To start the data collection software if "*PScope.exe*", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

Configure PScope for the appropriate variant of the DC520 demonstration circuit by selecting the correct A/D Converter as installed on the DC520. Under the "Configure" menu, go to "Device." Under the "Device" pull down menu, select device, either LTC 1741, LTC 1742, LTC 1743, LTC 1745, LTC 1746, LTC1747 or LTC1748.

If everything is hooked up properly, powered and a suitable convert clock is present pressing the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for *PScope* is available in the DC718 Quick Start Guide and in the online help available within the *PScope* program itself.

## ANALOG INPUT NETWORK

For optimal distortion and noise performance the RC network on the analog inputs are optimized for the analog input frequency on the different versions of the DC520. For input frequencies below about 40 MHz, the circuit in Fig. 2 is recommended (this is installed on DC520 versions A,C,D,E,G,I,K). For input frequencies above 40MHz and below 80MHz, the circuit in Fig. 3 is recommended (this is installed on versions B, F, H, J).

For input frequencies above 80MHz, the circuit in Fig. 4 is recommended. This circuit requires a different coupling transformer for T1. Please contact the Linear Technology Applications Department if you would like a DC520 demonstration circuit board with this circuit installed.

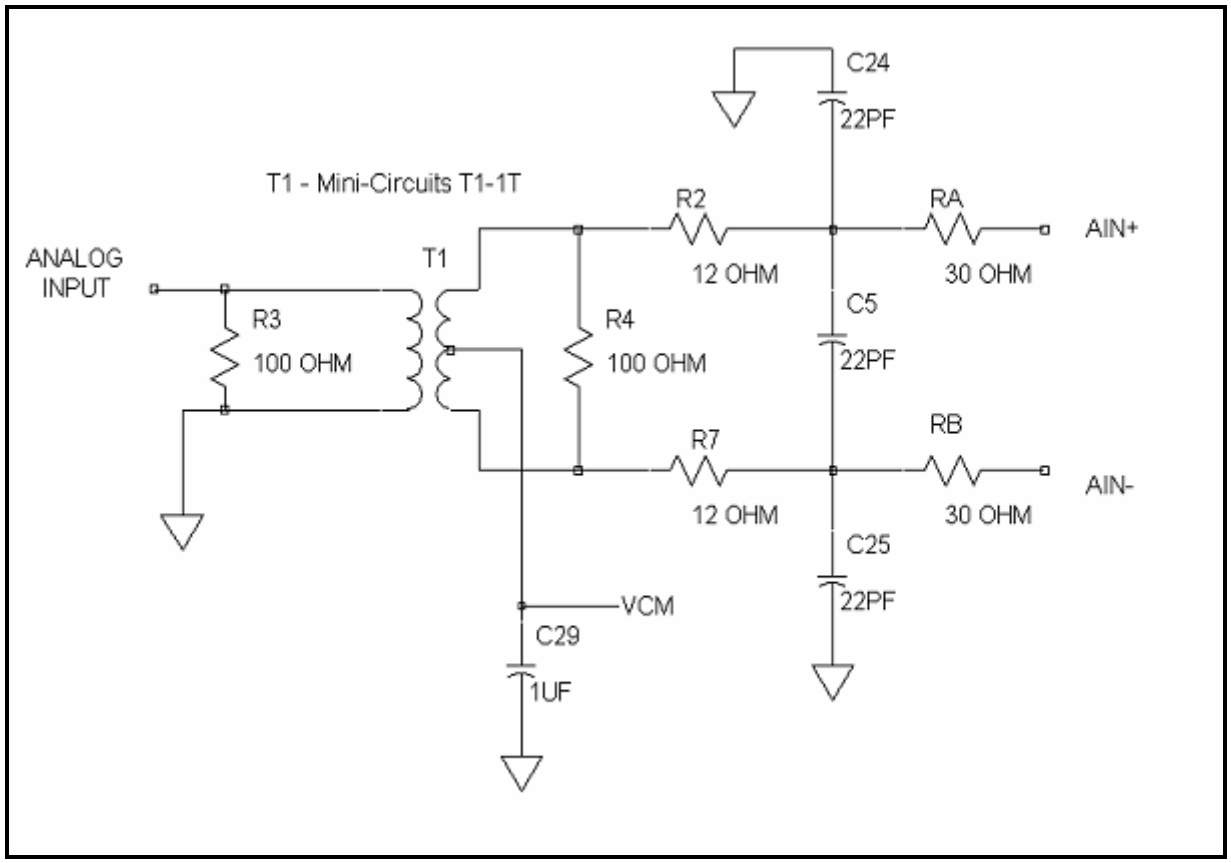



**Figure 2. Analog Front End Circuit For $A_{IN}$ < 40MHz**

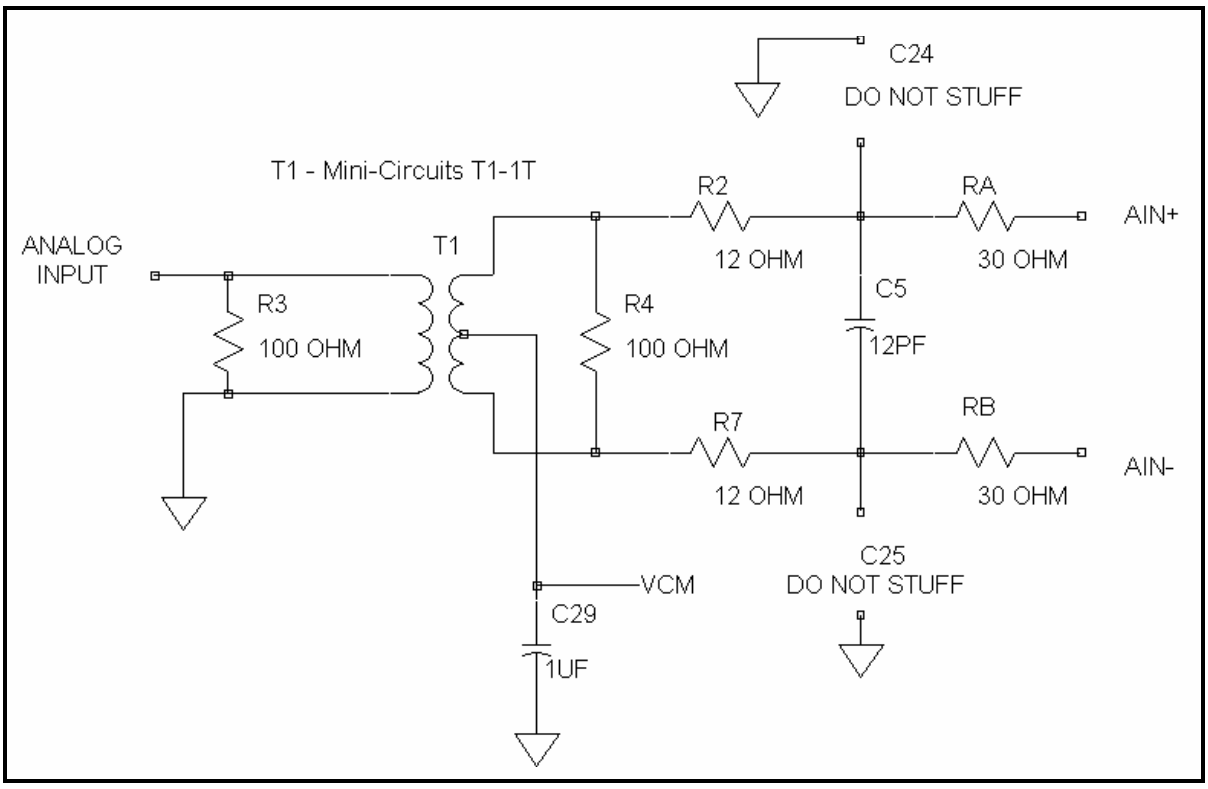



**Figure 3. Analog Front End Circuit For 40MHz < $A_{IN}$ < 80MHz**

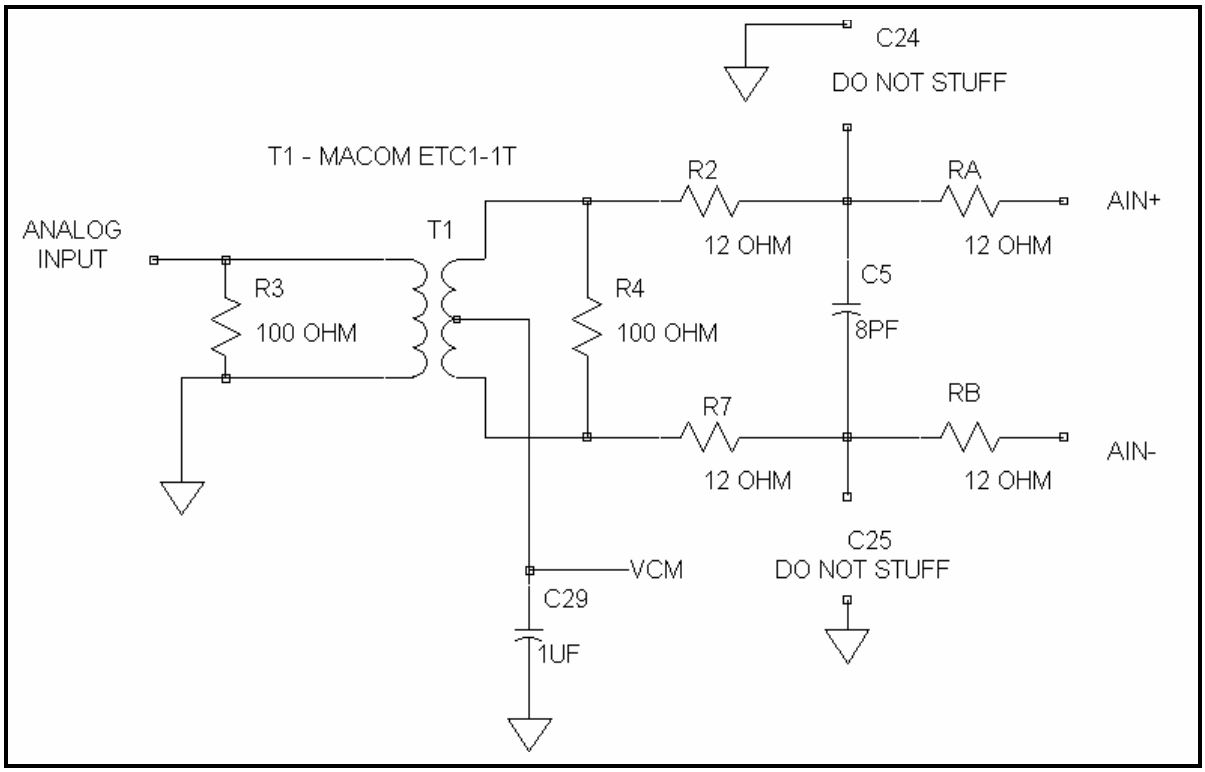
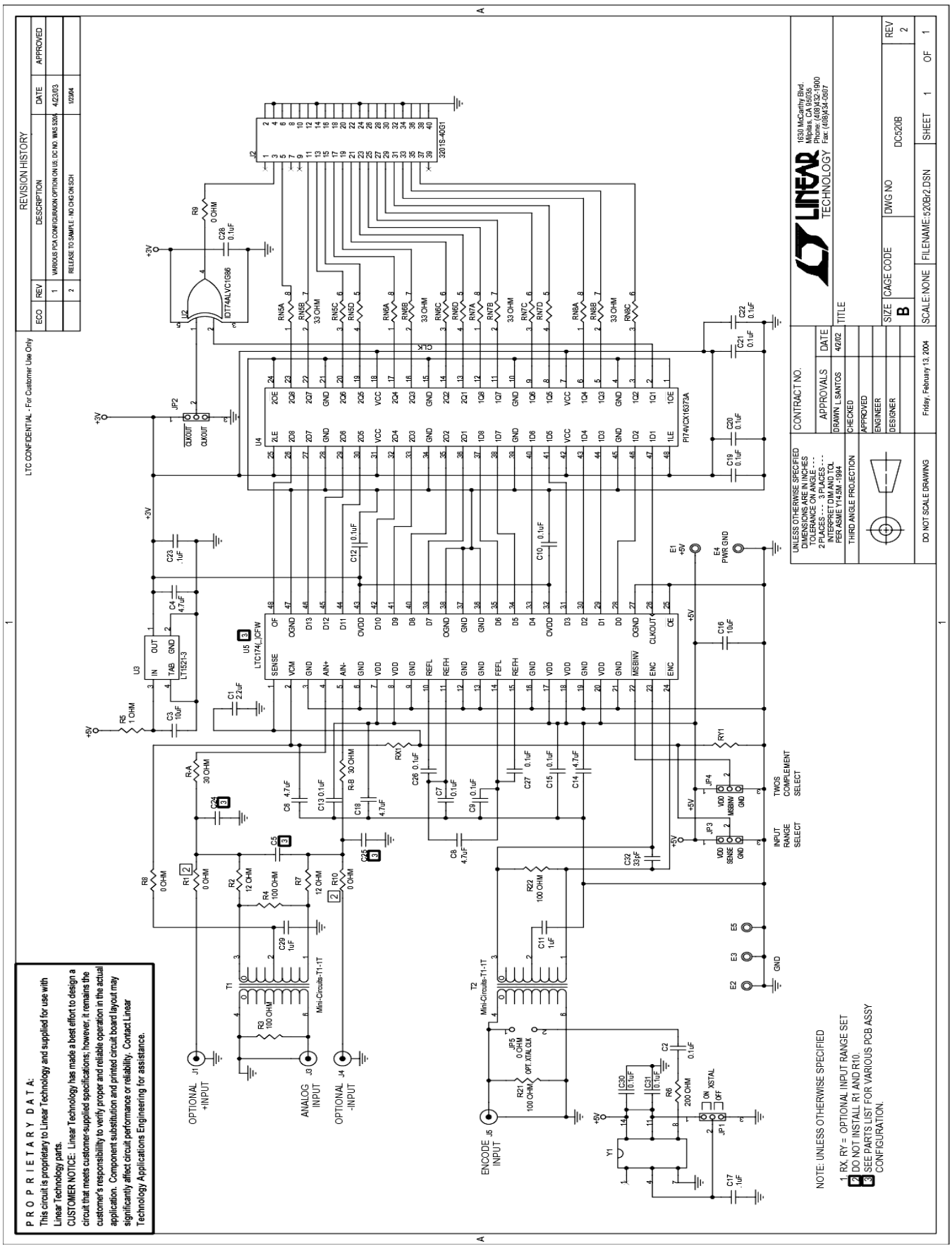



**Figure 4. Analog Front End Circuit For $A_{IN}$ > 80MHz**


LTC CONFIDENTIAL - For Customer Use Only
REVISION HISTORY
ECO REV DESCRIPTION DATE APPROVED
1 VARIOUS PCA CONFIGURATION OPTION ON US, DC NO. WAS 520A 4/23/03
2 RELEASE TO SAMPLE - NO CHG ON SCH 1/23/04
PROPRIETARY DATA:
This circuit is proprietary to Linear Technology and supplied for use with Linear Technology parts.
CUSTOMER NOTICE: Linear Technology has made a best effort to design a circuit that meets customer-supplied specifications; however, it remains the customer's responsibility to verify proper and reliable operation in the actual application. Component substitution and printed circuit board layout may significantly affect circuit performance or reliability. Contact Linear Technology Applications Engineering for assistance.
NOTE: UNLESS OTHERWISE SPECIFIED
1 RX, RY = OPTIONAL INPUT RANGE SET
2 DO NOT INSTALL R1 AND R10.
3 SEE PARTS LIST FOR VARIOUS PCB ASSY CONFIGURATION.
OPTIONAL +INPUT
ANALOG INPUT
OPTIONAL -INPUT
ENCODE INPUT
CLKOUT
INPUT RANGE SELECT
TWOS COMPLEMENT SELECT
LINEAR TECHNOLOGY
1630 McCarthy Blvd.
Milpitas, CA 95035
Phone: (408)432-1900
Fax: (408)434-0507
CONTRACT NO.
APPROVALS DATE
DRAWN L SANTOS 4/2/02
CHECKED
APPROVED
ENGINEER
DESIGNER
TITLE
SIZE B
CAGE CODE
DWG NO DC520B
REV 2
SCALE:NONE
FILENAME:520Brf2.DSN
SHEET 1 OF 1
DO NOT SCALE DRAWING
Friday, February 13, 2004