High Performance Switch Mode Power Solutions for Altera Low Voltage FPGAs

by Mike Shriver

INTRODUCTION

The core voltages for FPGAs are moving lower as a result of advances in the fabrication process. The newest FPGA family from Altera, the Stratix® II, now requires a core voltage of 1.2V and the Stratix, Stratix GX, HardCopy® Stratix and Cyclone™ families require a core voltage of 1.5V. This article discusses how to power the core and I/O of low voltage FPGAs using the latest step-down switch mode controllers from Linear Technology Corporation.

To ensure correct selection of power management circuitry, it is recommended to use Altera's PowerPlay Power Estimation Tools to obtain accurate results. Tools are available to help determine power consumption before and during the design process. More information on these tools is available from Altera's website: http://www.altera.com/support/devices/estimator/pow-powerplay.html.

Overview

The load and input voltage requirements for FPGA systems vary considerably. A single FPGA typically requires less than 2A, but for systems using multiple FPGAs, the load requirements can go to 10A or higher. Since power must be applied to the core and I/O, more than one rail is often required. Combinations of 1.2V and higher voltages such as 1.5V, 1.8V, 2.5V and 3.3V might be encountered. The input voltage requirements vary as well. The system designer may be inclined to step down from an input voltage such as 12V for high output current systems to reduce the I^2R losses in the PCB traces, connector and cabling. For low output current levels, an input voltage of 5V or lower may be used. The regulators shown in Table 1 cover a wide variety of output current and input voltage levels often encountered in low voltage FPGA systems. The special features shown in Table 1 along with more general ones are covered below.

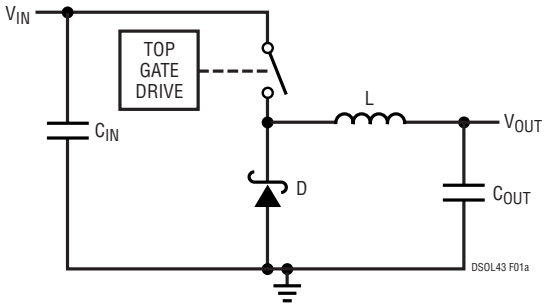
Table 1. Switch Mode Regulators for 1.2V and 1.5V FPGA Systems

LTC CONTROLLER		REFERENCE DESIGN	
PART NUMBER	SPECIAL FEATURES	V_{IN}	V_{OUT} AT I_{OUT}
LTC®3407	Dual Output, Monolithic, 100% Duty Cycle	3.3V, 5V	2.5V at 0.6A 1.5V at 0.6A
LTC3413	DDR Memory, Monolithic	2.5V, 3.3V, 5V	1.25V at ±3A
LTC3414	Single Output, Monolithic, 100% Duty Cycle	3.3V, 5V	1.5V at 4A
LTC3736	Dual Output/Dual Phase, Rail Tracking, No R_{SENSE}™, 100% Duty Cycle	3.3V, 5V	2.5V at 5A 1.2V at 5A (V_{IN} = 5V)
LTC3728L	Dual Output/Dual Phase, 3.3V and 5V LDO	5V, 12V	2.5V at 5A 1.5V at 5A
LTC1778	Single Output, Fixed On-Time, No R_{SENSE}, 5V LDO	5V, 12V	1.2V at 12A
LTC3717	DDR Memory, Fixed On-Time, No R_{SENSE}	5V, 12V	1.25V at ±10A
LTC3708*	Dual Output/Dual Phase, Rail Tracking, Fixed On-Time, No R_{SENSE}	5V, 12V	2.5V at 15A 1.2V at 15A

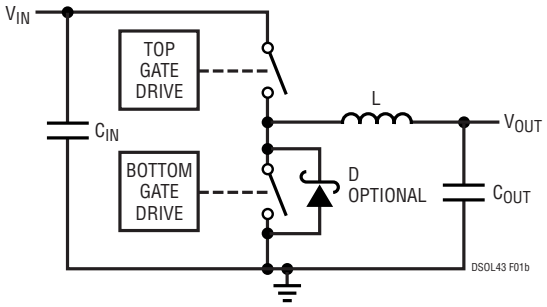
*5V bias supply required.

Synchronous Operation

All of the regulators shown in Table 1 are synchronous step-down regulators. This means that a MOSFET switch is used in place of the free-wheeling Schottky diode of nonsynchronous switch mode step-down regulators (see Figure 1). The advantage of using a synchronous step-down regulator as opposed to a nonsynchronous step-down regulator or linear mode regulator is efficiency. A small Schottky placed in parallel with the bottom switch provides further yet modest efficiency gains. The full load efficiency of all the regulators in Table 1 is greater than 78%, with most efficiencies in the mid 80% range. See Table 2 for efficiency data.



(1a) Conventional Step-Down Converter



(1b) Synchronous Step-Down Converter

Figure 1. Conventional Step-Down Regulator vs Synchronous Step-Down Regulator

Table 2. Full Load Regulator Efficiency

PART NUMBER	V_{OUT} at I_{OUT}	INPUT VOLTAGE			
		2.5V	3.3V	5V	12V
LTC3407	2.5V at 0.6A 1.5V at 0.6A		88% 81%	87% 80%	
LTC3413	1.25V at ±3A	78%	81%	81%	
LTC3414	1.5V at 4A	78%	80%	80%	
LTC3736	2.5V at 5A/3A 1.2V at 5A/3A (V_{IN} = 5V/3.3V)		92% 86%	90% 83%	
LTC3728L	2.5V at 5A 1.5V at 5A			90% 85%	91% 87%
LTC1778	1.2V at 12A			85%	83%
LTC3717	1.25V at ±10A			83%	82%
LTC3708	2.5V at 15A 1.2V at 15A			92% 88%	92% 88%

Monolithic Converters

The LTC3407, LTC3413 and LTC3414 devices are monolithic, which means that the switches and current sensing elements are built-in. These monolithic devices provide the user with a minimum parts count, reduced footprint solution. For higher output current levels, controllers driving external switches are required.

No R_{SENSE} Operation

The No R_{SENSE} parts (LTC1778, LTC3717, LTC3708, LTC3736) sense the voltage drop across the $R_{DS(ON)}$ of the external FETs, eliminating the need for a sense resistor. This reduces circuit size and cost and improves efficiency. Of the parts listed in Table 1, only the LTC3728L uses external sense resistors, and the advantage of this is tighter peak current measurement accuracy.

100% Duty Cycle

The LTC3407 dual monolithic, LTC3414 monolithic and LTC3736 controller are examples of synchronous devices that can operate at duty cycles up to and including 100%, which is beneficial in battery-powered applications. At 100% duty cycle, the top switch turns on continuously and reduces the dropout voltage to the voltage drop across the $R_{DS(ON)}$ of the top switch and the output inductor. Battery run-time is extended as a result, for small step-down ratio applications.

Light Load Efficiency

The devices listed in Table 1 feature a variety of light load operating modes such as Burst Mode® operation or Pulse Skip designed to improve efficiency by preventing reverse currents from flowing through the inductor. However, these operating modes may affect the output voltage ripple. Refer to the individual data sheets for more details on these operating modes.

Switching Frequency

A high switching frequency is desired because as the switching frequency increases, smaller output capacitors and inductors can be used. The lowest output current/lowest input voltage regulators are able to operate with the highest switching frequency, which further reduces the solution size. The highest output current/high input voltage regulators operate at lower frequencies. The switching frequency range for all of the reference design shown varies from 200kHz to over 1MHz.

Burst Mode is a registered trademark of Linear Technology.

Fixed On-Time

The fixed on-time parts (LTC1778, LTC3708, LTC3717) are ideal for applications that require a very fast response time with a minimal amount of output capacitance and/or for applications that operate with a very narrow duty cycle (i.e., large input to output voltage differentials) and a relatively high switching frequency.

Dual Output/Dual Phase Operation

The dual phase controllers (LTC3736, LTC3728L, LTC3708) drive their two outputs 180 degrees out of phase. This interleaves the current pulses flowing into the top switch of each phase which reduces the RMS ripple current through the input capacitors and eases input filter design requirements (see Figure 2). For a 2.5V/10A and 1.5V/10A converter operating with an input voltage of 4.5V to 14V, dual phase operation reduces the input capacitor ripple current by a least 30%. As a rule of thumb, the input capacitors only need to be sized for the phase with the highest output current operating at 50% duty cycle. The RMS ripple current for one phase is given as:

$I_{RMS} = I_{OUT(MAX)} \bullet \sqrt{(D \bullet (1 - D))}$, where $D = V_{OUT}/V_{IN}$.

At 50% duty cycle, the equation reduces to:

$I_{RMS} = I_{OUT(MAX)}/2$

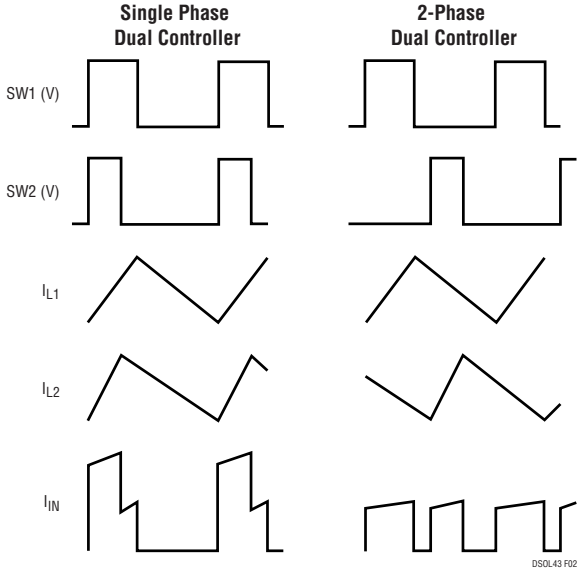


Figure 2a. Dual-Phase vs Single Phase Operation

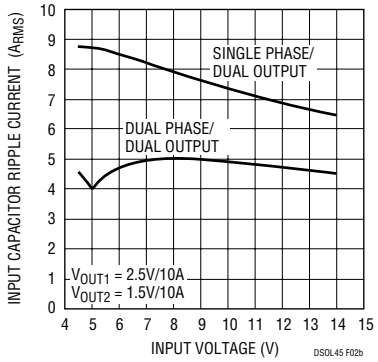


Figure 2b. Input Capacitor Ripple Current vs Input Voltage (LTC3708)

Power Supply Tracking

The most recent dual phase/dual output regulator controllers (LTC3736, LTC3708) offer rail tracking. This feature allows either coincidental or ratiometric tracking to be implemented. The LTC3736 offers ramp-up tracking. The LTC3708 offers both ramp-up and ramp-down tracking, and multiple LTC3708s can be daisy-chained for applications where tracking of more than two rails is required. See Figures 3 and 4 for examples.

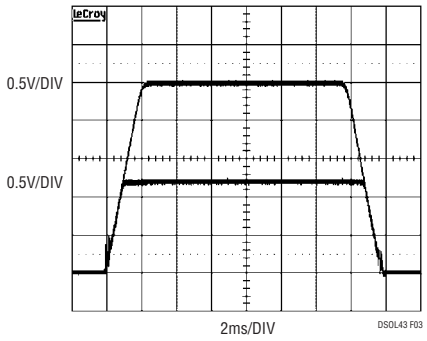


Figure 3. Up/Down Coincident Rail Tracking of the LTC3708

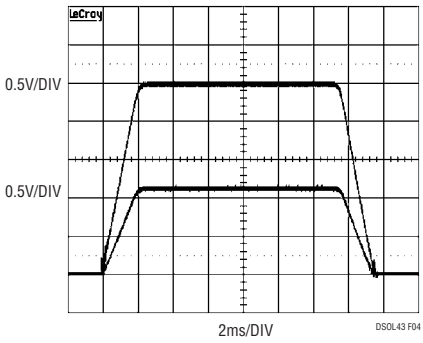


Figure 4. Up/Down Ratiometric Rail Tracking of the LTC3708

DDR Memory Termination

The Stratix II, Stratix, Stratix GX and Cyclone FPGAs can interface with DDR memory. A DDR memory interface requires a termination supply set to half the driver voltage that can both sink and source current. A synchronous buck regulator is well suited for the latter because current can flow both ways through the switches. A synchronous buck regulator is also more efficient than a linear mode DDR regulator. Two products targeted for DDR memory termination are the LTC3413 and the LTC3717.

REFERENCE DESIGNS

The reference designs in Table 1 are all optimized for specific output current and input voltage ranges found in FPGA systems, with an emphasis on 1.2V and 1.5V core voltages. A brief description of each follows.

LTC3407

Figure 5 shows a 2.5V/600mA and 1.5V/600mA LTC3407 regulator that can be powered from a local 3.3V or 5V rail. It operates at a frequency of 1.5MHz, allowing the use of tiny output capacitors and inductors with less than a 2mm profile, and its integrated switches conserve board space. This dual regulator provides a very compact design for low power FPGA systems.

LTC3414

Figure 6 shows a 1.5V/4A LTC3414 regulator that can be powered from a local 3.3V or 5V rail. This regulator is programmed for a switching frequency of 1MHz, allowing the use of a small, low DC resistance (DCR), 6.5mm × 6.9mm 0.47µH output inductor, and its internal switches conserve board space. This is a compact solution for medium power single voltage FPGA systems.

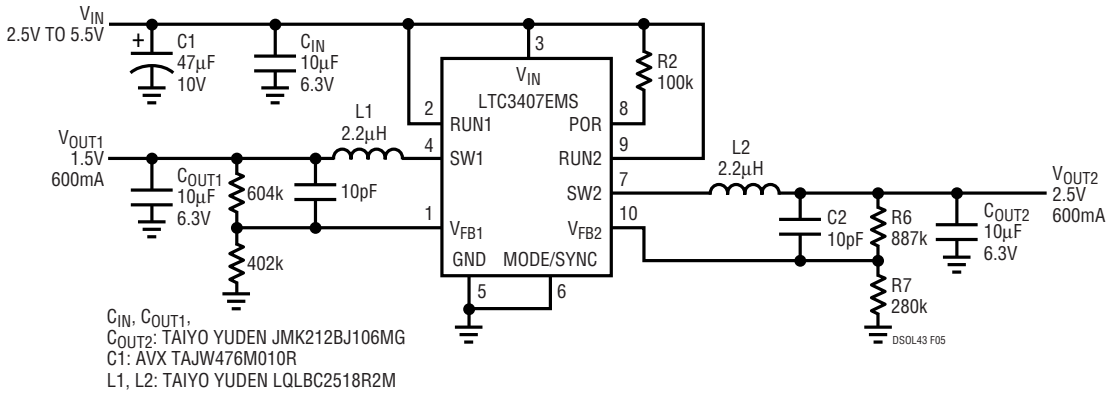


Figure 5. LTC3407: Monolithic 1.5V/600mA and 2.5V/600mA Regulator

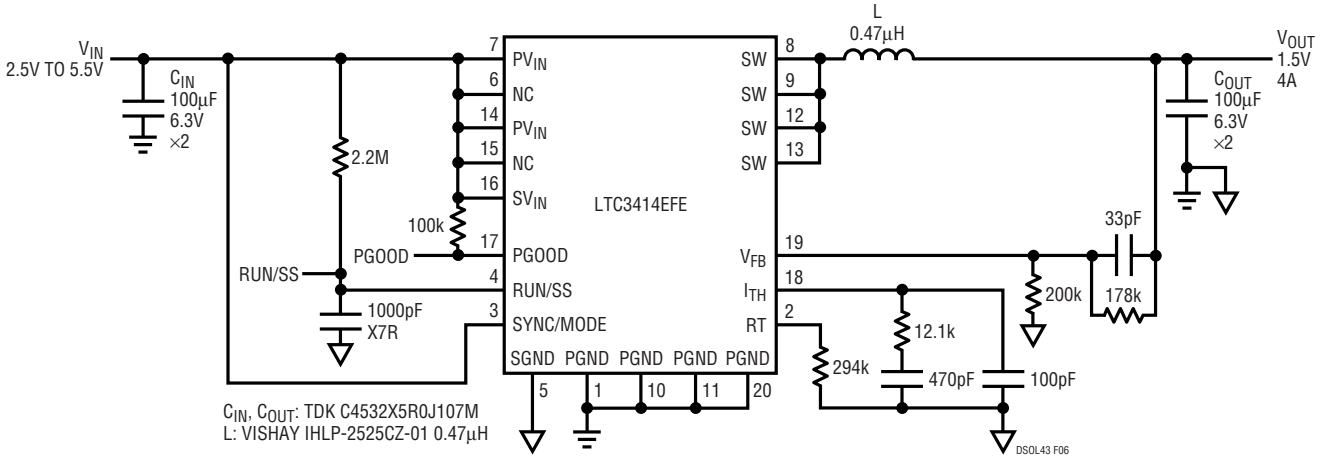


Figure 6. LTC3414: Monolithic 1.5V/4A Regulator

LTC3736

Figure 7 shows a 2.5V/1.2V dual output LTC3736 regulator that is powered from a local 3.3V or 5V rail. At an input voltage of 5V, both rails can provide 5A of output current. This regulator is an efficient solution for mid-power FPGA systems that require ramp-up power supply tracking.

LTC3728L

Figure 8 shows a 2.5V/1.5V dual output LTC3728L regulator which can be powered from either a 5V or 12V rail. Both outputs can provide 5A. This is another efficient solution for mid-power FPGA systems with a higher input voltage range.

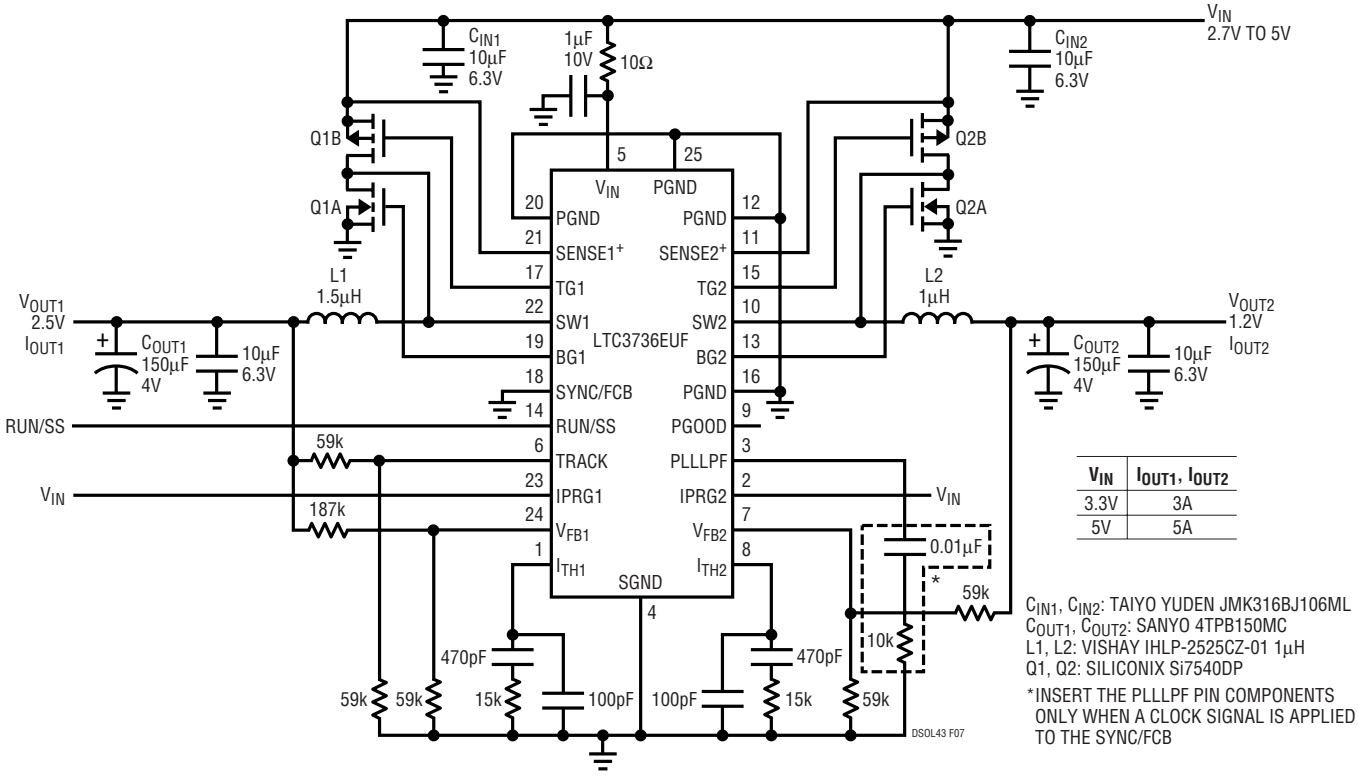


Figure 7. LTC3736: 2.5V/5A and 1.2V/5A Regulator with Rail Tracking

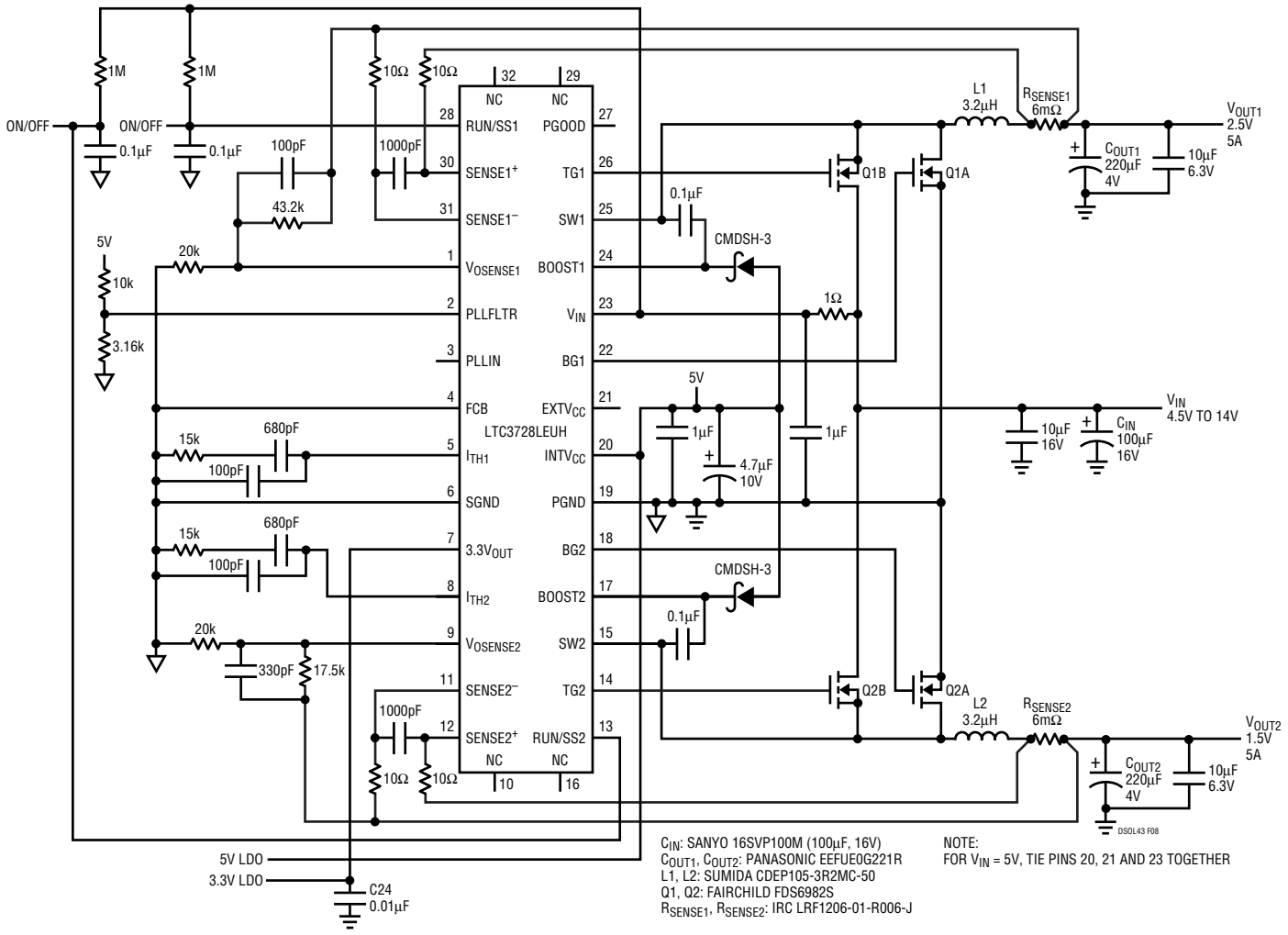


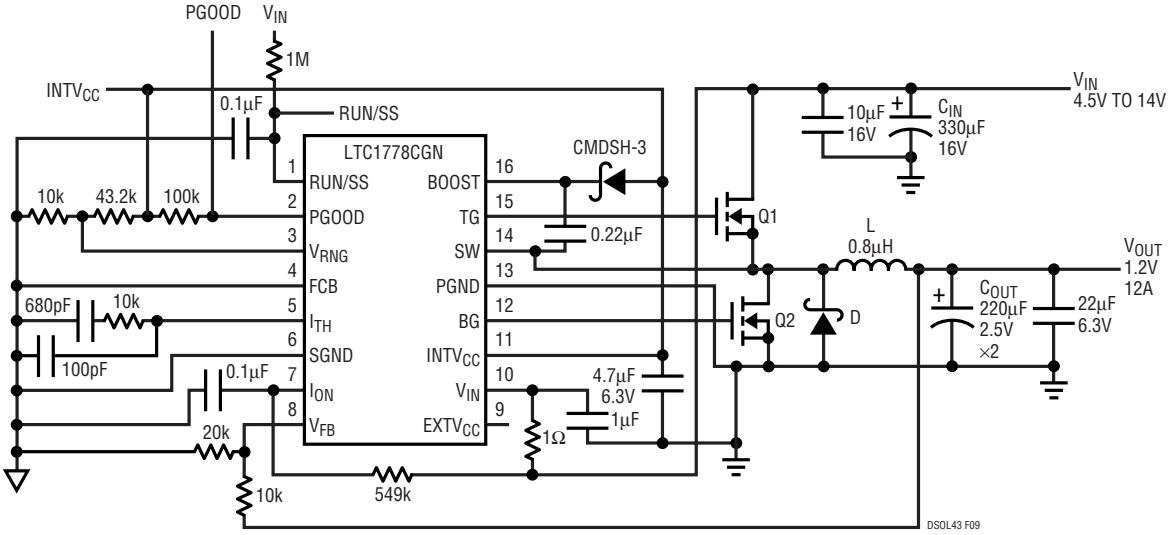
Figure 8. LTC3728L: High V_{IN} 2.5V/5A and 1.5V/5A Regulator

LTC1778

Figure 9 shows a 1.2V/12A single output LTC1778 regulator. Its input can be tapped from either a 5V or 12V rail. This is an efficient solution for high power FPGA systems.

LTC3708

Figure 10 shows a 2.5V/15A and 1.2V/15A LTC3708 regulator, which can use either 5V or 12V as its input. The strong gate drivers of the LTC3708 allow high output current to be delivered efficiently. For an input voltage of either 5V or 12V, its 1.2V output can deliver 15A with an efficiency of 88%. This is a very efficient solution for high-power FPGA systems that require up/down power supply tracking and has the highest efficiency of all the regulators shown.



C_{IN}: SANYO 16SVP330M
C_{OUT}: PANASONIC EEFUE0E221R
D: DIODES B340A

L: SUMIDA CDEP105-0R8MC-88
Q1: SILICONIX Si4860DY
Q2: SILICONIX Si4842DY

NOTE:
FOR V_{IN} = 5V, TIE PINS 9, 10 AND 11 TOGETHER

Figure 9. LTC1778: High V_{IN} 1.2V/12A Regulator

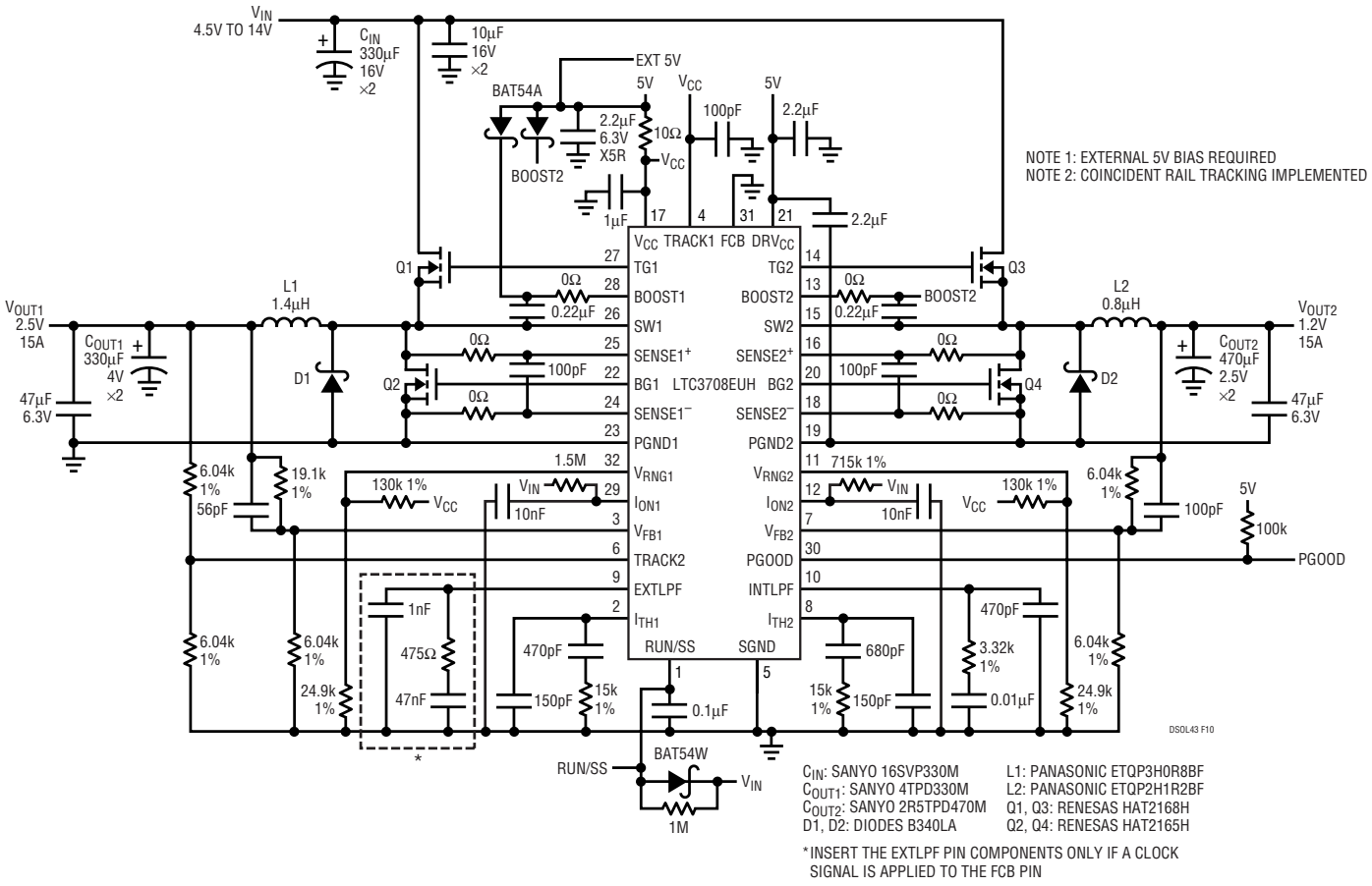


Figure 10. LTC3708: 2.5V/15A and 1.2V/15A Regulator with Up/Down Rail Tracking

LTC3413

Figure 11 shows a monolithic 1.25V ±3A DDR termination regulator featuring the LTC3413. It can use either a local 2.5V, 3.3V or 5V rail as its input voltage. It operates at a switching frequency of 1MHz, which allows a small 6.5mm × 6.9mm 0.47µH output inductor to be used. It is a compact and efficient solution for typical DDR applications.

LTC3717

Figure 12 shows a 1.25V ±10A DDR regulator that uses the LTC3717 controller. It can be powered from either a 5V or 12V rail. This is an efficient solution for high power DDR applications.

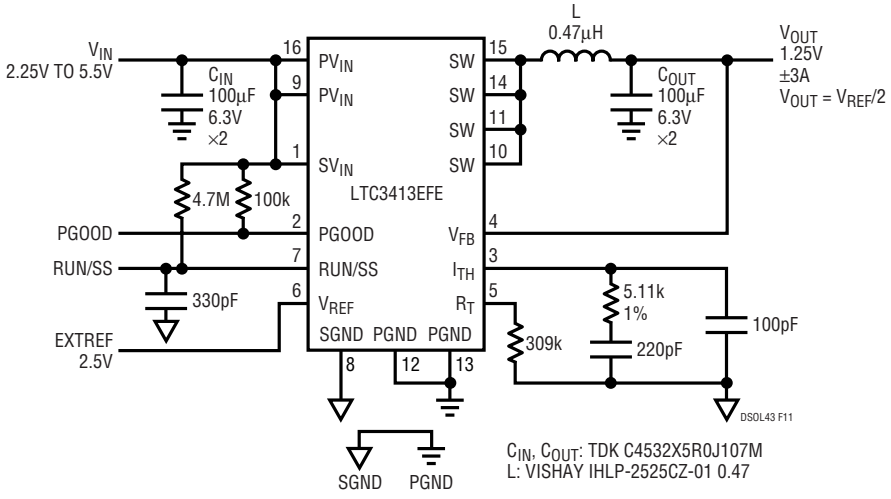


Figure 11. LTC3413: Monolithic 1.25V ±3A DDR Termination Regulator

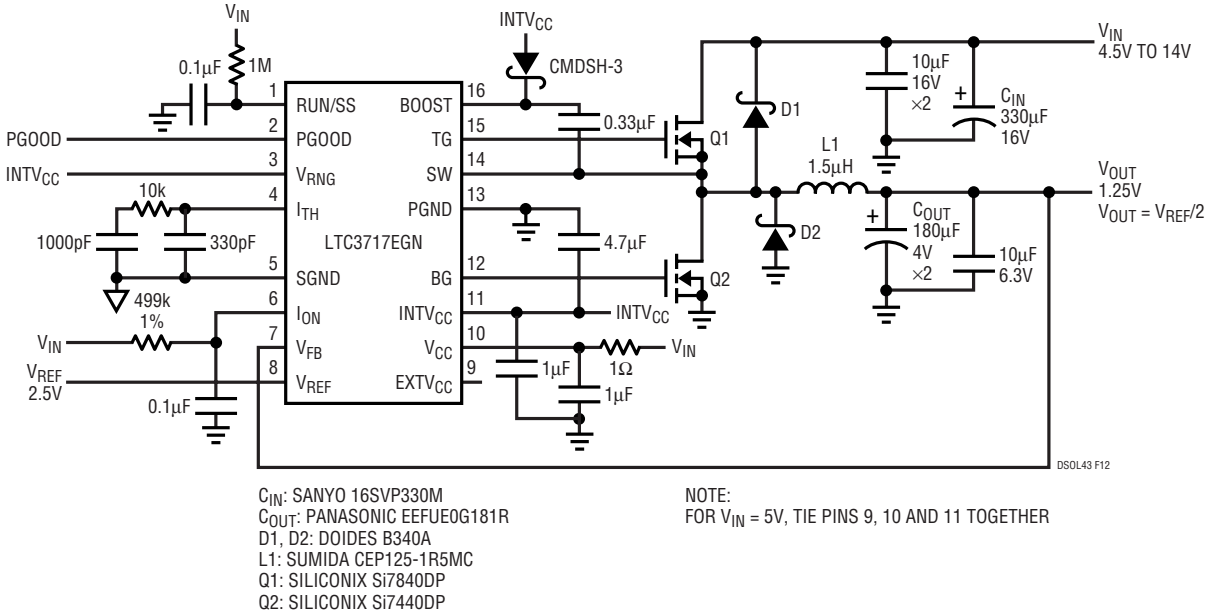


Figure 12. LTC3717: 1.25V ±10A DDR Termination Regulator

OUTPUT VOLTAGE REGULATION

Output voltage regulation is an important consideration when designing a power supply. Important factors to consider are set point accuracy, load regulation and output ripple.

Set Point Accuracy

The output voltage set point accuracy is determined by the tolerance of the reference and the feedback resistor divider used. The equation for the output voltage is given as:

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_{TOP}}{R_{BOTTOM}}\right)$$

See Figure 13 for a simplified schematic. The reference voltage tolerance for the parts discussed in this article is from 1% to 2%. Use 1% feedback resistors for the specified performance.

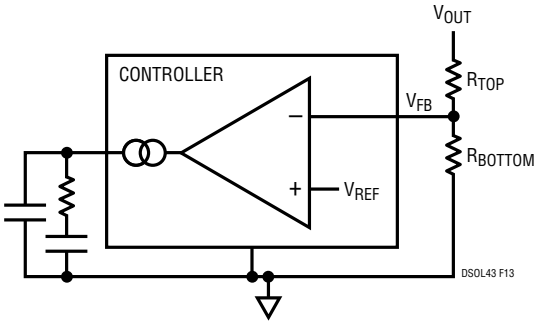


Figure 13. Feedback Voltage Divider

DC Load Regulation

The DC load regulation is affected by layout and open-loop gain. Layout is the dominant factor since the open-loop gain is always sufficiently high. To achieve good regulation, make sure the voltage feedback divider is connected directly across the (+) and (–) terminals of C_{OUT} .

Output Ripple

Ripple is measured in terms of mV peak-peak. This is the instantaneous variation of the output voltage and is determined by the switching frequency of the regulator as well as the input voltage, output voltage, inductor value, effective series resistance of the output capacitors and the amount of output capacitance.

An equation for output ripple is as follows:

$$\text{Ripple} = I_{P\text{-}P} \bullet \left(ESR + \frac{1}{8 \bullet f_{SW} \bullet C_{OUT}}\right) mV_{P\text{-}P}$$

where the peak-to-peak ripple current ($I_{P\text{-}P}$) is defined as:

$$I_{P\text{-}P} = \frac{V_{IN} - V_{OUT}}{L \bullet f_{SW}} \bullet \frac{V_{OUT}}{V_{IN}}$$

The dominant term in the above equation is ESR. When selecting output capacitors, choose components with low ESR values to minimize the output ripple.

CURRENT LIMIT

When designing a regulator, determine the maximum surge current that must be supplied. For FPGAs, the maximum surge current typically occurs during turn-on when the device is being programmed. The regulator's maximum output current ($I_{OUT(MAX)}$) must be greater than the maximum expected surge current. The data sheets for all of the parts shown contain the formulas for calculating $I_{OUT(MAX)}$. Refer to the data sheets and/or contact Linear Technology for assistance.

COMPONENT SELECTION

The four major components to be selected are the inductor(s), output capacitors, input capacitors and external MOSFETs. Use the demo board bill of materials and data sheet to help determine which parts to use, and consult with the parts vendor. An overview of the selection criteria follows.

Output Inductor

Select the inductor value such that inductor peak-to-peak ripple current ($I_{P\text{-}P}$) is 40% of $I_{OUT(MAX)}$. This is a good starting point. Smaller values can be chosen, but the trade-off is higher ripple current and higher output voltage ripple. A larger value can be chosen, but the trade-off is larger package size, increased DCR and reduced signal strength for the current sense signal. Make sure the inductor's rated saturation current is greater than $I_{OUT(MAX)} + I_{P\text{-}P}/2$. A partial list of vendors includes Sumida, Vishay, Toko, Pulse, Panasonic, Coilcraft, Coiltronics and Murata.

Output Capacitance

Select capacitors with low ESR to minimize the output voltage ripple. Low ESR capacitors include the Sanyo Poscap, Panasonic Specialty Polymer, Kemet AO-Cap, Kemet polymer tantalums (T520), as well as a variety of low ESR solid tantalums. Pay careful attention to the voltage derating. Multilayer ceramic capacitors can also be used, but they have very low ESR which makes loop compensation more challenging. Refer to Linear Technology Application Note 76 for more details.

Input Capacitance

The input capacitance must supply the pulsed current that flows through the top FET. Select C_{IN} with a ripple current rating that meets or exceeds the maximum expected ripple current. The capacitance value must also be high enough for adequate circuit stability.

Sanyo OS-CONs or similar parts are a good choice due to their high RMS current ratings and their high capacitance. However, they have high series inductance (ESL). To minimize the ESL, a ceramic capacitor should be paralleled with the OS-CON and placed next to the top and bottom FETs.

Aluminum electrolytics are inexpensive, but their RMS current ratings are low relative to OS-CONs and their ESL is also high. Sometimes, a carefully selected parallel combination of aluminum electrolytics and high grade ceramics can be used where the ceramics handle the ripple current and the aluminum electrolytics provide the bulk capacitance for stability.

MOSFETs

For the controllers, external MOSFETs are required. The bottom FET needs to have a low $R_{DS(ON)}$ to minimize conduction losses. The top FET needs to have a low gate charge (Q_G) to minimize transition losses, and if the duty cycle is high, a low value of $R_{DS(ON)}$ as well. Make sure the current rating of the MOSFET is not exceeded. Contact the MOSFET vendor for more details. MOSFET vendors include Vishay Siliconix, Renesas, International Rectifier, and Fairchild.

SWITCHING FREQUENCY

The controllers shown in Table 1 operate at various frequencies. The LTC3407 operates at a fixed frequency of 1.5MHz. The switching frequency on the other parts can be set within a range by a voltage or a resistor. For the fixed on-time parts, the switching frequency is determined by the output voltage and programmed on-time. Refer to the individual data sheets for more details.

LOOP COMPENSATION

All of the controllers shown in Table 1 use current mode control. In the simplest model of a current mode buck regulator, the output inductor is considered to be a current source controlled by the output voltage of the error amplifier. This reduces the output power stage to a first order system with the output capacitance forming the dominant pole. Both the value of C_{OUT} and its ESR are critical in designing a stable loop in addition to the compensation components and the feedback divider. Refer to Linear Technology's Application Note 76 for more details.

LAYOUT

Board layout is a very critical step in designing a switch mode step-down regulator. A poor layout can affect stability, regulation and reliability. Refer to the individual data sheets for specific guidelines as well as the demo board gerber files. Here are several points to keep in mind when addressing layout issues for controllers:

- Devote entire layers or planes for the ground, all output voltages and the input voltage. Liberally spread the copper for these signals.
- Make all of the high current connections as wide and short as possible.
- Place a ground plane underneath the controller.
- Keep the signal ground (SGND) and power grounds (PGND) separate, and tie SGND to PGND at one location.
- The loop area formed by the top FET, bottom FET and ceramic input capacitor should be as small as possible.
- Keep the high dV/dt traces away from the control signals.
- If necessary, shield the high dV/dt traces on one layer from the control signals on another with the GND plane, V_{IN} plane or V_{OUT} plane.
- Use Kelvin current sensing for the current sense lines (if applicable).
- Allow sufficient copper for heat-spreading.

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