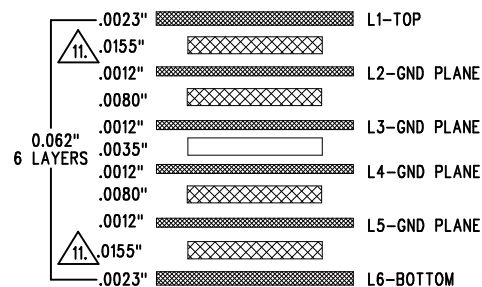


SIZE	QTY	SYM	PLATED	TOL
0.01	1044	+	YES	+/-0.003
0.065	8	×	YES	+/-0.003
0.06	2	□	YES	+/-0.003
0.187	4	◇	YES	+/-0.003
0.07	2	⊗	NO	+/-0.003
0.035	5	⊠	YES	+/-0.003
0.05	2	⊕ ^A	NO	+/-0.003
0.095	3	⊕ ^B	YES	+/-0.003

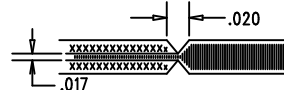
△1. SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC CONSTANT DEVIATIONS. PLEASE CONSULT LTC.

LAYER STRUCTURE



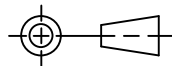
NOTES: UNLESS OTHERWISE SPECIFIED

- FAB PER IPC-A-600.
- MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR-370HR OR EQUIVALENT.
-FINISHED THICKNESS TO BE 0.062" +/- .005"
-TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.
-GOLD IMMERSION BOTH SIDES.
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):



- CONTROLLED 50 OHM +/-5% IMPEDANCE FOR LAYERS 1-3 USING 0.03" TRACE.
- CONTROLLED 100 OHM +/-5% IMPEDANCE FOR LAYERS 1-2 DIFFERENTIAL PAIR USING 0.00795" TRACE, 0.006" GAP.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
0.XX" = ±0.01"
0.XXX" = ±0.005"
INTERPRET DIM AND TOL
PER ASME Y14.5M-1994
THIRD ANGLE PROJECTION



APPROVALS

PCB DES.	AK
APP ENG.	CLARENCE M.
SCALE = NONE	

LINEAR TECHNOLOGY
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TITLE: FABRICATION DRAWING

LOW POWER DUAL ADC FAMILY

SIZE	IC NO.	LTC215XCUP FAMILY	REV
N/A		DEMO CIRCUIT 1564A	3
FILENAME:	DC1564A-3.PCB		SHT 1 OF 1