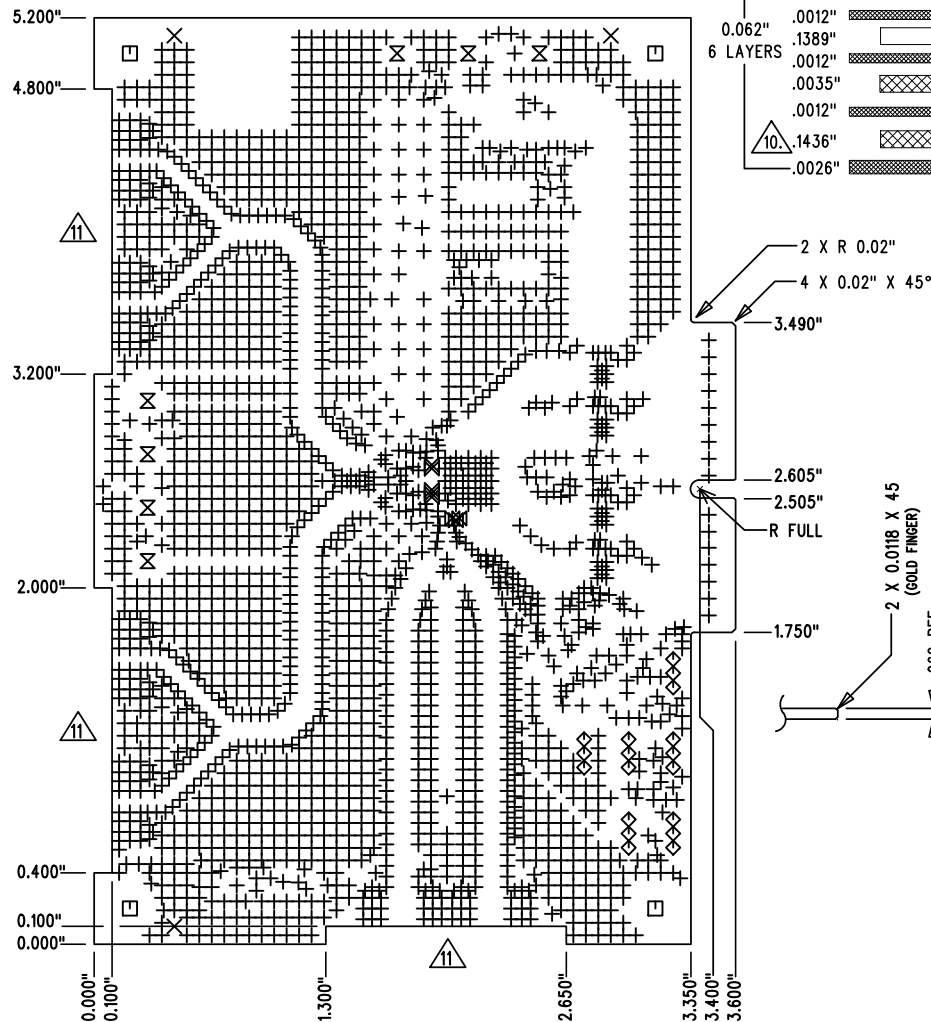


SHOWN FROM TOP SIDE



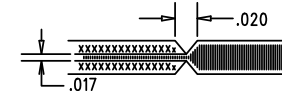
LAYER STRUCTURE

0.0026"	L1-TOP
0.1436"	L2-GND PLANE
0.0012"	L3-GND PLANE
0.0035"	L4-GND+PWR+SIGNALS
0.0012"	L5-GND PLANE
0.1436"	L6-BOTTOM

0.062"
6 LAYERS

NOTES: UNLESS OTHERWISE SPECIFIED

- FAB PER IPC-A-600.
- MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR-370HR OR EQUIVALENT.
-FINISHED THICKNESS TO BE 0.062" +/- .005"
-TOTAL OF 6 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR BLACK.
-GOLD IMMERSION BOTH SIDES.
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):



- CONTROLLED 50 OHM +/-5% IMPEDANCE FOR LAYERS 1-3 USING 0.029" TRACE AT 2GHz FREQ.
CONTROLLED 50 OHM +/-5% IMPEDANCE FOR LAYERS 1-2 USING 0.030" TRACE AT 2GHz FREQ.

10. SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC CONSTANT DEVIATIONS. PLEASE CONSULT LTC.

11. INNER AND OUTER LAYER COPPER SHALL BE EXPOSED ALONG BOARD EDGES. DO NOT MODIFY INNER LAYER COPPER BACKOFF OUTLINE (SMA CONNECTOR).

- FINGER AREA: GOLD PLATE TO MIN. OF 0.00003 INCHES.
PER MIL-G-45204, TYP II, CL1, GRADE C, OVER 0.0002 INCHES LOW STRESS NICKEL PER QQ-N-290, CL2.

UNLESS OTHERWISE SPECIFIED		APPROVALS			
DIMENSIONS ARE IN INCHES		PCB DES.	KIM T.		
TOLERANCES:		APP ENG.	CLARENCE M.	TITLE: FABRICATION DRAWING	
0.XX" = ±0.01"				2-CHANNEL, HIGH SPEED LOW POWER	
0.XXX" = ±0.005"				ADC FAMILY, CMOS	
INTERPRET DIM AND TOL PER ASME Y14.5M-1994				SIZE	IC NO.
THIRD ANGLE PROJECTION				N/A	LTC2XXXCUP FAMILY
					DEMO CIRCUIT 1975A
				SCALE = NONE	REV 1
				FILENAME: DC1975A-1.PCB	SHT 1 OF 1

REVISION HISTORY

ECO	REV	DESCRIPTION	APP. ENG.	DATE
-	1	PRODUCTION	CLARENCE M.	03-27-13

SIZE	QTY	SYM	PLATED	TOL
0.01	2386	+	YES	+/-0.003"
0.07	3	X	NO	+/-0.003"
0.188	4	□	YES	+/-0.003"
0.035	18	◇	YES	+/-0.003"
0.094	7	⊗	YES	+/-0.003"
0.006	8	⊗	YES	+/-0.003"

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