LINEAR TECHNOLOGY

DESIGN NOTES

Micropower Op Amp Drives 8-Channel 18-Bit Simultaneous Sampling ADC without Compromising Accuracy or Breaking the Power Budget

Design Note 541

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Introduction

The op amps used to drive 18-bit analog-to-digital converters (ADCs) typically draw as much supply current as the ADC itself, often with a maximum offset spec that is well above that of the ADC. If multiple ADC channels are required, the power dissipation from these drivers quickly rises to unacceptable levels.

If 18-bit precision is required (SNR, THD, V_{OS}), but not high sampling rates, and the input signals are low frequency or DC, the simple buffer presented is capable of driving the LTC®2348-18 8-channel simultaneous sampling ADC. It also achieves performance equivalent to typical specs for SNR, THD and offset performance with very low power dissipation.

Circuit Description

The LTC2348-18 is a low noise, 8-channel simultaneous sampling 18-bit successive approximation register (SAR) ADC with wide input common mode range. With a ±10.24V input range, the LTC2348-18 achieves –109dB THD (typical), 96.7dB SNR (typical) with an offset of ±550µV (maximum) while dissipating only 140mW (typical) at 200ksps. When operated at the 10ksps rate of this application, the ADC's power consumption drops to 45mW (typical) by using the device's NAP mode.

The LT6020 is a dual micropower, 5V/µs precision rail-to-rail output op amp with input offset voltage of less than 30µV (maximum) that draws only 100µA per amplifier (maximum).

The circuit of Figure 1 shows the LT6020 op amp configured as a noninverting buffer driving the analog inputs of the LTC2348-18. Maximum power dissipation of each op amp is only 3mW. For all eight channels this adds up to only 24mW, approximately half the ADC power consumption at 10ksps.

The RC filter at the buffer output minimizes the noise contribution of the LT6020 and reduces the effect of the sampling transient caused by the MUX and the input sampling capacitor. For a chosen RC time constant, the R value should be kept as small as possible to reduce the voltage drop across the resistor. This results in a gain error if the filter output is not allowed to settle completely. The R value must be large enough to prevent excessive ringing at the op amp output, which adds to settling time and increases distortion.

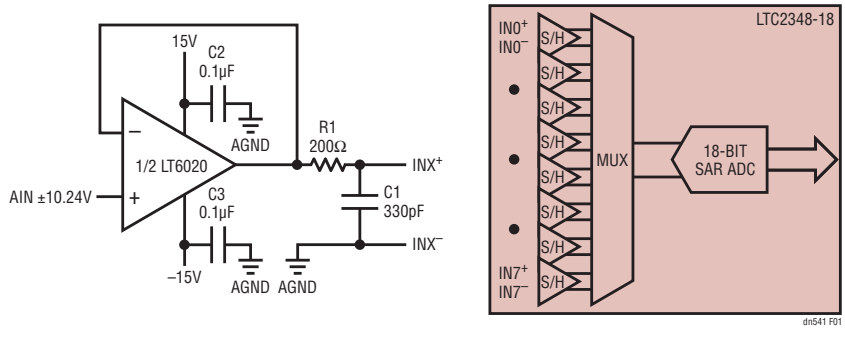

Figure 1. LT6020 Buffer Driving the LTC2348-18 8-Channel Simultaneous Sampling SAR ADC

The LTC2348-18 accepts arbitrary differential input signals swinging over a wide common mode range. Differential signals may be buffered into the positive and negative analog inputs using two unity-gain amplifiers. Pseudo-differential input signals referenced to a low impedance node such as ground require only one buffer amplifier. This second case is used by the circuit in Figure 1.

Circuit Performance

All data and curves shown were taken with the DC2094A-A. Improved performance may be possible by holding t_{ACQ} constant at 12µs while varying the sample rate. Figure 2 shows an 8192-point FFT of the LTC2348-18 driven pseudo-differentially by the buffer of Figure 1. THD is –108dB and SNR is 95.8dBFS at 10ksps, which compares well with the typical specs of the LTC2348-18.

Figure 3 shows SNR and THD vs sampling rate. SNR stays fairly flat near 96dBFS up to 10ksps. THD starts to rise above –108dB at 10ksps.

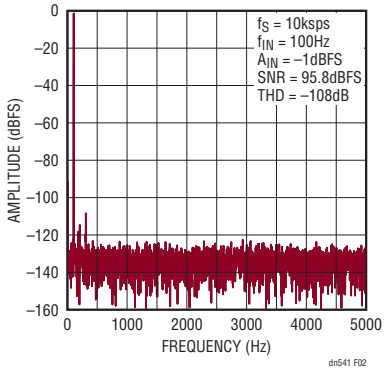

Figure 2. 8192-Point FFT for the Circuit of Figure 1

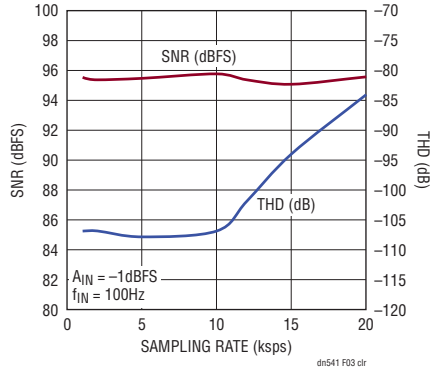

Figure 3. SNR and THD vs Sampling Rate for the Circuit of Figure 1

Figure 4 shows SNR and THD vs input frequency. Both SNR and THD slowly degrade from the typical specs of the LTC2348-18 above 100Hz until at 1kHz SNR is 94dBFS and THD is –85dB.

Figure 5 shows the combined offset error of the LT6020 driver and ADC vs sampling rate. Offset is initially less than 1LSB and starts to degrade as the sampling rate exceeds 10ksps.

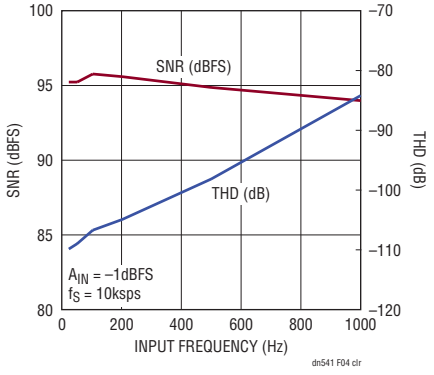

Figure 4. SNR and THD vs Input Frequency for the Circuit of Figure 1

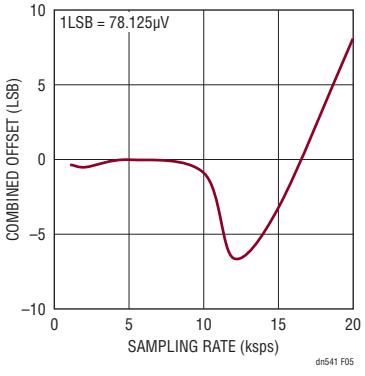

Figure 5. Combined ADC and Driver Offset vs Sampling Rate for the Circuit of Figure 1

Conclusion

A simple driver for the LTC2348-18 18-bit, 200ksps, 8-channel simultaneous sampling SAR ADC—consisting of the LT6020 low power precision dual op amp configured as noninverting buffers—dissipates only 3mW per op amp (maximum), and at 10ksps the LTC2348-18 dissipates only 45mW. At a sampling rate of 10ksps, SNR is measured at 95.8dB, THD –109dB and offset is measured at less than 1LSB.

Data Sheet Download

www.linear.com/LTC2348-18

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