Design Checklist for LTC297X Family of PSM Managers

Introduction

Please review this checklist to ensure the following topics are considered for your LTC®297x board design. If you make any exceptions to these rules, please contact Linear Technology® to make sure your design will work properly. The term "LTC297x" refers to the following devices: LTC2974, LTC2975, LTC2977, LTC2978, LTC2978A, LTC2980, LTM2987.

Connect Logic/Coordination Signals

- ❑ Tie WDI/RESETB to V_{DD33} with a 10kΩ resistor. Do not connect a capacitor to the WDI/RESETB pin.
- ❑ Tie all SHARE_CLK pins together, pull up to 3.3V with a single 5.49kΩ resistor.
- ❑ FAULTB pins may be tied together or separated but make sure each FAULTB pin has a 10kΩ pull-up to V_{DD33}. FAULTB pins are not only outputs, but inputs as well. If a FAULTB pin is floating, this could cause unexpected faulting behavior.
- ❑ Tie CONTROL pins high or low, pull up/down to 3.3V/GND with a 10kΩ resistor if CONTROL pin is used to enable outputs (CONTROL pin behavior depends on device configuration).
- ❑ Tie all ALERTB pins together, pull up to 3.3V with a single 10kΩ resistor.
- ❑ Tie all SCL pins together; tie all SDA pins together; pull up each to 3.3V with a 10kΩ resistor.
- ❑ Adjust SDA/SCL pull-up or add an I^2C bus buffer if stray capacitance is an issue. Check the rising edges of SCL/SDA with an oscilloscope to confirm.
- ❑ Tie all WP pins together, pull up/down to 3.3V with a single 10kΩ resistor to enable/disable write-protect.
- ❑ Do not leave WDI/RESETB, SHARE_CLK, CONTROL or FAULTB pins floating!

Addressing (ASEL)

- ❑ The address select pins (ASELs) are tri-level inputs: low, high, and float. Check the Address Look-Up Table in the data sheet. The device responds to the address: base address + offset. The base address is defined by the MFR_I2C_BASE_ADDRESS register and the offset is defined by the ASEL pins.
- ❑ Check for collision with other devices on the bus and any global addresses published in their data sheets (e.g., do not use address 0x5D if using LTC4306 I^2C addressable bus multiplexer since this device uses 0x5D for the mass write address).
- ❑ Best practice is to use a single common base address for all devices and tie ASEL pins such that each device has a different offset. This provides smooth bus enumeration and ensures recovery if in-system programming fails.

Output Enable Pins (V_{OUT_EN})

- ❑ Connect the output enable pins of the LTC297x device to the RUN/SHDN pins of the switchers/ LDOs.
- ❑ Use appropriate pull-ups on all V_{OUT_ENn} pins, 10kΩ is a typical value.
- ❑ The absolute maximum voltages of the V_{OUT_ENn} pins are:
  - V_{OUT_EN}[3:0]: –0.3V to 15V (for all LTC297x), these pins have an optional weak internal pull-up to 12V
  - V_{OUT_EN}[7:4]: –0.3V to 6V (LTC2977/LTC2978/LTC2978A).

Anti-Aliasing Filters (V_{SENSE}, I_{SENSE})

- ❑ Add anti-aliasing filters to the LTC297x inputs $V_{SENSEPn}$, $V_{SENSEMn}$, $I_{SENSEPn}$ and $I_{SENSEMn}$.
- ❑ The recommended filtering for voltage inputs is 100Ω and 100nF.
- ❑ The recommended filtering for current sensing is 1kΩ and 10nF (LTC2974/LTC2975).
- ❑ Add a first stage matched filter when using DCR current sensing.
- ❑ There is no need to add an external resistive divider to sense voltages up to 15V on the VIN_SNS pin. This pin has an internal calibrated divider.

Remote Temperature Sensing (T_{SENSE}) (LTC2974/LTC2975 Only)

- ❑ Use a diode-connected PNP or NPN (2N3906/3904).
- ❑ Do *not* use real diodes such as 1N4148 for temperature sensing!
- ❑ The ground connection should go back to the LTC2974/LTC2975 local ground.
- ❑ Use up to 330nF decoupling capacitance if the layout is noisy.
- ❑ Route the temperature sensing traces away from switch nodes or other noise sources.
- ❑ Tie unused T_{SENSE} pins to ground.
- ❑ If T_{SENSE} pins are connected to a removable board (floating inputs in some situations), connect inputs to ground with 100kΩ resistors.

Decoupling Capacitors

- ❑ Use 100nF decoupling capacitors for V_{PWR}, V_{DD33}, V_{DD25}, and between the REFP and REFM pins.
- ❑ Use 10nF decoupling capacitor on $V_{IN\_SNS\_CAP}$ pin of an LTC2975 device.

REFP

- ❑ Do not exceed 100µA of load current on the REFP pin (typically used for negative rail sensing).

Fault Handling

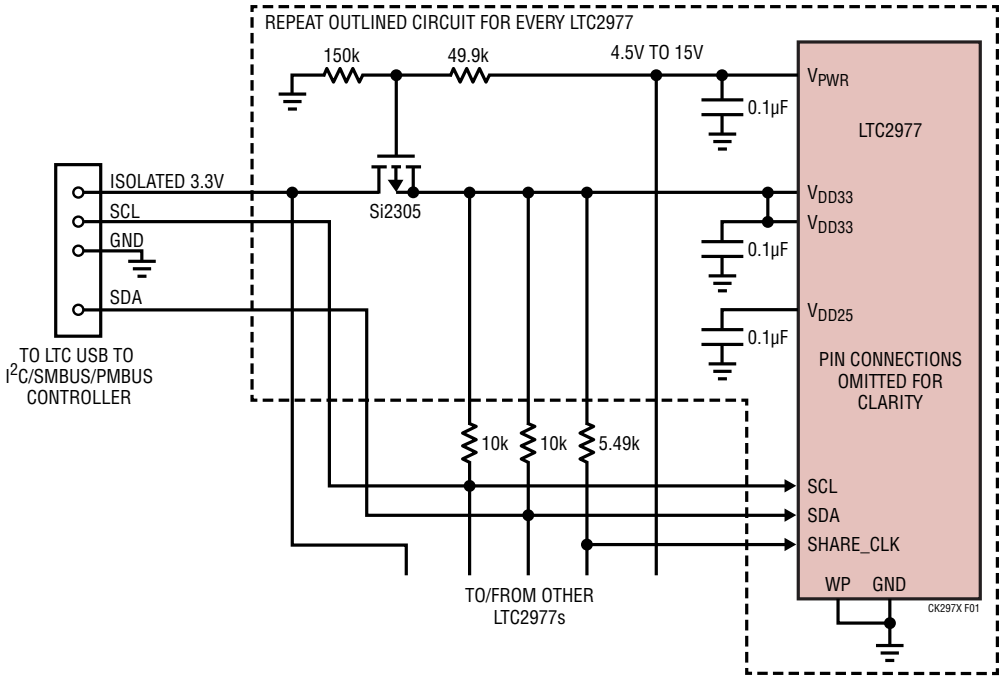
- ❑ For maximum flexibility and software control, tie all FAULTB pins together and pull up to 3.3V with a single 10kΩ resistor.
- ❑ Do not mix power good, fault, and control pins to design custom fault-handling or event-based sequencing schemes. These approaches are extremely difficult to debug and do not allow last minute software fixes.

Unused Inputs

- ❑ Connect all unused $V_{SENSEPn}$, $V_{SENSEMn}$, T_{SENSEn}, and V_{DACMn} pins to GND. Do not allow these pins to float.

Programming

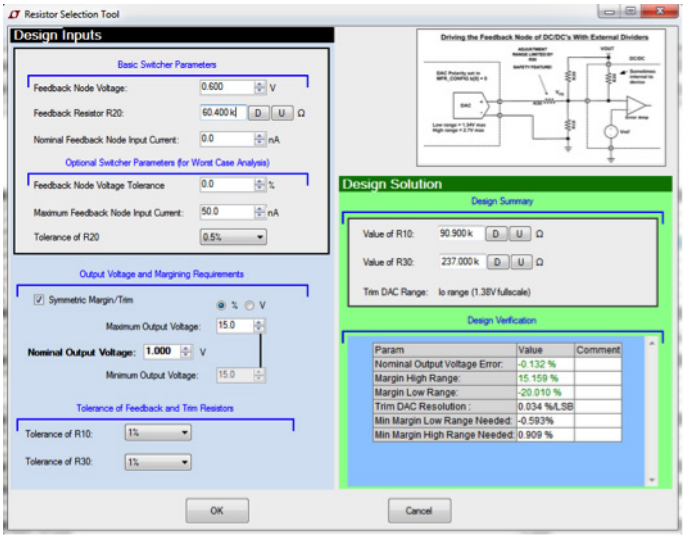
- ❑ Use the schematic below for each LTC297x if programming with DC1613 dongle power only is desired.
- ❑ Ensure that V_{DD33} consumes less than 100mA to avoid overloading the DC1613 I^2C dongle. Otherwise use DC2086 to provide more current.
- ❑ No body diodes between SDA/SCL from any slave device are allowed.



Trim DAC Resistors

❑ Select the trim DAC resistors using the resistor selection tool in the LTpowerPlay® GUI:

- From the main menu “Utilities” -> “Resistor Selection Tool”
- Enter the required information in the form (feedback voltage, desired trim range, etc.).
- The closest 1% standard resistor values are displayed.



Special Note for LTC2980 and LTM2987

These two devices integrate two separate LTC2977s into a single package. If powered from V_{PWR}, do not connect the $V_{DD33(A)}$ and $V_{DD33(B)}$ pins together. Each V_{DD33} pin has an independent internal regulator. However, if power from an external 3.3V supply is being applied directly to the V_{DD33} pins, tie all V_{PWR} and V_{DD33} pins (A and B sides) together.

Use of CPLD/FPGA with PSM

Best practices: connect V_{OUT_ENn} pins to RUN, connect CPLD enables to LTC297x CONTROL pins.

Caution should be taken when connecting CPLD/FPGA to a power system manager. Decide which device has control of the RUN pins of the DC/DC converters. If the CPLD controls DC/DC converters, it is recommended to configure PSM to monitor-only.

Unprogrammed CPLD/FPGA I/O pins may have unpredictable behavior at first board bring up. Consider adding hardware provisions that allow a way to temporarily disconnect CPLD signals (jumpers/zero ohm resistors that can be removed).

Revision History

REV	DATE	DESCRIPTION	PAGE NUMBER
1	11/14	Initial release.	N/A
2	08/16	Improved readability, added 2980/87 section.	All

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