Honing the Adjustable Compensation Feature of Power System Management Controllers

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INTRODUCTION

This application note introduces methods for tuning the adjustable compensation of the LTC®3886 to achieve optimal phase margin, bandwidth and transient response. The information in this note is applicable to all constant frequency peak current mode power system management controllers (PSMCs) in the ADI family with adjustable compensation. In typical designs using current-mode PSMCs, the device is adapted to the design requirements by manually choosing the capacitors and resistors for the compensation network. PSMCs with adjustable compensation contain internal circuitry that quickly and easily modify the compensation via PMBus, allowing the user to optimize a solution with greater ease. By eliminating the need to make external component changes on the PCB to change loop properties, adjustments to the circuit can be made dynamically to expedite the tuning process.

OVERVIEW

In addition to demonstrating the techniques by which optimal phase margin, bandwidth and transient response time is achieved, this note addresses the trade-offs that come along with adjusting the compensation. The goal is to familiarize the reader with the DC2155A demo board and its supporting software, to develop an understanding of compensation network adjustment and to provide a tuning procedure. The first part of this note examines the compensation design, provides a tuning sequence, explains the PSMC open-loop and closed-loop transfer function and offers some general design advice. The focus of the note then shifts to the effects of adjusting the compensation.

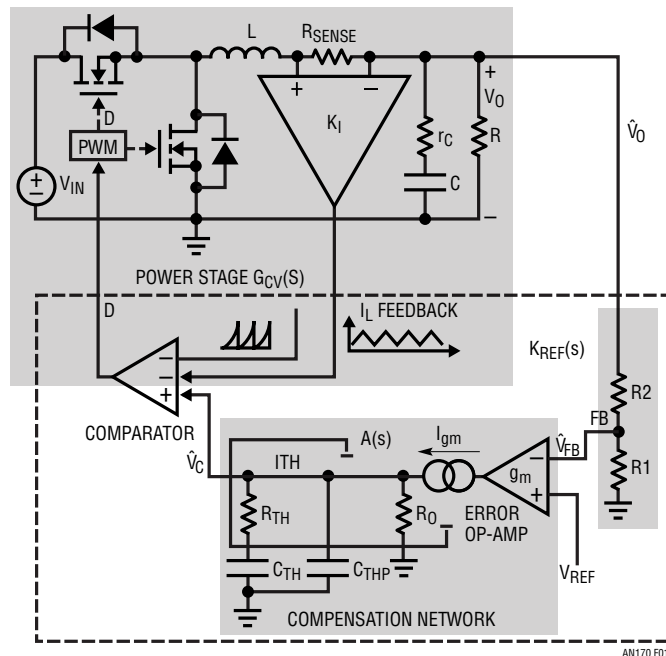All registered trademarks and trademarks are the property of their respective owners.

Figure 1. Block Diagram of Current-Mode PSMC

All measurements were made using LTC3886 Demo Circuit 2155A-A. In addition to the demo circuit, a PICOTEST Common Mode Transformer,[1] PICOTEST Injection Transformer[2] and OMICRON Bode 100 Frequency Analyzer[3] were utilized. A DC1613A USB-to-PMBus controller enabled communication between LTpowerPlay® and the demo circuit. Software including LTpowerCAD®, LTpowerPlay and Bode Analyzer Suite (Bode 100 version) were employed as well.

PROGRAMMABLE TUNING

The compensation network consists of an operational transconductance amplifier (OTA) whose output drives a single capacitor in parallel with a capacitor and resistor in series.
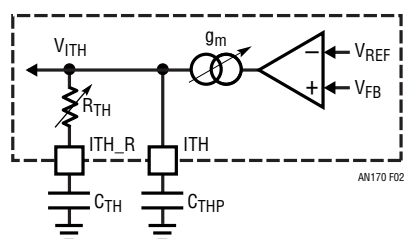
Figure 2. Compensation Diagram. R_{TH} and g_m Internal and Adjustable

The LTC3886 allows the OTA and the value of the resistor (R_{TH} and g_m in Figure 2) to be adjusted, via PMBus using either LTpowerPlay software or Linduino® firmware, to alter the DC gain, gain/phase margins and bandwidth frequency of the voltage loop as well as the controller output impedance. These two parameters—the resistance and gain—are the "knobs" with which the loop is tuned.

In a peak current-mode PSMC, the compensation is part of the voltage loop, which regulates output voltage by setting the peak inductor current. The compensation provides the voltage loop with high DC gain to minimize regulation error, a phase boost near the crossover frequency f_C, and a pole to roll off the gain at high frequencies and to filter out switching noise.

To produce a stable output voltage, a fractional portion of the output voltage is obtained by a resistor divider— $K_{REF}(s)$ in Figure 1—and passed to the inverting node of the OTA to be compared to a stable reference. The difference between the reference and this feedback voltage are the input to the compensation network. The voltage at the output, V_{ITH}, is a function of this input as specified by the compensation transfer function.

In peak current mode PSMCs, at the start of each clock cycle, the top MOSFET turns on and its current charges the inductor. The voltage across the current sense resistor is summed with a slope compensation ramp and compared to V_{ITH}. Once the sum of the slope compensation and sense resistor voltages are equal to V_{ITH}, the peak current comparator turns off the top MOSFET and asserts the bottom MOSFET, discharging the inductor. This process repeats every switching cycle.

Changes in output voltage cause an oppositional change in V_{ITH}. V_{ITH} responds by modifying the peak inductor current. This is observed in the load transient condition shown in Figure 3. The peak inductor current limit tracks V_{ITH}, increasing current supplied to the output load when the output voltage drops and forcing the output voltage to return to the programmed value.
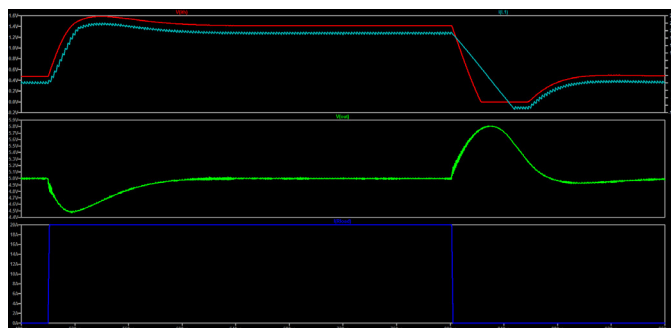
Figure 3. Output Voltage (Green), ITH Voltage (Red) and Inductor Current (Light Blue) in Response to Load Step (Dark Blue)

For a more in-depth explanation of the feedback mechanisms underlying the compensation loop, consult the section on Switching Mode Power Supplies in AN140, "Basic Concepts of Linear Regulator and Switching Mode Power Supplies."[4]

Note 1. Model No: J2102A
https://www.picotest.com/products_J2102A.html
Note 2. Model No: J2101A
https://www.picotest.com/products_J2101A.html
Note 3. OMICRON Bode 100
https://www.omicron-lab.com/bode-100/product description.html
Note 4. http://dcs.linear.com/docs/en/application-note/AN140fa.pdf

BASICS OF TUNING

Using R_{TH} and g_m, the resistance and transconductance of the compensation network, the bandwidth frequency, gain, and phase of the voltage loop can be adjusted. The goal is to make the circuit stable, reduce jitter and react quickly to load and line changes.

Limitations on Bandwidth and Phase Margin

Generally speaking, higher bandwidth and gain corresponds to faster settling time and smaller output voltage perturbation responding to a load step. Notice in Figure 4 and Figure 5, as bandwidth and gain are increased, the magnitude of the voltage dip in response to a load step shrinks. Increasing phase margin improves loop stability, reducing output voltage ringing in response to load changes.

There are, however, practical limitations on bandwidth and phase margin.

Bandwidth is determined mostly by the switching frequency. Bandwidth should be between 1/10 and 1/6 of the switching frequency—this adequately filters out switching noise. Thus, the PWM frequency must be selected prior to tuning the compensation network. The PWM frequency is typically set as fast as possible while maintaining the desired efficiency. However, other factors such as noise, component sizes, or board layout may also factor into the frequency selection.

A compensation network with too much phase margin can significantly slow transient response and one with too little will be unstable. Sixty to eighty degrees of phase margin is ideal, anything approaching ninety degrees can become too slow and anything below fifty can have undesirable oscillations.

Tuning Procedure

Begin tuning with a desired bandwidth in mind, somewhere within 1/10 to 1/6 of the switching frequency. This bandwidth is the operating point about which the loop is tuned, first by optimizing phase margin at that desired bandwidth, and then by adjusting the actual bandwidth (whatever it may be after phase optimization) to be as close to the goal as possible.

- **Step One:** Optimize phase margin at the desired bandwidth frequency by adjusting R_{TH}.

- **Step Two:** Move the crossover frequency as close as possible to the desired bandwidth by adjusting g_m.

As will be explained in the next section, compensation transfer function, R_{TH} and g_m affect the loop transfer in different ways and therefore have different roles in the tuning process.

COMPENSATION TRANSFER FUNCTION

The compensation network is a Type II amplifier circuit with open loop gain A(s) and impedance $Z_{ITH}(s)$.

$$A(s) = \frac{V_{ITH}(s)}{V_{FB}(s)} = g_m \bullet Z_{ITH}(s)$$

The large capacitor C_{TH} in parallel with the OTA's finite output impedance R_O defines a low frequency pole. This pole introduces −90 degrees of phase shift, which when added with the −180 degrees phase shift inherent in negative feedback and the −90 degrees from output capacitor in the power stage model $G_{CV}(s)$[5] makes the loop unstable.

To boost phase, a zero is created by adding a resistor R_{TH} in series with C_{TH}. While this resistor is necessary for stability, it also significantly increases the voltage loop bandwidth. This has the potential to introduce switching noise into the voltage loop. To minimize this, a small capacitor C_{THP} is added in parallel. This increases the gain margin and filters out high frequency noise.

$$A(s) = g_m \bullet R_O \bullet \frac{1 + \dfrac{s}{s_Z}}{\left(1 + \dfrac{s}{s_{P0}}\right) \bullet \left(1 + \dfrac{s}{s_{P1}}\right)}$$

where,

$$s_{P0} = \frac{1}{R_O \bullet C_{TH}} \quad s_Z = \frac{1}{R_{TH} \bullet C_{TH}} \quad s_{P1} \cong \frac{1}{R_{TH} \bullet C_{THP}}$$

Changing R_{TH} affects the location of the zero and high frequency pole, and thus the mid-band gain as shown

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Note 5. At low frequency, the power stage, PWM and output filter can be modeled as a first order system. See the appendix or AN149 for an explanation.

in Figure 4. A larger R_{TH} leads to greater mid-band gain, which can produce a better transient response. It also increases bandwidth, but simultaneously moves the zero and its accompanying phase boost in the opposite direction toward DC. Likewise, decreasing R_{TH} will increase the phase boost frequency as the bandwidth decreases. Use R_{TH} to move the location of the phase boost so that phase is maximized at the desired bandwidth frequency. The key to stabilizing the circuit with R_{TH} is lining up the maximum phase boost with the desired crossover frequency.

a)

b)
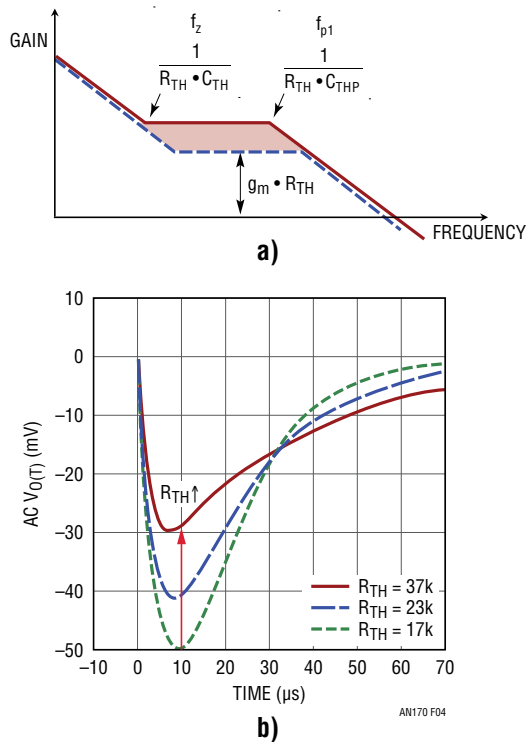
Figure 4. Effects of R_{TH} on Transfer Function and Load Transient

The transconductance of the error amplifier, g_m, doesn't influence the phase of the open-loop transfer function because it doesn't influence pole or zero locations. It scales the open-loop gain up or down. Modifying the open-loop gain changes the crossover frequency proportionally. Use g_m to change f_C as needed. Keep in mind, although phase doesn't change, changing f_C will change the phase margin.

A more detailed, step-by-step analysis of the open-loop compensation transfer function and of current-mode loop modeling can be found in AN149, "Modeling and Loop Compensation Design of Switching Mode Power Supplies."[6]

a)

b)
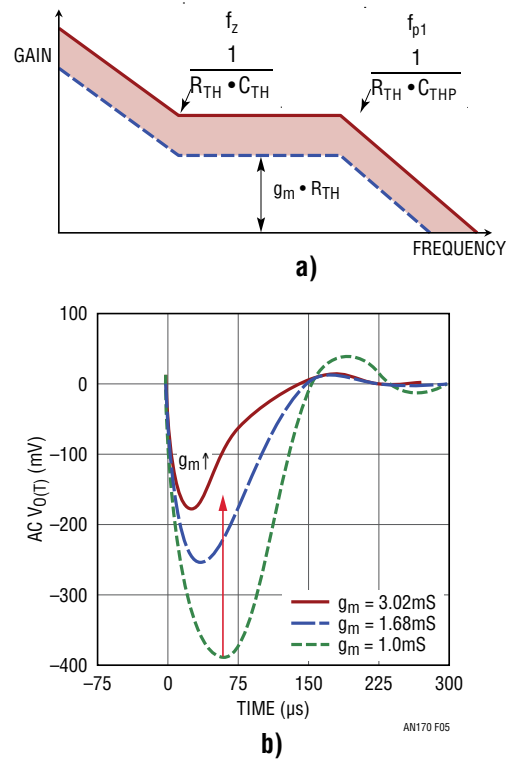
Figure 5. Effects of g_m on Transfer Function and Load Transient

OPEN AND CLOSED LOOP TRANSFER

The previously mentioned effects of changing R_{TH} and g_m apply only to the open-loop transfer function. However, the closed-loop transfer function is influenced by the open-loop transfer function, making it worthwhile to understand the open-loop effects.

The open-loop gain of the voltage loop, T(s), is the product of the open-loop gains of each of its three major parts: the compensation network, the feedback divider and low pass output filter (in this note referred to as "power stage").

$$T(s) = A(s) \bullet K_{REF}(s) \bullet G_{CV}(s)$$

where A(s), $K_{REF}(s)$ and $G_{CV}(s)$ are the open-loop gains of the compensation network, feedback divider and power stage respectively. Figure 6 is a simplified closed-loop model of a buck switching regulator including power stage, resistor divider and compensation blocks.

an170f
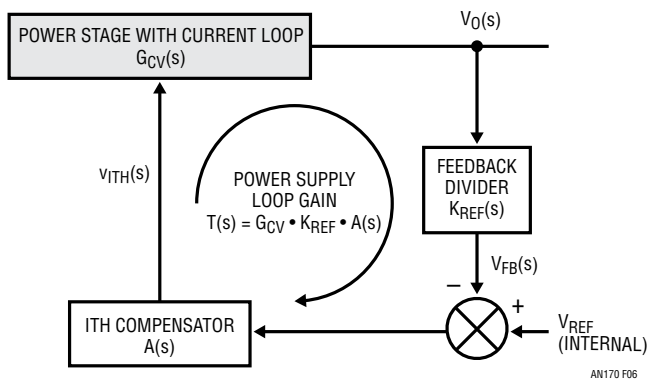
Figure 6. Control Block Diagram for Feedback Loop Design

For the purposes of this app note, the power stage is modeled as a first order system and does not reflect the phase delay associated with the sample and hold inherent in switching supplies, thus the model is only accurate up to 1/50 the switching frequency. The model is sufficiently accurate to allow the reader to understand the effects of adjusting R_{TH} and g_m when tuning. LTpowerCAD utilizes a more accurate frequency model and will allow the user to optimize the compensation network with better accuracy. Final optimization requires a working board. The user can adjust the compensation network to address board and component issues not fully modeled. Diagrams and transfer functions of the first order model of $G_{CV}(s)$ and of $K_{REF}(s)$ can be found in the appendix.

The closed-loop case is more complicated.

$$G(s) = \frac{1}{K_{REF}(s)} \bullet \frac{T(s)}{T(s)+1}$$

where G(s) is closed-loop gain from the reference voltage to the output. If open-loop gain T(s) is very large, then the transfer between V_{OUT} and V_{REF} can be almost entirely accounted for by the resistor divider, meaning that there is very low output error.[7] An infinite open loop gain would imply no output error.

At frequencies far below its unity gain bandwidth, T(s) should be much greater than one. This allows a term to be simplified.

$$\frac{T(s)}{T(s)+1} \approx 1 \text{ (when } f \ll f_C)$$

Note 7. In the LTC388X, a servo also corrects DC regulation errors to guarantee 0.5% accuracy.

At frequencies far above its unity gain bandwidth, open loop gain drops such that T(s) ≪ 1.

$$\frac{T(s)}{T(s)+1} \approx T(s) \text{ (when } f \gg f_C)$$

This leads to the asymptotic equations for G(s).

$$G(s) \approx \frac{1}{K_{REF}(s)} \text{ (when } f \ll f_C)$$

$$G(s) \approx \frac{T(s)}{K_{REF}(s)} = A(s) \bullet G_{CV}(s) \text{ (when } f \gg f_C)$$

The closed-loop compensation gain is $A_C(s) = G(s)/G_{CV}(s)$. Applying the same asymptotic simplification as before, the approximations of the closed-loop compensation transfer are:

$$A_C(s) \approx \frac{T(s)}{K_{REF}(s) \bullet G_{CV}(s)} \text{ (when } f \ll f_C)$$

$$A_C(s) \approx \frac{T(s)}{K_{REF}(s) \bullet G_{CV}(s)} = A(s) \text{ (when } f \gg f_C)$$

In the low frequency range, neither G(s) nor $A_C(s)$ are functions of A(s), and therefore R_{TH} and g_m don't have an effect on the gain or phase. In this range, G(s) has a gain fixed by the inverse of the resistor divider gain, which is flat across low frequency. This is shown in Figure 7, which has feedback divider ratio of 10x. The single low frequency
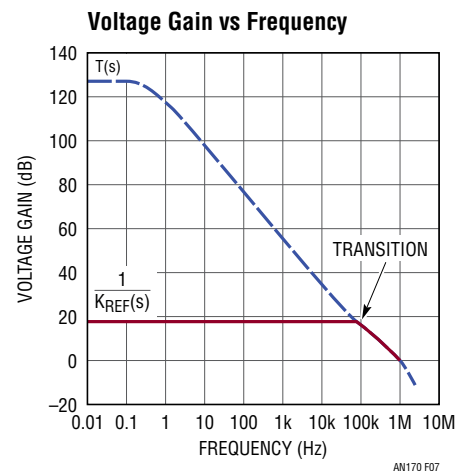
Figure 7. Relationship Between Closed-Loop and Open-Loop Gain

pole from $G_{CV}(s)$ gives $A_C(s)$ a 20dB/decade slope and a 90-degree phase boost because it's in the denominator, and the curve is shifted by the inverse of $K_{REF}(s)$.

In the high frequency asymptote, the effects of g_m and R_{TH} are observable and predictable. Adjustments to R_{TH} affect bandwidth and the location of the phase boost. R_{TH} adjustment moves the mid-band gain segment up and left or down and right when increased or decreased, respectively. The OTA gain g_m simply scales $A(s)$, and therefore proportionally scales $T(s)$. It doesn't affect poles or zeroes. Changing g_m simply shifts the gain curve of the controller and compensation vertically.

The asymptotic approach is only sufficient for explaining the behavior of the gain and phase far from the unity gain bandwidth. What happens at the unity gain bandwidth and does adjusting compensation affect it? Changes to compensation affect the frequency location and behavior of the curve at the transition point, the point when $f = f_C$.

$$\frac{T(s)}{T(s)+1} = \frac{1}{2} \text{ (when } f = f_C)$$

The compensation network changes the transition frequency because it affects the open-loop bandwidth. At the bandwidth frequency $T(s) = 1$, so gain is reduced by 3dB and phase lags by 45 degrees because of the ½ multiplying $1/K_{REF}(s)$. By changing f_C, this distinctive transition point can be moved.

Changes to R_{TH} influence peaking observed at the transition frequency in the gain graph. Both the controller and compensation network closed-loop gains indicate peaking around the crossover frequency. This peaking is caused by the $T(s)/(T(s)+1)$ term and is a function of phase margin. For an explanation of why a larger R_{TH} causes less peaking, consult the appendix.

DESIGN CONSIDERATIONS

When designing with a PSMC, there are many decisions that come prior to choosing the compensation network components. These include whether to use inductor DCR or resistor current-sensing, the switching frequency of the current loop, power MOSFET selection, input and output capacitor size, inductor size, voltage range, and current range. All of these decisions involve trade-offs between size, cost, efficiency and performance. The LTpowerCAD program makes testing these choices easy, and is a suggested first step in the design process. Once components have been defined and a switching frequency selected, the compensation network can be optimized. For more detail on design trade-offs in switch mode power supplies refer to the section "Design Considerations of the Switching Power Components" in AN140.[8] The "Applications Information" section of the LTC3886 data sheet covers these choices as well. Nevertheless, the non-adjustable components most relevant to loop tuning are considered briefly in this section.
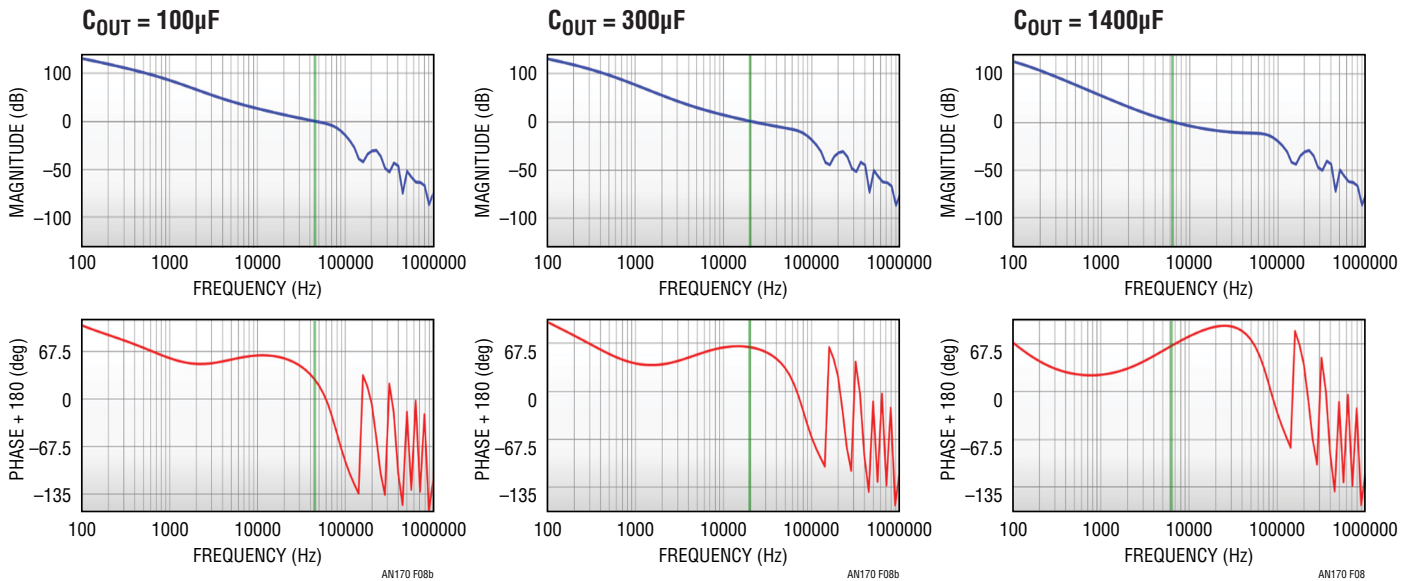
Output Capacitor C_{OUT}

The output capacitor has significant effects on loop phase and gain because it influences the transfer function of the power stage. A larger output capacitance lowers the frequency of the single power stage pole and a smaller output capacitance increases the pole frequency. Because this pole is typically at a low frequency in comparison to the unity gain bandwidth, changes to C_{OUT} have minor influence on the phase curve. However, the frequency location of this pole has a substantial effect on the bandwidth and therefore phase margin. Large output capacitance reduces bandwidth and small output capacitance increases bandwidth.

The capacitor series resistance, ESR, also has a large impact on the output voltage ripple and the associated power stage zero can affect the compensation network. The output capacitors are placed in parallel to minimize the overall ESR so that the zero is at very high frequency, beyond the point where it influences the tuning procedure. To understand the direct effects of ESR on power stage transfer, consult the appendix entry on power stage transfer.

Despite the reduction in bandwidth, it's desirable to have a larger output capacitance. A large output capacitance improves transient response because it stores more charge to supply the load during a load transient and it also reduces output voltage ripple.

$$\Delta V_{OUT} \approx \Delta I_{L(P-P)} \bullet \left(ESR + \frac{1}{8 \bullet f_S \bullet C_{OUT}} \right)$$

Note 8. http://dcs.linear.com/docs/en/application-note/AN140fa.pdf.

$C_{OUT} = 100\mu F$ $C_{OUT} = 300\mu F$ $C_{OUT} = 1400\mu F$

Table 1.

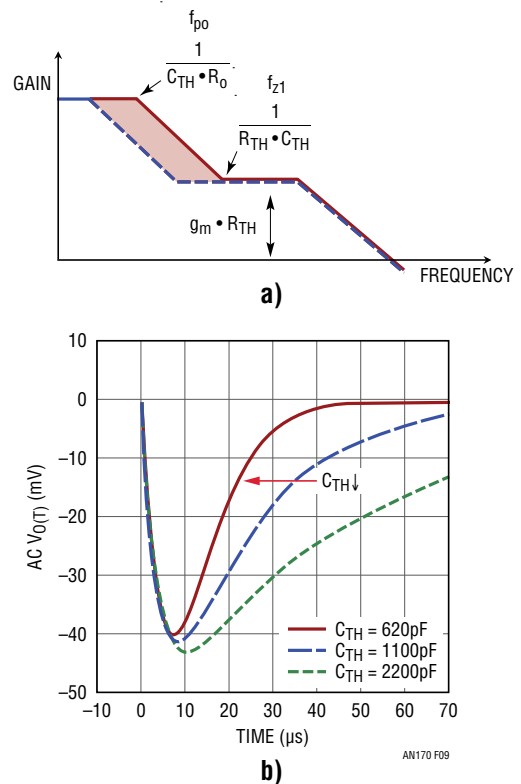| C_{OUT}	100µF	300µF	1400µF
Bandwidth (kHz)	44.67	19.95	6.31
Phase Margin	26.26	61.1	63.77

Figure 8. Open-Loop Gain and Phase of DC2155A-A Simulation as C_{OUT} Is Varied (ESR Assumed to Be Zero)

where f_S is the PWM switching frequency. A nominal value of output capacitance is between 300µF and 500µF, but this can vary greatly depending on the application. Refer to Figure 8 to see how C_{OUT} modifies the loop transfer.

Compensation Capacitors C_{TH} and C_{THP}

Generally, C_{TH} should be about a factor of ten larger than C_{THP}. This gives sufficient separation between the zero and high frequency pole as well as adequate mid-range gain and phase boost.

Changing C_{TH} affects the location of the low frequency pole and the zero of the compensation network. Shrinking C_{TH} increases low to mid frequency gain, improving transient response. Like all things, this comes with a trade-off: moving the zero closer to the high frequency pole reduces the size of the phase boost near the crossover frequency that is crucial to loop stability. Increasing C_{TH} does the opposite: increase phase boost at the cost of low frequency gain. No change in bandwidth occurs as a result of changing C_{TH}.

f_{po}
$$\frac{1}{C_{TH} \bullet R_o}$$

f_{z1}
$$\frac{1}{R_{TH} \bullet C_{TH}}$$

$g_m \bullet R_{TH}$

a)

$C_{TH}\downarrow$

$C_{TH} = 620pF$
$C_{TH} = 1100pF$
$C_{TH} = 2200pF$

b)

Figure 9. Conceptual Effect of C_{TH} on Compensation Gain and Loop Transient

C_{THP} affects the location of the high frequency pole. Increasing C_{THP} decreases the bandwidth and phase boost. Shrinking C_{THP} increases bandwidth and phase margin, meaning better transient response and stability to a point. However, if C_{THP} is too small, it no longer filters switching noise.
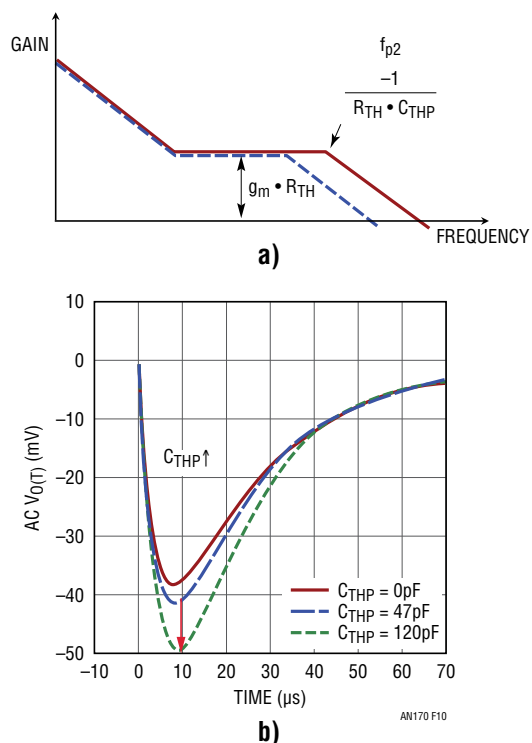
Figure 10. Conceptual Effect of C_{THP} on Compensation Gain and Loop Transient

Capacitor values are typically around 3nF to 10nF for C_{TH} and 100pF to 500pF for C_{THP}, but these can vary significantly depending on other design choices.

Current and Voltage Ranges

In the LTC3886 there are two voltage ranges, V_{OUTR0} (high) and V_{OUTR1} (low), and two current ranges, set by $V_{I(ILIMIT)}$. These variables can be found on page 5 of the LTC3886 data sheet. The voltage range determines the feedback resistor divider gain $K_{REF}(s)$. The current range sets the V_{ITH} to peak current limit gain.

Once the voltage and current ranges are fixed, changes to the output voltage or current limit will not affect gain and therefore do not require retuning.
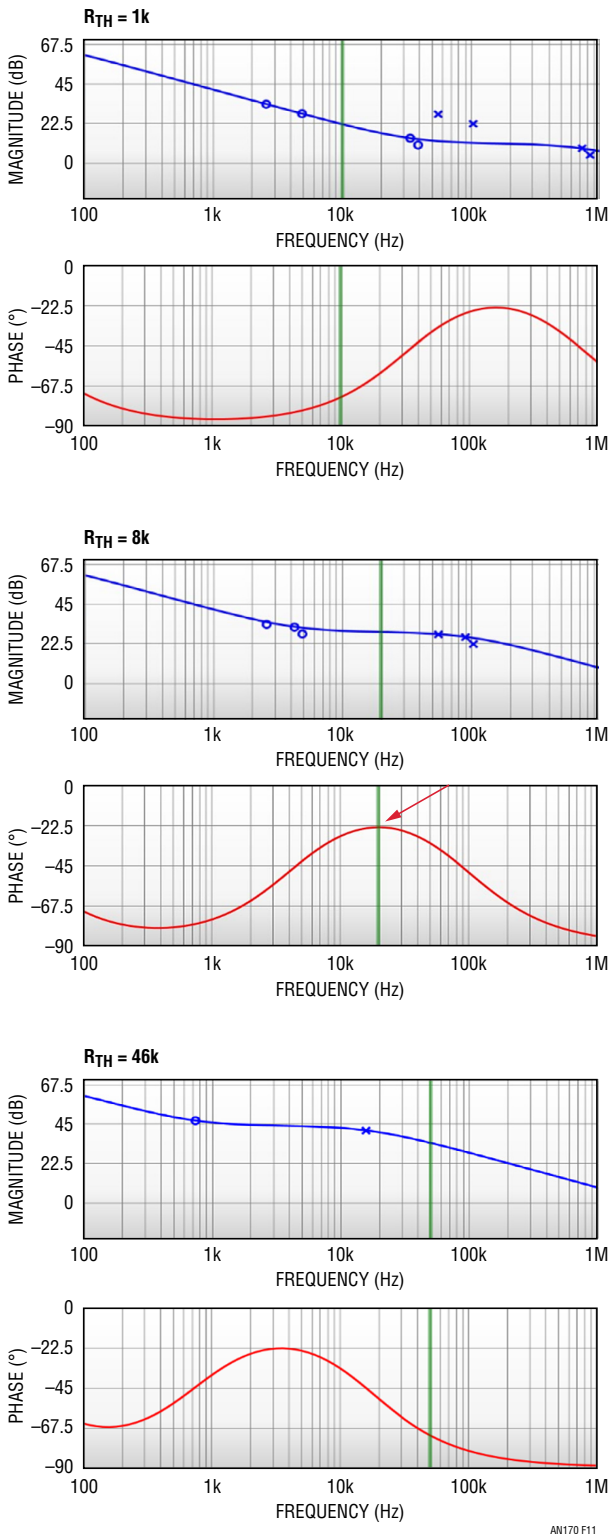
SIMULATION

The LTpowerCAD design tool allows easy optimization of loop compensation, and is a good starting point for testing a design. It can generate accurate gain, phase and impedance plots for the loop, compensation or power stage. The graphs in Figures 11, 12, 14 and 15 were produced using LTpowerCAD, and are exceptionally accurate thanks to Linear's circuit model for current-mode control [5]. Note that the vertical green line indicates the loop bandwidth.

Open LTpowerCAD and start a new "Supply Design." Specify a "Buck" converter topology and "All" for converter type. Indicate two output rails and then enter 3886 for the part number. Output voltage and current are arbitrary and the minimum, nominal and maximum input voltages can be found in the demo circuit manual. Open up a Linear (not Excel) design for the dual-output LTC3886.

The DC2155A-A uses a current sensing resistor, so once the design page has been opened, toggle the button on the LTC3886 to make sure the schematic is in this configuration. Either input unique values or copy the values from the DC2155A-A schematic for the components.

Figure 11. DC2155A Simulation of Compensation Open-Loop Gain and Phase as R_{TH} Is Increased Top to Bottom; Vertical Green Line Indicates Loop Crossover Frequency
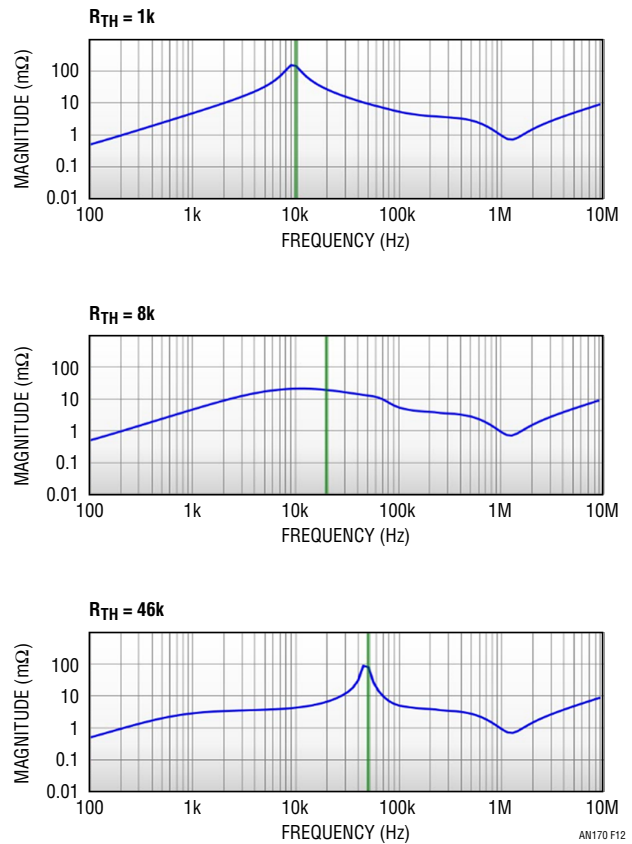
Figure 12. DC2155A Simulation of Controller Closed-Loop Output Impedance as R_{TH} Is Increased Top to Bottom

Table 2.

R_{TH}	1k	8k	46k
Bandwidth (kHz)	10.00	19.95	50.12
Phase Margin	15.41	61.10	−7.87

LTpowerCAD has an auto-compensation feature shown in Figure 13 that calculates compensation values given desired bandwidth, phase margin and gain margin. These values are a good starting point. They are found in the left-hand control panel when viewing the "Loop Comp. and Load Transient" panel.
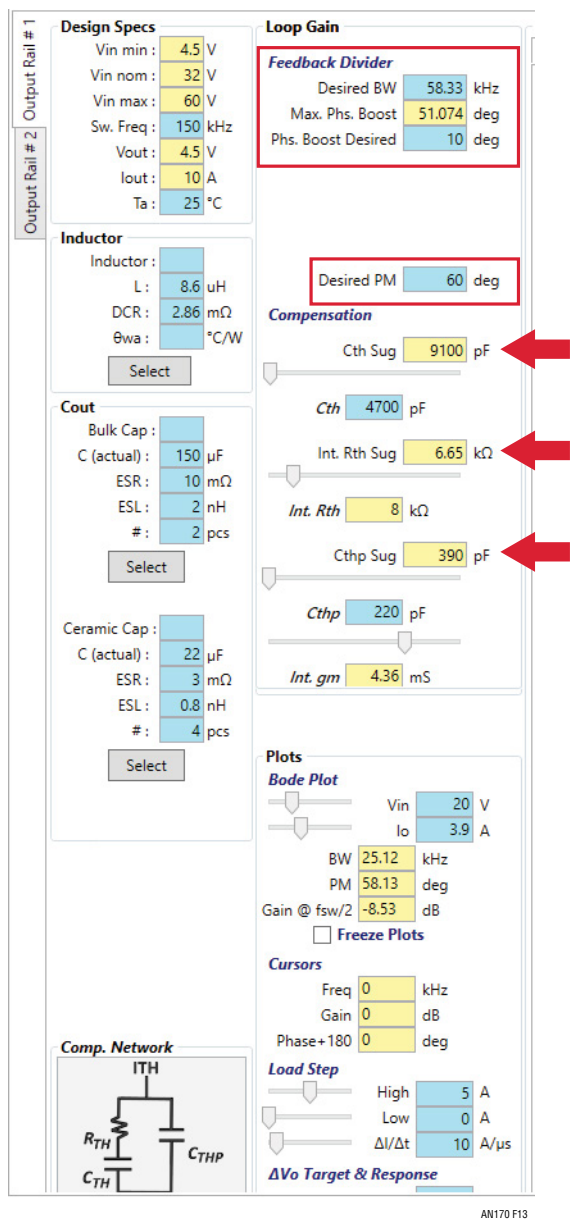
Figure 13. Auto-Compensation in PowerCAD

Step 1: Phase Adjustments with R_{TH}

On the design page, set g_m to some nominal value such as 3.02mS and begin with R_{TH} at a low value such as 1kΩ. Go to the tab "Loop Comp and Load Transient" to observe the open loop gain and phase, and take note of the phase margin, bandwidth and transient response. Make sure the correct output rail is being observed. The phase margin is likely very low, and thus the transient response most

likely indicates severe ringing and oscillation. Increase R_{TH} incrementally and observe the gain, phase, impedance and transient graphs again to see how they've changed. Mid-band gain and bandwidth should increase and the phase boost should shift lower in frequency as the crossover frequency increases. Position the phase boost so that the phase is optimal at the desired crossover frequency. Hopefully, the actual crossover frequency f_C is reasonably close to what is desired. An ideal situation would look something like the second image in Figure 11, noted by the red arrow; if the desired bandwidth is ~20kHz, then hardly any tuning of f_C for step two will be required.

Step 2: Bandwidth Adjustments with g_m

Once the outer pole and zero have been correctly adjusted and the phase margin has been optimized at the desired bandwidth frequency, use g_m to adjust the crossover frequency to the desired bandwidth frequency. Changing g_m doesn't change phase, so this allows manipulations of the crossover frequency without affecting the optimized phase. For example, consider the plots in Figure 14. Suppose that phase has been optimized at 20kHz and that the user then adjusts bandwidth using g_m. The middle figure of Figure 14 results if the loop is successfully tuned, because the crossover frequency has been moved to the desired bandwidth where phase has been optimized.

Once R_{TH} and g_m have been selected, examine the impedance plot. If there is sufficient gain and bandwidth the output impedance should be low and flat over the entire frequency range. Likewise, if phase margin is sufficient, there should be no substantial peaking in the impedance. If that is not the case, the bandwidth and phase margin specifications should be reconsidered and the previously described tuning procedure should be re-run targeting a lower crossover frequency.

If Tuning is Unsuccessful…

If changing R_{TH} and g_m don't provide acceptable stability or response time, initial design choices may have to be reconsidered. Review the "Design Considerations" section once more and make changes to the inductor, C_{OUT}, C_{TH}, C_{THP}, the voltage or current range, or switching frequency.
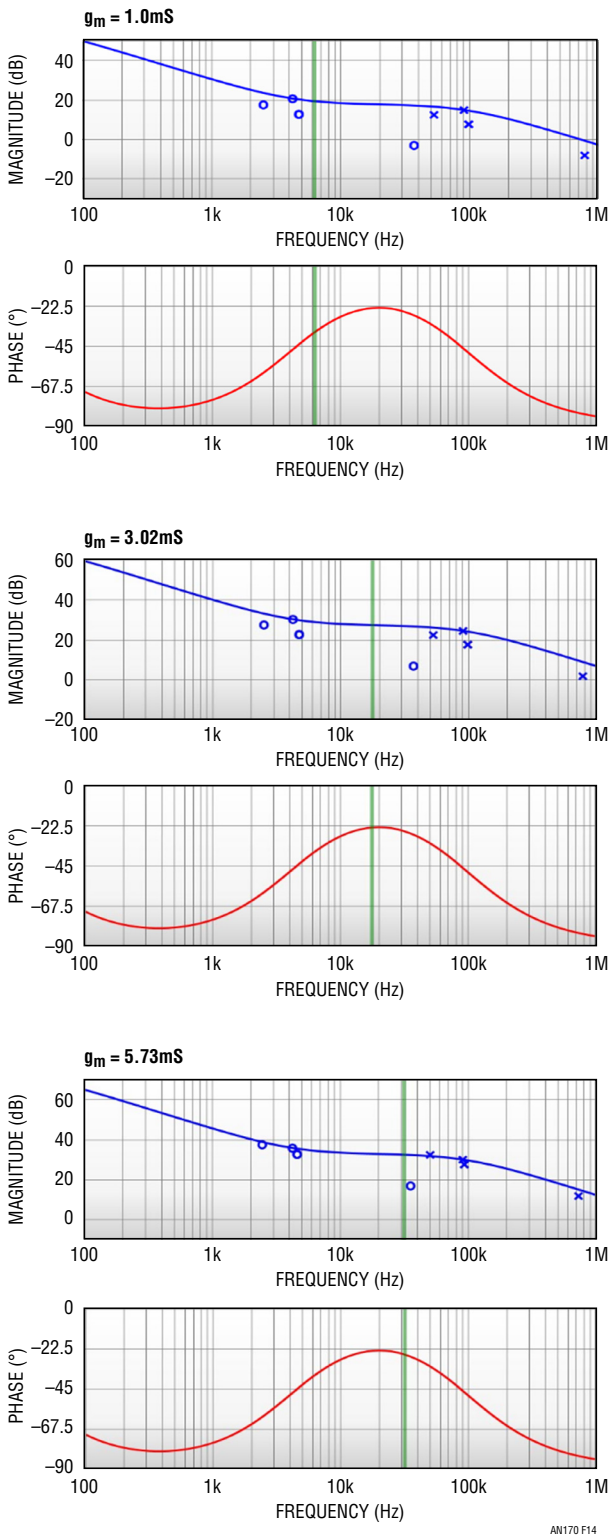
Figure 14. DC2155A Simulation of Compensation Open-Loop Gain and Phase as g_m Is Increased Top to Bottom; Vertical Green Line Indicates Loop Crossover Frequency
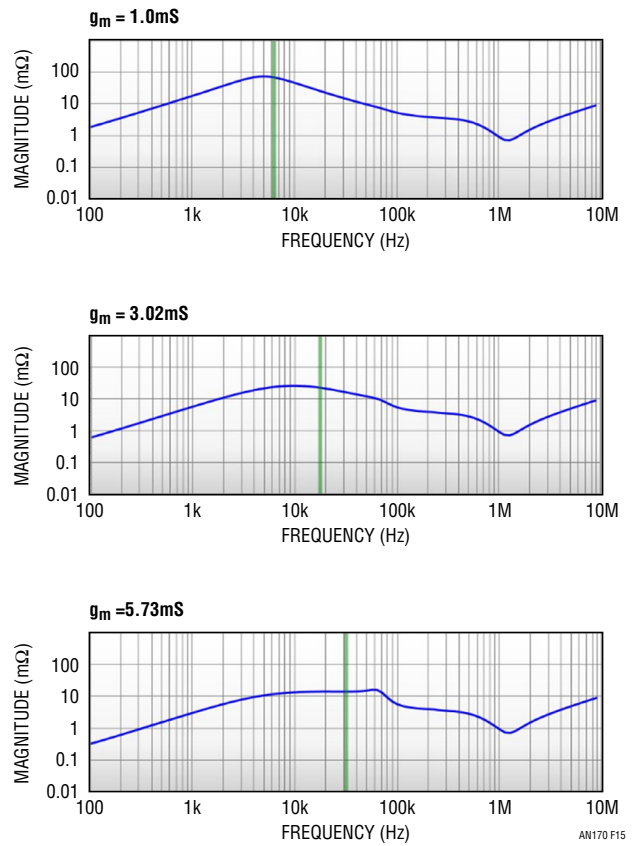
Figure 15. DC2155A Simulation of Controller Closed-Loop Output Impedance as g_m Is Increased Top to Bottom

Table 3.

g_m	1.0mS	3.02mS	5.73mS
Bandwidth(kHz)	6.31	17.78	31.62
Phase Margin	54.79	61.93	53.00
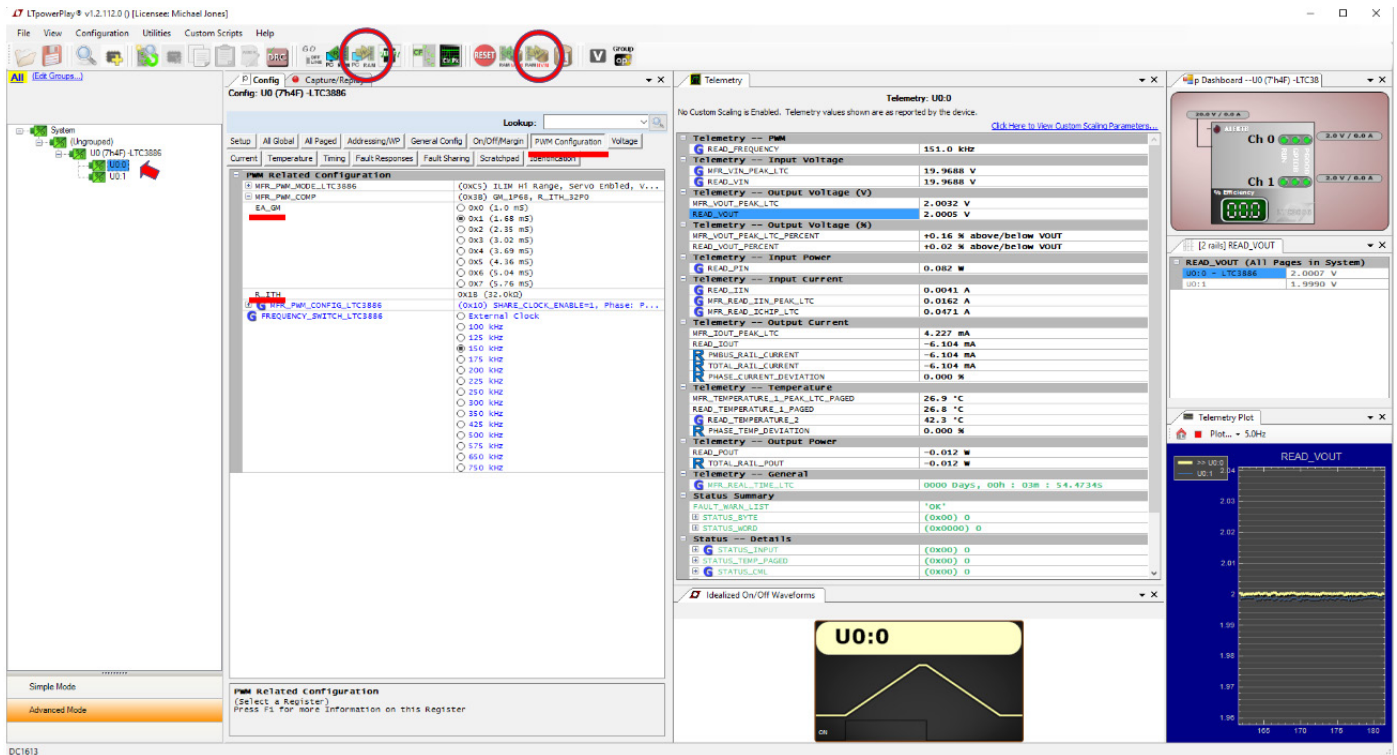
Figure 16. LTpowerPlay GUI — Adjusting Compensation

ADJUSTING DC2155A-A COMPENSATION USING LTPOWERPLAY

NOTE: All examples and measurements in the following sections were made using the DC2155A-A. Consult the DC2155A-A Info Page[9] to become familiar with the board's layout and properties.

See the Quick Start section in the DC2155A Demo Manual to get the board up and running. The following sections are designed to provide an understanding of how changing the resistance, R_{TH} and error amplifier transconductance, g_m, of the compensation network affects:

1. Phase/Gain Margin
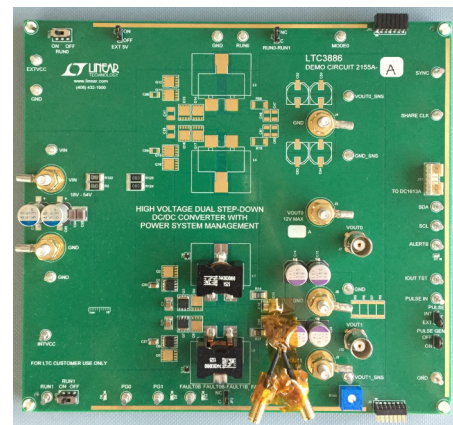
2. Transient Response

3. Output Impedance

4. Jitter

Figure 17. DC2155A-A

For all tests, it's helpful to have the demo circuit connected to the DC1613A and LTpowerPlay running in order to monitor system behavior via the GUI's telemetry readings and to adjust the LTC3886 compensation. To adjust the compensation, select the output channel on the left-hand tree and go to the "PWM Configuration" tab. Drop down the "MFR_PWM_COMP" menu and adjust the internal

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resistance R_ITH and gain EA_GM as desired. Click the "PC RAM" button in the toolbar to make the changes on the board. To save these settings to non-volatile memory, press the button labeled "RAM NVM." These buttons are marked by circles in Figure 16.

To adjust output voltage, go to the "All Paged" tab and double click the value at "VOUT_COMMAND" and type in a new value. Use the "PC RAM" and "RAM NVM" buttons to make the changes as before.

Support for this software can be found at the LTpowerPlay website.

PHASE/GAIN MARGIN

Frequency domain analysis provides an informative analysis of a control loop. By evaluating the system in the frequency domain, the compensation network can be optimized. This analysis gives information on any resonances or sensitivities the loop has and enables the user to visualize the gain and stability changing with input

Figure 18. R45 and R17

or compensation components. However, a drawback of frequency domain analysis is that stability and transient response time cannot be seen first-hand; any notions of response time or stability can only be inferred. A transient analysis must be performed to assure the compensation network is optimized.

To measure gain and phase of the DC2155A-A using the Bode 100, first download and open the Bode Analyzer Suite program. Under the "Vector Network Analysis" tab, start a Gain/Phase measurement. Connect the probes as shown in Figure 19 and run a "full-range" calibration. Check the accuracy of the calibration by leaving the probes connected as they were during calibration and run a single test. The gain and phase should both flat-line at zero.

Before a measurement can be performed, resistor R17 on the demo board must be changed. The resistor R17 is 0Ω by default; to prevent shorting the leads where signal injection occurs, replace R17 with a 5Ω resistor. 5Ω is small enough that it will not impact the loop transfer appreciably. See the schematic for a better understanding of why this is necessary.

This frequency analysis technique is not unique to the DC2155A. In any loop, a suggested method for measuring is to separate the injector probes by some small resistance such as 5Ω. It doesn't matter where in the loop the signal is injected.
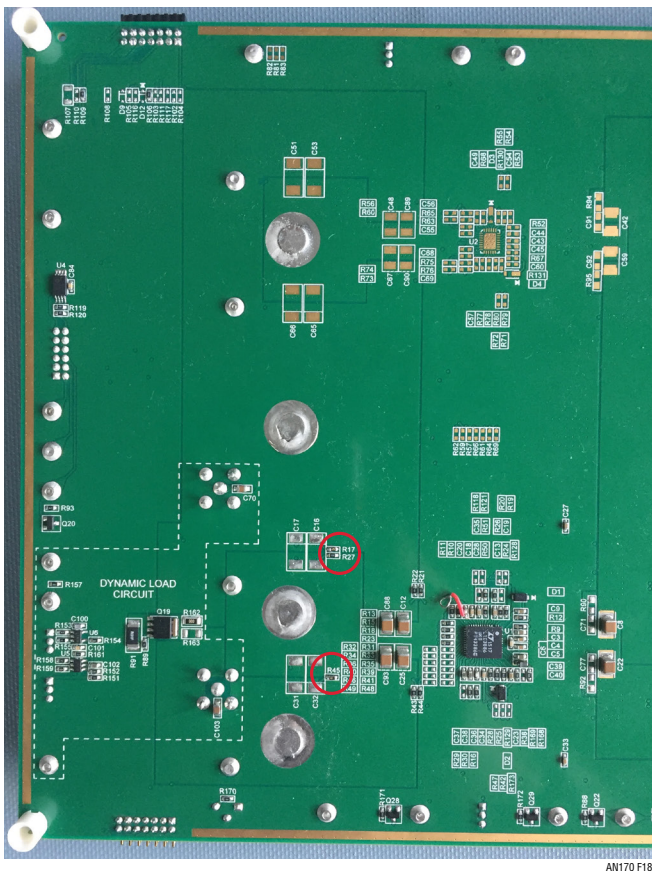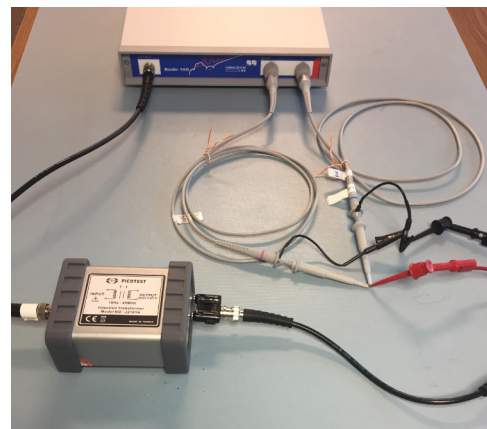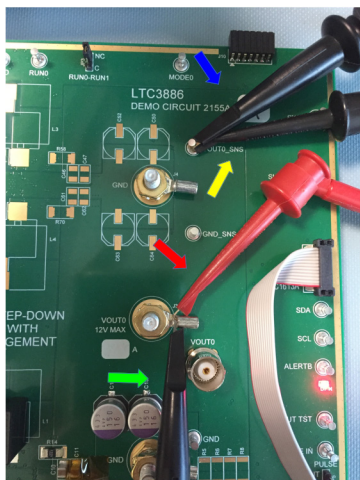

Figure 19. Gain Calibration Set-Up
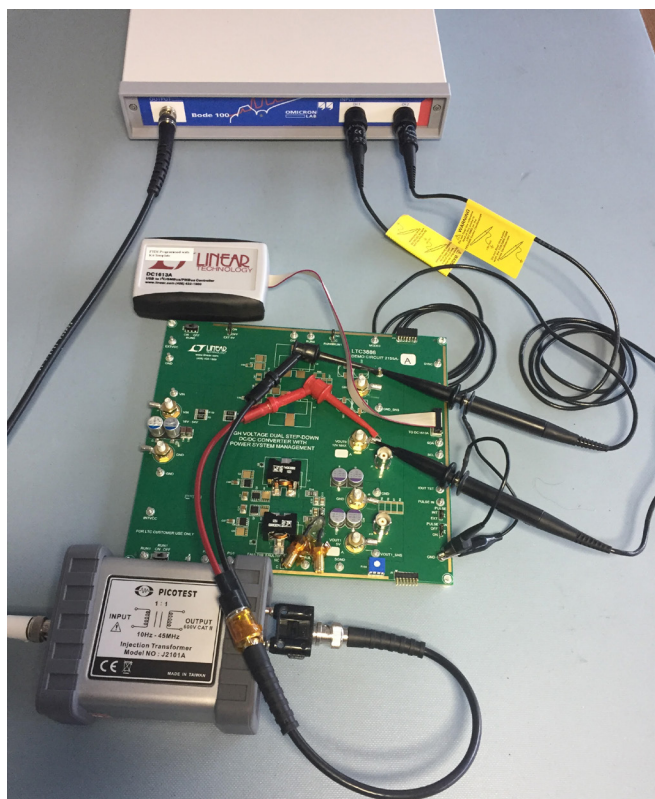
Closed-Loop Controller Measurement

Connect the Bode 100 to the demo circuit as shown in Figure 20. The Bode 100 performs a frequency sweep and the two probes measure the voltage at their leads, dividing them to give the gain and phase. The injector's red output

Figure 20a. Set-Up for Controller Measurement: Injector Output (Red), Injector Output (Yellow), Input Probe/CH2 (Green), Output Probe/CH1 (Blue)
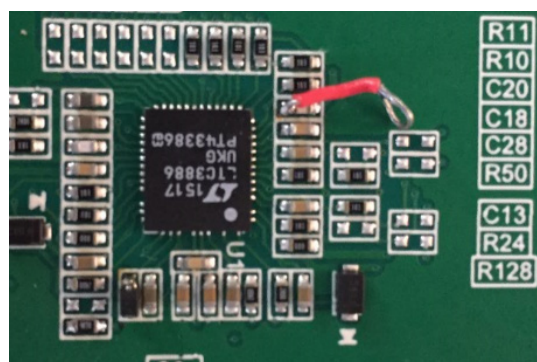

Figure 20b. Controller Measurement Set-Up

goes on VOUT0 and its black output on VOUT0_SNS. The CH 2 probe measures input, so connect that to VOUT0 and the CH 1 probe, which measures output, to VOUT0_SNS. Connect the ground leads to the GND turrets on the demo board.

To evaluate the frequency response of Channel 1, replace R45 with a 5Ω resistor and follow all the same instructions except monitor Channel 1 using VOUT1 and VOUT1_SNS.

Because VOUT0 is a very low impedance node and the input impedance to the LTC3886 at VSNSP0 is nominally 150kΩ, the impact of the 5Ω resistor R17 is minimal.

Closed-Loop Compensation Measurement

For measuring the gain and phase of the error amplifier and compensation, the set-up is the same as the controller measurement except that the output probe (CH 1) must be attached to ITH0, the output voltage of the compensation. To measure this, solder a wire to the pad of C20 connected to I_{TH0}. An example of a lead to which the probe can be attached is shown in Figure 21.


**Figure 21. Lead Connection for Compensation Measurement; Attach Output Probe (CH1) Here**

Tuning Approach

Set up the Bode 100 to measure the controller voltage loop. As with the simulation, optimize phase by adjusting R_{TH}. Starting with a low value, increase R_{TH} until the gain peaking at the transition point is eliminated. This is shown in Figure 22. As R_{TH} is increased, the phase boost moves lower in frequency as the crossover frequency increases. Set the phase as desired at the objective crossover frequency. Make sure that no audible ringing is heard as the injection transformer sweeps; audible ringing is an indication of instability and low phase margin.
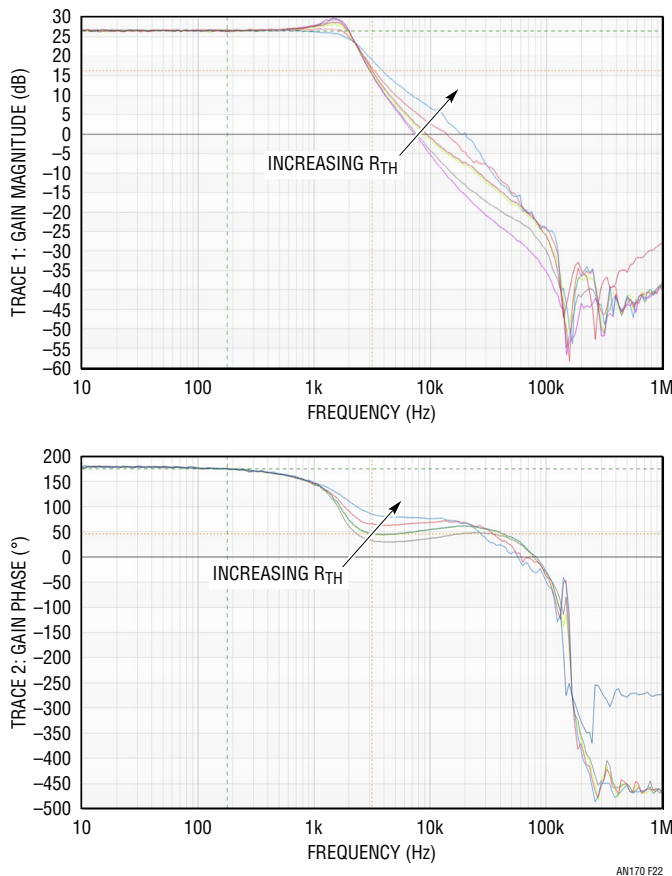
Figure 22. Closed-Loop Controller Gain and Phase Over Range 10Hz to 1MHz as R_{TH} Is Increased (1, 2, 4, 8, 15)
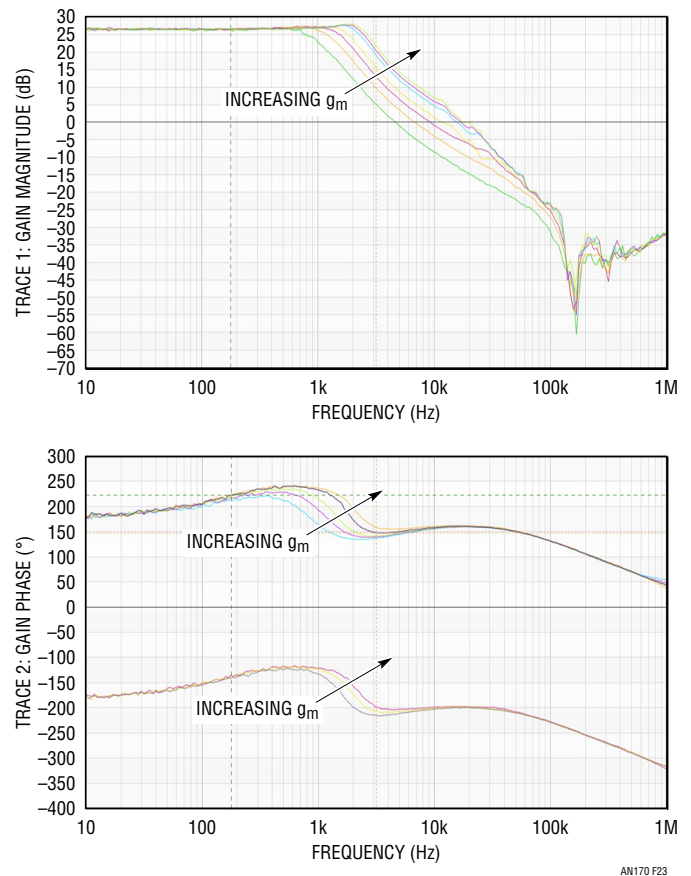
Figure 23. Closed-Loop Controller Gain and Phase Over Range 10Hz to 1MHz as g_m Is Increased (1.0, 1.68, 2.35, 3.02, 3.69, 4.36, 5.04, 5.73)

In closed-loop, g_m does affect phase, but typically not near the crossover frequency. Changes to g_m will affect the unity gain of $T(s)$, and therefore the frequency at which

$$\frac{T(s)}{T(s)+1} = \frac{1}{2}$$

and phase lags by 45 degrees. Figure 23 graphically illustrates that the transition point where phases diverge occurs at lower frequencies than the crossover, and that they converge before the crossover frequency. Thus, as with the open-loop analysis, use g_m to manipulate the crossover frequency to the desired value.

TRANSIENT RESPONSE

While frequency analysis is a great way to get an intimate understanding of the PSMC, time domain analysis is a more intuitive and direct measurement of how the PSMC will respond to load transients. It is also the easier to measure.

To measure transient response, start by setting JP5 to EXT and JP6 to OFF (these located are just below PULSE IN on the right side of the board, between the red and yellow arrows in Figure 24). This disconnects the internal pulse generator from the gate of the n-channel MOSFET load. Now an external gate voltage can be applied. The MOSFET drain is connected to VOUT0 and its source is connected
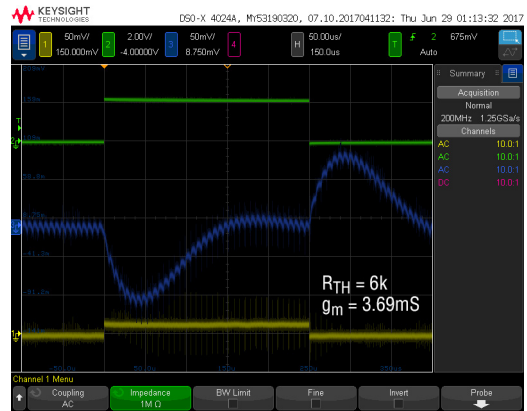
through a 0.01Ω resistor to GND. Set a function generator to output a rectangular pulse at no more than a 5% duty cycle—any more can cause thermal runaway and damage the MOSFET. Initialize the amplitude of the pulse at 1V, and connect the output lead to the PULSE IN probe. Using a
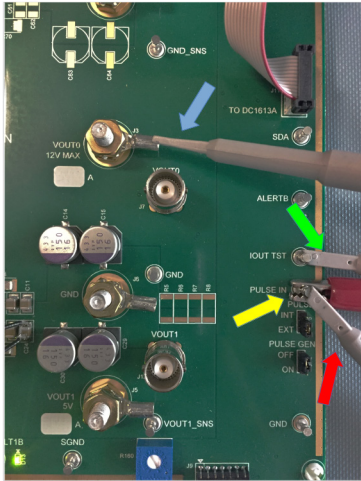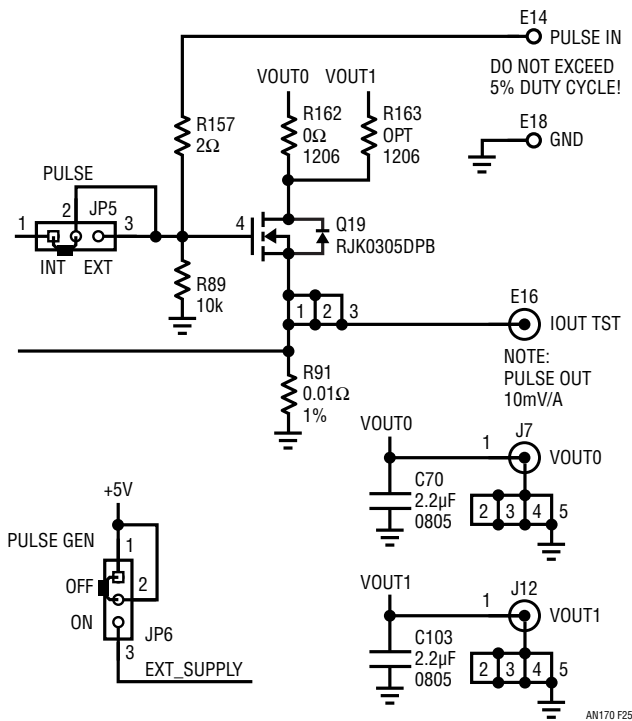

Figure 24. Set-Up for Load Transient Measurement: CH1 (Blue), CH2 (Green), CH3 (Red), Signal Generator Input (Yellow)

Figure 25. Transient Pulse Schematic

multi-channel oscilloscope, connect Channel 1 to PULSE IN, Channel 2 to V_{OUT} and Channel 3 to IOUT TST. Configure Channel 1 and Channel 2 to be AC coupled. Channel 3 should be DC coupled because it is ground referenced. Channel 2 displays the transient response of the output voltage and Channel 1 shows the pulse coming from the function generator. Channel 3 measures the voltage across the 0.01Ω resistor, so every 10mV detected equates to 1A of load current. Enable the function generator output and trigger the oscilloscope on the function generator output. Adjust the time and voltage scales of the oscilloscope until the function generator input is clearly visible.

Figure 26. Example Transient Test Oscilloscope Screenshot: VOUT0 (Blue), PULSE IN (Green), IOUT TST (Yellow)

Begin to slowly increase the amplitude of the pulsed signal, trying to put the transistor in its linear range. This will be indicated by a reaction at V_{OUT} to the load current, meaning that the transistor has turned on and is effectively a resistor draining current from the output voltage. This turn-on gate voltage is typically about 2.3V or 2.4V. Keep increasing the gate voltage until Channel 3 on IOUT TST indicates the output is being loaded with a load step of 50% of the maximum current limit (6A for the DC2155A-A ~ 60mV on scope).

The circuit was tuned based on its frequency analysis. Transient response analysis will show whether or not those adjustments were accurate.

If the phase margin is too low, the system response will be underdamped. This is indicated by output oscillation in response to a load step, as seen in Figure 27a and
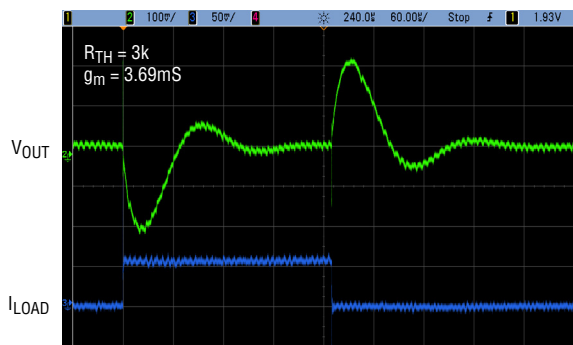
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Figure 27c. If the output voltage response magnitude is large, as in Figure 27a, increase R_{TH} until the response is critically damped as in Figure 27b. If the output voltage response magnitude is small as in Figure 27c, decrease R_{TH} until the oscillation disappears.

If the output voltage is very slow to settle, the system is overdamped. Increase R_{TH} until this problem disappears.

For slightly faster settling time and smaller magnitude response, increase g_m. It has a smaller effect on the transient response and works well for fine tuning. The third image in Figure 28 has the best transient response, however this may be because phase margin has been sacrificed. Be conservative; a good, stable response assures proper operation given component manufacturing variation and drift over the life of the product.
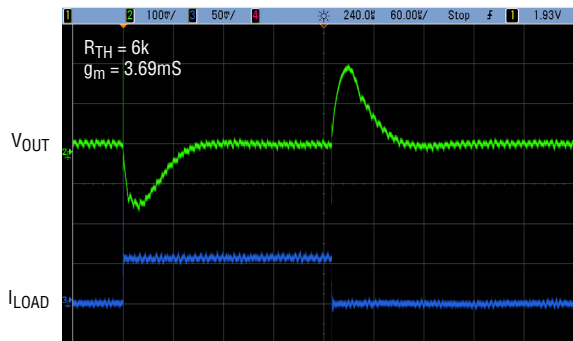
After the transient response has been optimized, another frequency analysis should be conducted to make sure that the phase margin is still within the acceptable range. If not, adjust as instructed in the Phase/Gain Margin section until phase margin is acceptable.
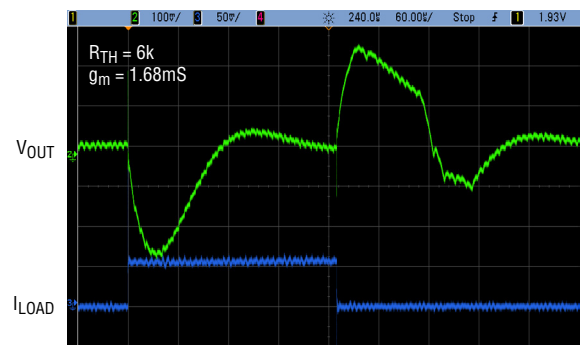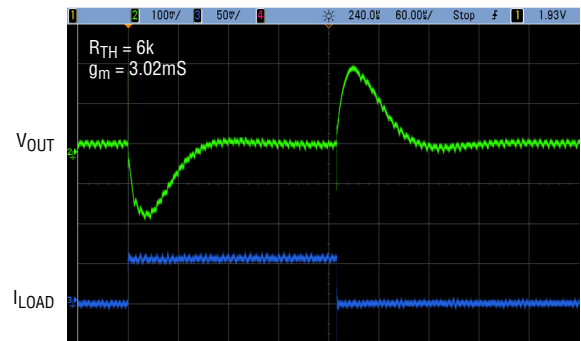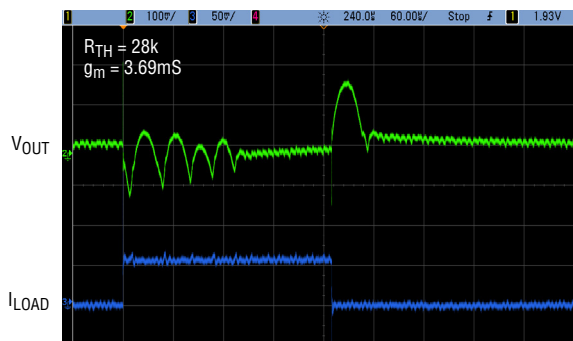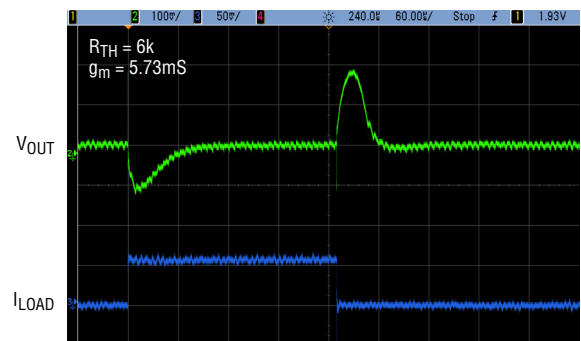

Figure 27. Load Transient Response as R_{TH} Is Varied. 3k and 28k Both Underdamped, Exhibit Oscillation; 6k Is Ideal
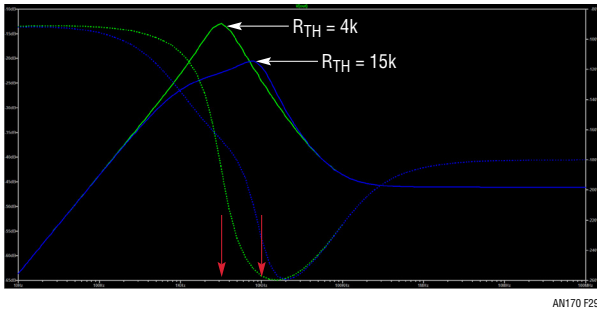

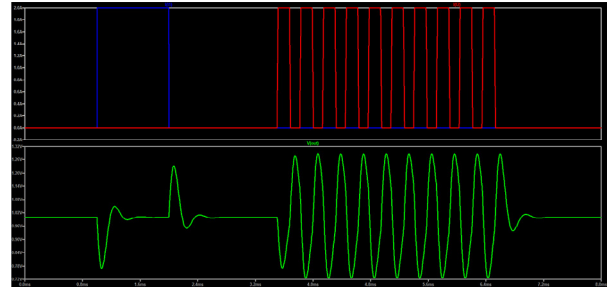Figure 28. Load Transient Response as g_m Is Increased

OUTPUT IMPEDANCE

Optimum impedance is consistently low at all frequencies of interest. If the output impedance peaks at any frequency, then a load frequency at that resonance point could cause significant and unexpected output voltage oscillations. Oftentimes an engineer will prioritize fast transient response over flat impedance, increasing gain and reducing phase margin, thinking that if the response is fast then the system will behave well under transient conditions. In this sense, transient analysis is misleading: it only gives information about the system response to fast changes in load current with lots of time to settle. In real applications, load current can change rapidly and inconsistently, so there is less time to settle and all frequencies of input are possible, not just the ones that were present in transient testing.
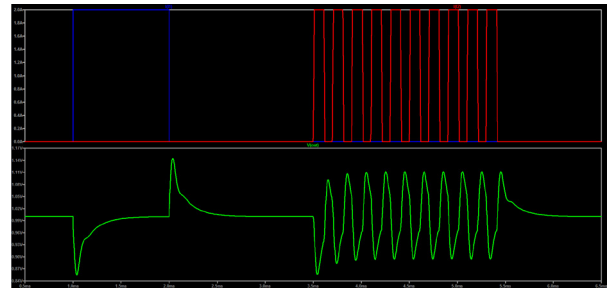
Figure 29 shows the impact of high output impedance at the frequency of the load transient. The circuit responds well to a typical transient test, but when the load is applied at a 50% duty cycle at its resonant frequency, the output oscillates. For this reason, it's worthwhile to make phase margin more conservative and sacrifice some transient response time in order to improve the output impedance characteristics.

R_{TH} = 4k
f_{LOAD} = 7.98kHz

R_{TH} = 15k
f_{LOAD} = 7.98kHz

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Figure 30. Buck Converter Model, Load Step Frequency at Maximum Impedance

The PSMC's output impedance is the impedance from its output voltage to ground. The easiest way to measure this on the LTC3886 demo board is to inject and probe across one of the ceramic output capacitors. C10 for Channel 0 and C24 for Channel 1 are good choices.

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Figure 31. Coax Connection Diagram

To make this measurement, two coaxial cables need to be soldered across one of the output capacitors. Inside the rubber insulator of the leads are two wires, one input and one ground. Cutting the leads as short as possible, strip the insulation and solder the two inputs to the top of the capacitor (at V_{OUT}) and solder the two grounds to the other side of the capacitor. The wires on the cables should be of

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Figure 29. Impedance Magnitude and Phase Plots for Simple Buck Converter Model with R_{TH} Set at 4k (Green) and 15k (Blue). Frequency of Peaks Marked by Red Arrows
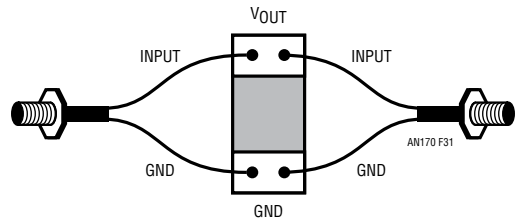
equal length to cancel out any parasitic inductances. Make sure the ground and input cables are not shorted together. Because the outer edge of the coaxial cables is at ground, it is a good idea to tape them to prevent grounding any leads on the demo board. As shown in Figure 32, it is also wise to glue the wires to the board near the solder joint; otherwise repeated movement and twisting may fray or break the connection.
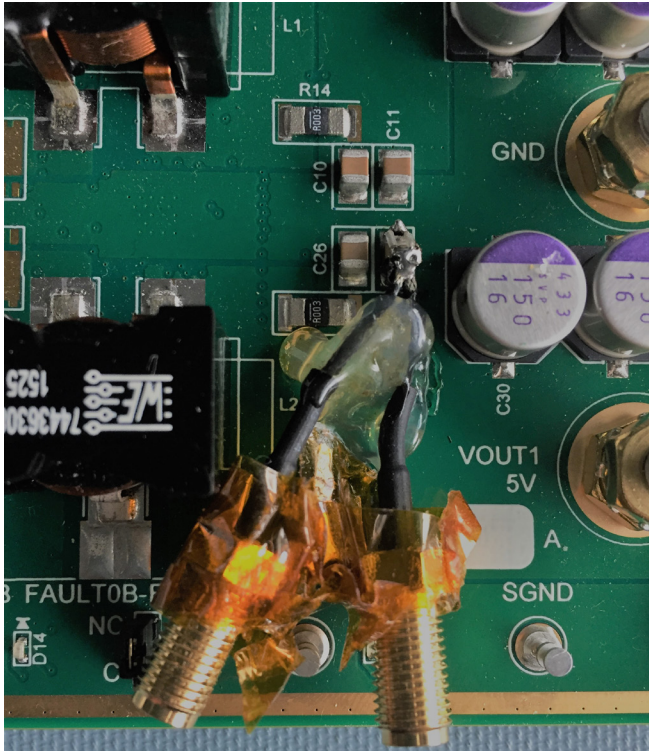
Figure 32. Coax Cables for Impedance Measurement

To measure impedance with the Bode 100 and PICOTEST common mode transformer, begin by powering the Bode 100 and opening the Bode Analyzer Suite. Connect the Input of a PICOTEST common mode transformer to the Output channel of the Bode 100, and put coax cables on both the Output of the PICOTEST common mode transformer and CH2 of the Bode 100. These will be connected to the cables across the capacitor on the demo board once the machine is calibrated. Under the tab "Impedance Analysis", start a "Shunt-Thru" measurement. A full-range calibration is sufficient for this test.

A "Thru Calibration" is the easiest to perform. Connect the Output of the common mode transformer to CH2 with a barrel connector. Run the calibration by pressing the "Start" button under the "Shunt-Thru" header. The box next to the button will turn green and display "Performed" once the calibration is complete.
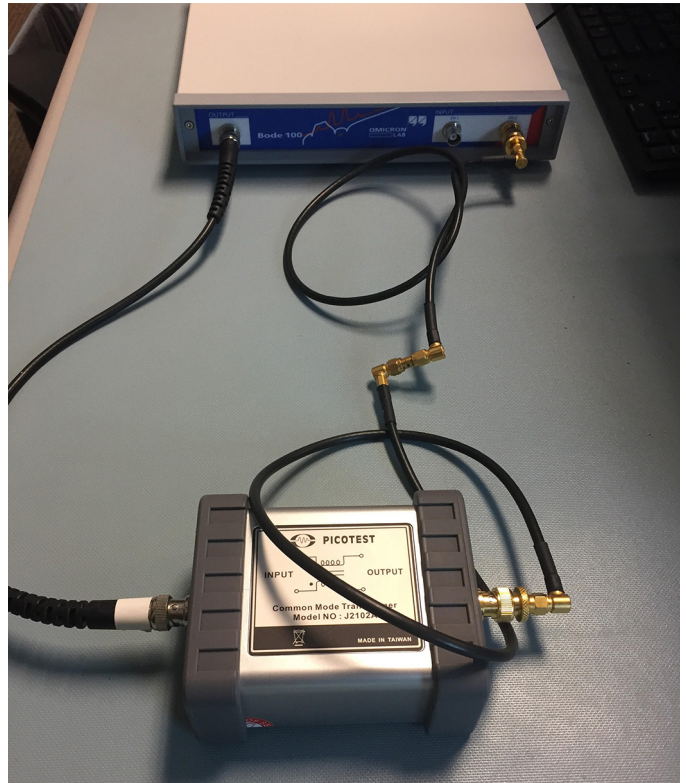
Figure 33. Shunt-Thru Calibration Set-Up

Remove the connector and check that the calibration was successful by measuring the impedance across a small and accurate resistor (1Ω or less). The impedance should be fairly constant at the impedance of the resistor.

If using a Bode 100, make sure that the output voltage is less than 7V to prevent damage. When ready to measure, connect the common mode transformer Output to one of the board's coax cables and the CH2 cable to the other.
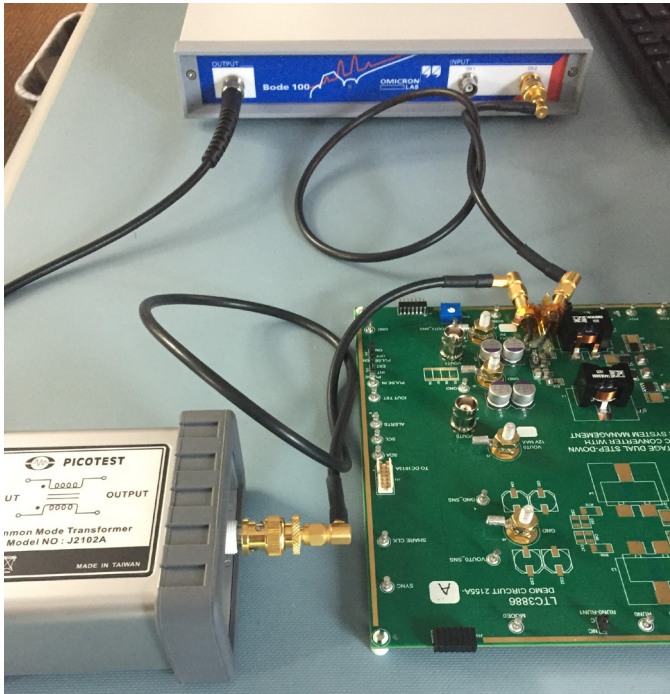
Figure 34. Full Impedance Measurement Set-Up

While the board is powered off, run a test and save the measurement. This curve is the open-loop impedance and is a good reference point for closed-loop impedance testing.

Like closed-loop gain, closed-loop output impedance is a function of its open-loop equivalent.

$$Z_{OCL} = \frac{Z_0}{1 + T(s)}$$

where Z_0 is the open loop output impedance and T(s) is the open-loop gain. If the loop has low phase margin, then at the unity gain frequency T(s) will approach –1 and cause the closed-loop impedance to peak, making it even larger than the open-loop impedance.

The open-loop output impedance Z_0 is a function of the output capacitance, its ESR, and PCB resistance and inductance, combining to form a V-shaped impedance plot as seen in Figure 35. At low frequencies, the open-loop impedance looks like an ideal capacitor and is large. Thus, it is desirable to have high loop gain in this region to reduce impedance. Ideally, the open-loop gain would be just high enough that the closed-loop impedance was low and flat until the open-loop impedance was dominated by the output cap ESR, in which case the loop gain could be

attenuated and the closed-loop impedance would track the open-loop impedance. Unfortunately, phase margin issues and other limitations usually don't allow this ideal scenario.

If the closed-loop impedance peaks and exceeds the open-loop impedance as in the top image of Figure 35, the phase margin is too low. The red arrows in Figure 35 show where low phase margin has resulted in impedance peaking at the unity gain frequency. Increase phase margin using the two-step approach such that the closed-loop impedance never exceeds the open-loop impedance.

If the closed-loop impedance begins to track the open-loop impedance at a low frequency, as exhibited in the lower image of Figure 35, when g_m is small, increase bandwidth by increasing g_m. Be careful that phase margin isn't sacrificed at the crossover frequency.

Like most cases, use g_m for finer adjustments. Adjust g_m slowly to make minor improvements to the impedance and to lower peaking.
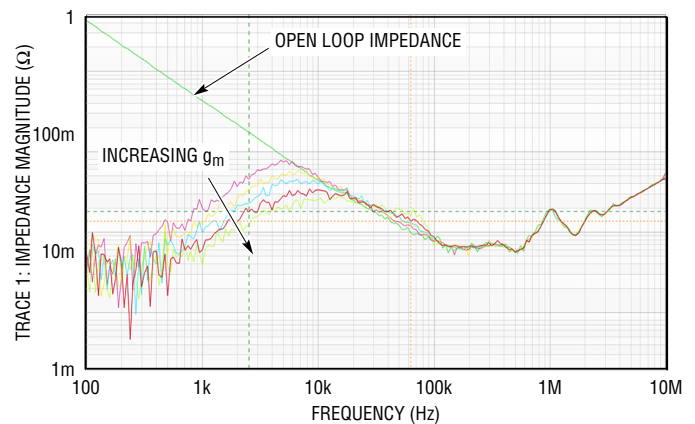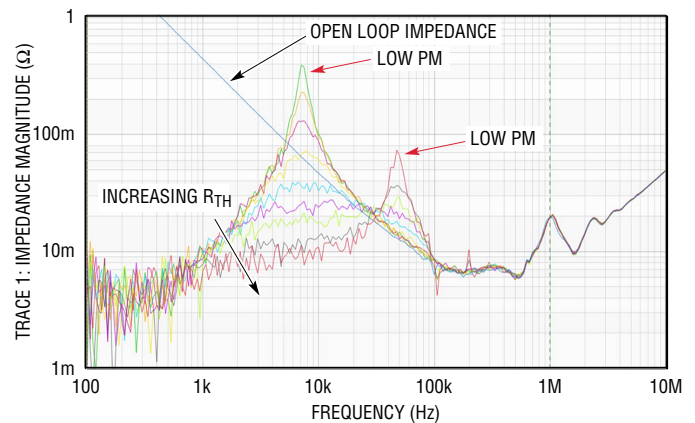
Figure 35. Closed Loop Output Impedance in Range 100Hz to 10MHz as g_m (1.68, 2.35, 3.02, 4.36, 5.73) and R_{TH} (1, 2, 4, 8, 13, 20, 32, 46) Are Varied

As always, go back and check that phase margin is sufficient in a frequency analysis and that the transient response is acceptable. If the impedance plot looks good and the transient response and phase margin are acceptable (but perhaps not ideal), that's okay—low and flat impedance is important.

JITTER

In a stable circuit, jitter is caused by noise coupled into the current sense signal by the power stage. A properly designed compensation and voltage loop have little impact on jitter because C_{THP} filters out high frequency noise. Increasing the value of R_{SENSE}, the sense resistor in series with the inductor, reduces jitter by increasing the magnitude of the current signal, increasing the signal to noise ratio.

Jitter is most accurately measured by probing the switching node indicated in Figure 36.

Figure 36. Probe Switching Node for Best Jitter Measurement

FIRMWARE

For the coding-inclined, the compensation can also be tuned using the Linduino library. While LTpowerPlay supports a broad assortment of PMBus commands, it may be desirable to automate the optimization procedure with a tuning sketch. This section introduces the LTC3886's PMBus Command table (which can be found in the LTC3886 data sheet) and explains the basics of serial PMBus communication with the demo board. A simple, interactive tuning sketch was written as an example. It prompts the user for either an R_{TH} or g_m value, updates the parameter, and then outputs the new configuration. It displays some of the basics of reading and writing to the LTC3886 with PMBus, and can be found in Figures 37–41. The full sketch can be found under the name "Adjustable_Comp" in the Linduino Sketchbook by following the path: File → Sketchbook → Part Number → 3000 → 3800 → 3886 → Adjustable_Comp.

All slave devices must have a unique 7-bit address to allow access by the PMBus master. The LTC3886 address can be set either by an EEPROM register or resistor dividers on pins ASEL0 and ASEL1. For instructions on addressing the LTC3886, consult page 56 in the LTC3886 data sheet or AN152, "Power System Management Addressing".[10] Once an address is selected, define the address in the sketch for clarity as shown in Line 14. In the sketch below, the LTC3886 address is the default value of 0x4F.

The complete command table for the LTC3886 begins on page 35 of its data sheet. Command MFR_PWM_COMP, code 0xD3, is used for adjusting the compensation.

Write commands are structured as such: a start bit, the address byte of the LTC3886, the data and an acknowledge bit. For configuring the compensation, two bytes of data are sent. The first byte of data is the command code MFR_PWM_COMP, which is followed by the configuration code. The three most significant digits in the configuration code byte correspond to the eight possible values of g_m. The five least significant digits correspond to the 32 possible R_{TH} values. For example, the configuration code 0x00 corresponds to a g_m of 1.0mS and R_{TH} of 0kΩ, the smallest possible values of g_m and R_{TH}. Likewise, 0xFF corresponds to a g_m of 5.73mS and R_{TH} of 62kΩ, the

Note 10. http://cds.linear.com/docs/en/application-note/an152f.pdf

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Table 4.

BIT	MEANING
BIT [7:5]	**EA_{gm} (mS)**
000b	1.00
001b	1.68
010b	2.35
011b	3.02
100b	3.69
101b	4.36
110b	5.04
111b	5.73
BIT [4:0]	**R_{ITH} (kΩ)**
00000b	0
00001b	0.25
00010b	0.5
00011b	0.75
00100b	1
00101b	1.25
00110b	1.5
00111b	1.75
01000b	2
01001b	2.5
01010b	3
01011b	3.5
01100b	4
01101b	4.5
01110b	5
01111b	5.5
10000b	6
10001b	7
10010b	8
10011b	9
10100b	11
10101b	13
10110b	15
10111b	17
11000b	20
11001b	24
11010b	28
11011b	32
11100b	38
11101b	46
11110b	54
11111b	62

maximum values. The table of values are displayed in Table 4. Lines 54 and 64 show examples of writing using the MFR_PWM_COMP code.

The `writeByte` command takes the address, followed by the command code, followed by the data as its parameters. Because the user typically wants to change R_{TH} or g_m one at a time, updating the `comp_config` requires some global variables and simple binary operations.

The global variables `ith` and `gm` store the 8-bit values of the current R_{TH} and g_m, where the bits not used in designating the component's value are set to zero. For example, the value stored in `gm` only contains relevant information in its three most significant bits, the five least significant bits are set to zero. Likewise, `ith` keeps its three most significant bits set at zero. When one of the variables is updated, bitwise OR `ith` and `gm` to update the `global comp_config` variable. See Lines 53 and 63.

Oftentimes it's helpful to read the compensation configuration from the MFR_PWM_COMP register to initialize `gm` and `ith`. In these cases, the master sends a read command of the MFR_PWM_COMP command to the LTC3886 at the chip's PMBus address. The LTC3886 then sends back the command code data. The R_{TH} and g_m values can be extracted simply by performing a bitwise AND with a hex value that is 1 at the digits of interest and zero elsewhere. This is shown in Lines 84–87.

SUMMARY

Compensation tuning gives the user control over the PSMC transfer function. The digital compensation adjustment of the LTC3886 allows the user to optimize loop performance easily without changing external components. Once the design is completed, compensation adjustments should be made to optimize the loop. This will ensure stability, a flat impedance and fast transient response. More information about ADI PSM products is available at the following link:

http://www.linear.com/solutions/Digital_Power_System_Mnagement

```
01: #include <Arduino.h>

02: #include <stdint.h>

03: #include "UserInterface.h"

04: #include "Linduino.h"

05: #include <LT_12CBus.h>

06: #include <LT_PMBus.h>

07: #include <LT_PMBusMath.h>

08: #include <LT_SMBus.h>

09: #include <LT_SMBusBase.h>

10: #include <LT_SMBusGroup.h>

11: #include <LT_SMBusNoPec.h>

12: #include <LT_SMBusPec.h>

13: #include <LT_Wire.h>

14: #define LTC3886_I2C_ADDRESS 0x4F

15: #define PWM_COMP_CONFIG 0xD3

16: #define PAGE 0x00

17: #define CH_0 0x00

18: #define CH_1 0x01
```

Figure 37. Include Statements

```
...
19: //Global variables

20: static uint8_t ltc3886_i2c_address;

21: static LT_SMBusNoPec *smbus = new LT_SMBusNoPec();

22: static uint8_t channel;

23: static uint8_t ith;

24: static uint8_t gm;

25: static uint8_t comp_config;

26: static float ith_dec;

27: static float gm_dec;
```

Figure 38. Global Variables

```
...
28: // Initialize Linduino
29: void setup()
30: {
31:   Serial.begin(115200);
32:   print_title();
33:   ltc3886_i2c_address = LTC3886_I2C_ADDRESS
34:   channel = CH_0;
35:   print_comp_config90;
36:   print_prompt();
37: }
```

Figure 39. Set-Up Block

```
38: //! Repeats Linduino loop
39: void loop()
40: {
41:   uint8_t user_select;
42:   float user_value;
43:   if (Serial.available())
44:   {
45:     user_select = read_int();
46:     switch (user_select)
47:     {
48:       case 1:
49:         Serial.print(F"\nEnter desired gm (1-5.73), this will be rounded:\n"));
50:         user_value = read_float();
51:         gm_dec = gm_round(user_value);
52:         gm = gm_decimal2hex(gm_dec);

53:         comp_config = gm | ith;
54:         smbus->writeByte(ltc3886_i2c_address, PWM_COMP_CONFIG, comp_config);
                                         ...
```

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...

```
55:        print_comp_config();
56:        print_prompt();
57:        break;
58:    case 2:
59:        Serial.print(F("\nEnter desired ith (0-62), this will be rounded:\n"));
60:        user_value = read_float();

61:        ith_dec = ith_round(user_value);
62:        ith = ith_decimal2hex(ith_dec);

63:        comp_config = gm | ith;
64:        smbus->writeByte(ltc3886_i2c_address, PWM_COMP_CONFIG, comp_config);

65:        print_comp_config();
66:        print_prompt();
67:        break;
68:    case 3:
69:        if (channel == 0) {
70:          smbus->writeByte(ltc3886_i2c_address, PAGE, CH_1);
71:          channel = CH_1;
72:        }
73:        else {
74:          smbus->writeByte(ltc3886_i2c_address, PAGE, CH_0);
75:          channel = CH_0;
76:        }

77:        Serial.println();
78:        print_comp_config();
79:        print_prompt();
80:        break;
81:    }
82:  }
83: }
```

Figure 40. Loop Block

```
                                      ...
84: void print_comp_config() {
85:    comp_config = smbus->readByte(ltc3886_i2c_address, PWM_COMP_CONFIG);


86:    ith = 0x1F & comp_config;
87:    gm = 0xE0 & comp_config;
88:    ith_dec = ith_hex2decimal(ith);
89:    gm_dec = gm_hex2decimal(gm);
90:                                  [...Print Statements...]
91: }
```

Figure 41. comp_config() Function

APPENDIX

Explanation of Closed-Loop Gain Peaking[11]

The controller's closed-loop transfer function is a function of $K_{REF}(s)$ and $T(s)$, the feedback divider and controller open-loop transfer functions respectively.

$$G(s) = \frac{1}{K_{REF}(s)} \bullet \frac{T(s)}{T(s)+1}$$

Because $K_{REF}(s)$ is typically a resistor divider, it doesn't vary with frequency. Therefore, the key to understanding the cause of the near-f_C peaking lies in understanding the term
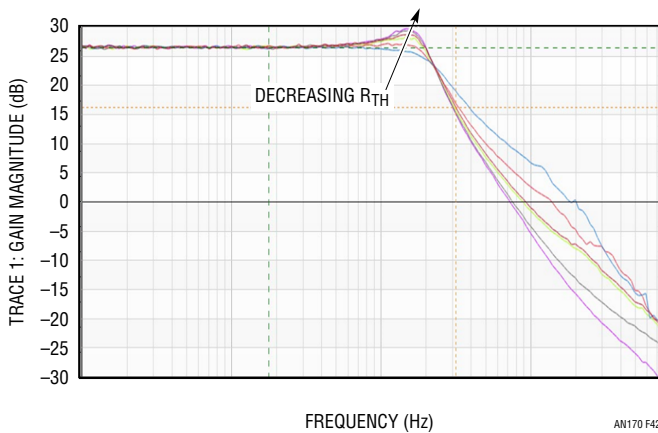
$$\frac{T(s)}{T(s)+1}$$

Figure 42.

Assuming the output filter capacitor is large and therefore has a pole at very low frequency, the controller's transfer function in the vicinity of f_C can be approximated by that of the compensation network, where the low frequency pole is treated as an origin pole.

$$T(s) \equiv A(s) \approx R_0 \bullet g_m \bullet \frac{1 + \dfrac{s}{s_Z}}{\dfrac{s}{s_{P0}} \bullet \left(1 + \dfrac{s}{s_{P1}}\right)}$$

Note 11. This derivation is based on a similar one in section 9.4.2 of *Fundamentals of Power Electronics Ed.2* by Robert W. Erickson and Dragan Maksimovic. Instead of approximating the transfer as a two-pole system, the compensation transfer is used.

where A(s) is the open-loop compensation transfer, and

$$s_{P0} = \frac{1}{R_0 \bullet C_{TH}} \qquad s_Z = \frac{1}{R_{TH} \bullet C_{TH}} \qquad s_{P1} \cong \frac{1}{R_{TH} \bullet C_{THP}}$$

It helps to rearrange $T(s)/(T(s) + 1)$ as follows. The constants out front can be neglected because they are not affected by R_{TH} and therefore don't assist in explaining why changing R_{TH} affects peaking.

$$\frac{T(s)}{T(s)+1} = \frac{1}{1 + \dfrac{1}{T(s)}} = \frac{1 + \dfrac{s}{s_Z}}{1 + s\left(\dfrac{s_{P0} + s_Z}{s_{P0}s_Z}\right) + \dfrac{s^2}{s_{P0}s_{P1}}}$$

Putting this into standard form gives

$$\frac{1 + \dfrac{s}{s_Z}}{1 + \dfrac{s}{Qs_C} + \left(\dfrac{s}{s_C}\right)^2}$$

where,

$$s_C = \sqrt{s_{P0}s_{P1}} \qquad Q = \frac{s_{P0}s_Z}{s_C(s_{P0} + s_Z)}$$

This Q-factor determines the height of the peak at s_C. A larger Q causes a larger peak, an undesirable trait. In this case, Q is mostly a function of the frequencies of the zero and dominant pole. Changing R_{TH} has no effect on the dominant pole frequency, but it does change the zero frequency, which is why R_{TH} influences the size of the peak in G(s).

Increasing R_{TH} lowers s_Z, therefore reducing Q, which reduces the height of the peak. However, R_{TH} also affects s_C because it is a function of s_{P1}. There are two reasons the change in s_{P1} is negligible.

In most cases, $C_{TH} \gg C_{THP}$, so given some finite ΔR_{TH} then

$$\Delta s_Z > \Delta s_{P1}$$

which would mean that the change in the zero has more influence than the change in the high frequency pole. In addition, the square root further reduces the influence of s_{P1}.

Derivation of A(s)

The open-loop transfer function of the compensation network is the gain of the OTA times the impedance of the network.

$$V_{ITH} = (V_\Delta \cdot g_m) \cdot Z_{ITH}$$

$$A(s) = g_m \cdot Z_{ITH}$$

where V_{ITH} and V_Δ are both small AC signals, and $V_\Delta = V_{FB} - V_{REF}$, the difference between the feedback and the reference voltages at the OTA inputs.

This derivation takes advantage of two assumptions: that the OTA output impedance R_0 is much greater than R_{TH}, and that C_{TH} is much greater than the high frequency capacitor C_{THP}. These assumptions simplify the derivation considerably and make the resulting transfer function easier to understand.

If the compensation is just one capacitor C_{TH}, then Z_{ITH} is easy to derive and results in an integrator with infinite DC gain.

$$A(s) = g_m \cdot \frac{1}{C_{TH} \cdot s}$$

Accounting for some finite output impedance R_0, this can add in parallel to C_{TH}.

$$Z_{ITH} = \left(\frac{1}{R_0} + sC_{TH} \right)^{-1}$$

$$A(s) = \frac{g_m}{\dfrac{1}{R_0} + sC_{TH}} = \frac{g_m}{\dfrac{1}{R_0} + (sC_{TH} + 1)}$$

$$= R_0 \cdot g_m \cdot \frac{1}{\left(1 + \dfrac{s}{s_{P0}} \right)}$$

where s_{p0} is as defined in previous sections.

To boost phase, R_{TH} is added in series with C_{TH}. The new impedance leads to a new transfer function.

$$Z_{ITH} = \left(\frac{1}{R_0} + \frac{1}{\dfrac{1}{sC_{TH}} + R_{TH}} \right)^{-1}$$

Use algebra to change around denominators and combine terms:

$$A(s) = \frac{g_m}{\left(\dfrac{1}{R_0} + \dfrac{sC_{TH}}{R_{TH}C_{TH}s} \right)} = \frac{g_m}{\dfrac{sC_{TH}R_0 + R_{TH}C_{TH}s + 1}{R_0 \cdot (1 + R_{TH}C_{TH}s)}}$$

$$= R_0 \cdot g_m \cdot \frac{(1 + R_{TH}C_{TH}s)}{1 + sC_{TH}(R_{TH} + R_0)}$$

Since $R_0 \gg R_{TH}$, the R_{TH} can be ignored, leaving:

$$A(s) = R_0 \cdot g_m \cdot \frac{\left(1 + \dfrac{s}{s_Z} \right)}{\left(1 + \dfrac{s}{s_{P0}} \right)}$$

where s_{P0} and s_Z are as defined in previous sections.

Finally, C_{THP} is added to filter switching noise.

$$Z_{ITH} = \left(\frac{1}{R_0} + \frac{1}{\dfrac{1}{sC_{TH}} + R_{TH}} + sC_{THP} \right)^{-1}$$

To avoid the messy algebra that comes with solving for the full impedance, Z_{ITH} is approximated in the high frequency range where $R_{TH} \gg 1/sC_{TH}$). At high frequency C_{TH} is effectively a short, so the compensation network is modeled as a parallel network of two resistors—R_0 and R_{TH}—and C_{THP}. Because $R_0 \gg R_{TH}$, the parallel impedance of the resistors is approximated by that of R_{TH}.

$$R_0 \parallel R_{TH} = \frac{R_0 R_{TH}}{R_0 + R_{TH}} \cong R_{TH}$$

This means that at high frequency, the network is effectively R_{TH} in parallel with C_{THP}.

$$Z_{ITH} = \left(\frac{1}{R_{TH}} + sC_{THP} \right)^{-1}$$

This network has one pole at s_{P1}. By including this high frequency pole in the transfer function derived before C_{THP} was factored in yields the compensation transfer.

$$A(s) = R_0 \bullet g_m \bullet \frac{\left(1 + \dfrac{s}{s_Z}\right)}{\left(1 + \dfrac{s}{s_{P0}}\right) + \left(1 + \dfrac{s}{s_{P1}}\right)}$$

Transfer of $K_{REF}(s)$

In most cases of interest, $K_{REF}(s)$ is simply a resistor divider and therefore has a constant gain, unaffected by frequency. $K_{REF}(s)$ is dependent on the voltage range (low or high).

$$K_{REF}(s) = \frac{R_{LOWER}}{R_{UPPER} + R_{LOWER}}$$

Some designs of $K_{REF}(s)$ include capacitors in parallel with one or both of the resistors in the divider. For this transfer function, consult AN149.[12]

Transfer of $G_{CV}(s)$

Because the current loop regulates the inductor current, the inductor can be considered a current source dependent on V_{ITH}. This model is typically accurate up to about 1/50th the switching frequency, which is sufficient for understanding how the compensation network can be adjusted to optimize performance. At higher frequencies the phase plot is not accurate. This is shown in Figure 44.
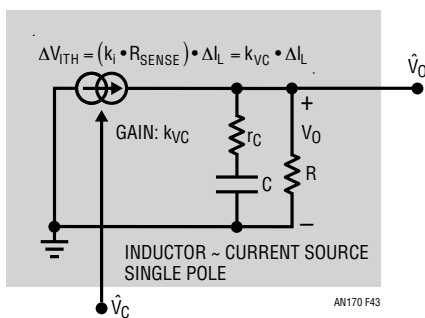
Figure 43. First Order Model of Current Mode Buck Converter PWM and Output Filter
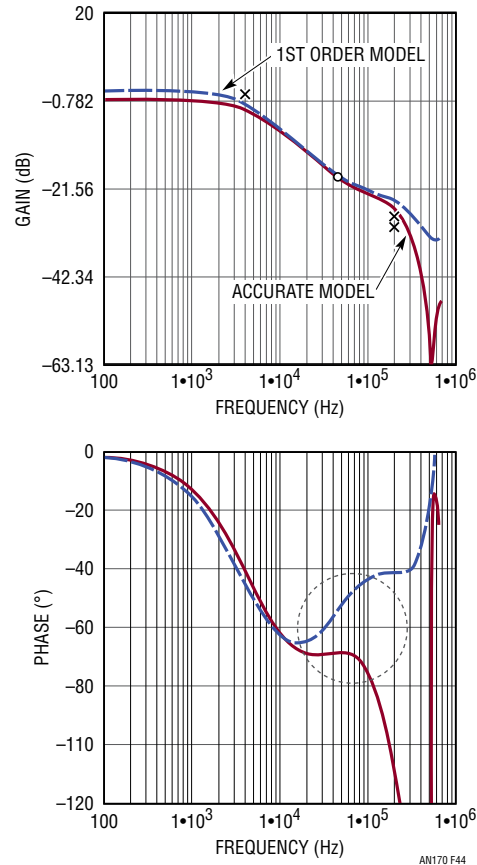
Figure 44. Gain and Phase Accuracy of First Order Power Stage Model

The power stage is modeled as a current source producing current I_L in series with an impedance network $Z_{PS}(s)$ consisting of a capacitor, C_{OUT}, and its series resistance, r_{ESR}, in parallel with the load resistor, R.

$$V_{OUT} = I_L \bullet Z_{PS}(s)$$

The current source output is linearly proportional to V_{ITH}.

$$\frac{\Delta V_{ITH}}{k_{vc}} = \Delta I_L$$

where ΔV_{ITH} is the change in ITH voltage and k_{vc} is the current source gain, dependent on the current range, sense resistor and slope compensation.

Note 12. http://cds.linear.com/docs/en/application-note/an149fa.pdf

By using the equation for parallel impedance and doing some simple algebra, one obtains the equivalent impedance $Z_{PS}(s)$.

$$Z_{PS}(s) = R \bullet \frac{1 + \dfrac{s}{s_{ESR}}}{1 + \dfrac{s}{s_R}}$$

$$s_{ESR} = \frac{1}{r_{ESR}C_{OUT}}$$

$$s_R = \frac{1}{(R + r_{ESR})C_{OUT}} \cong \frac{1}{RC_{OUT}}$$

Thus, the power stage transfer function $G_{CV}(s)$ is shown to be

$$G_{CV}(s) = \frac{R}{k_{cv}} \bullet \frac{1 + \dfrac{s}{s_{rc}}}{1 + \dfrac{s}{s_R}}$$

Because R is likely much greater than r_{ESR}, the zero frequency is much higher than the pole frequency. This is why a 20dB per decade slope is observed when measuring the closed loop compensation gain. The transition frequency is below the frequency at which the zero becomes relevant.

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