LTC4015

August 2017

LTC4015 ERRATA

The errata below describes conditions that may cause an LTC®4015 to operate differently than expected or described in the data sheet.

ERRATA SUMMARY

ERRATA NUMBER	DESCRIPTION	PAGE
1	Device Resets, Losing Settings and Data	1

ERRATA #1: DEVICE MAY RESET

The device may reset itself resulting in loss of data and configuration settings. This can only occur in one specific use case detailed below. All other operating states are immune to this issue.

Conditions:

All of the following conditions must be present at the same time to expose this problem:

1. Battery Only Operation: $V_{IN} < V_{BAT}$;

   AND

2. Telemetry is not on. (Default setting in battery only – non-charging, force_meas_sys_on = 0, sub-address 0x14, bit 4);

   AND

3. I^2C communications with idle time longer than 20ms;

   AND

4. I^2C port programmed (e.g., charger settings or alerts have been configured or coulomb counter has been enabled). If the I^2C port is not programmed, this error has no impact.

Even with the above conditions, the issue only presents infrequently. All other use cases are immune to the issue.

Impact:

The device can reset itself, returning all registers to factory defaults. If this type of self-reset occurs, it will be indicated by the single bit flag at register 0x39, bit 12.

Root Cause:

An internal timing conflict exposed after watchdog timeout.

Workarounds:

Two workarounds are possible. These workarounds will wake the logic system before the watchdog can time out.

1. Use continuous I^2C polling and ensure a polling rate greater than 50Hz.
2. Force the telemetry system on using the force_meas_sys_on bit at register 0x14, bit 4. This will result in increased battery-only mode quiescent current by 2mA – 3mA.

DEVICE FIX PLANNED:

The internal timing conflict will be corrected. A PCN will be issued as soon as revised devices are available to sample, which is expected within Q1, CY 2017.

UPDATE:

The internal timing conflict has been corrected. Revised silicon available starting Q2 CY 2017, with top mark date codes 1716 and higher.

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	08/17	Added Date Code cutoff	1

LT 0817 REV B • PRINTED IN USA
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