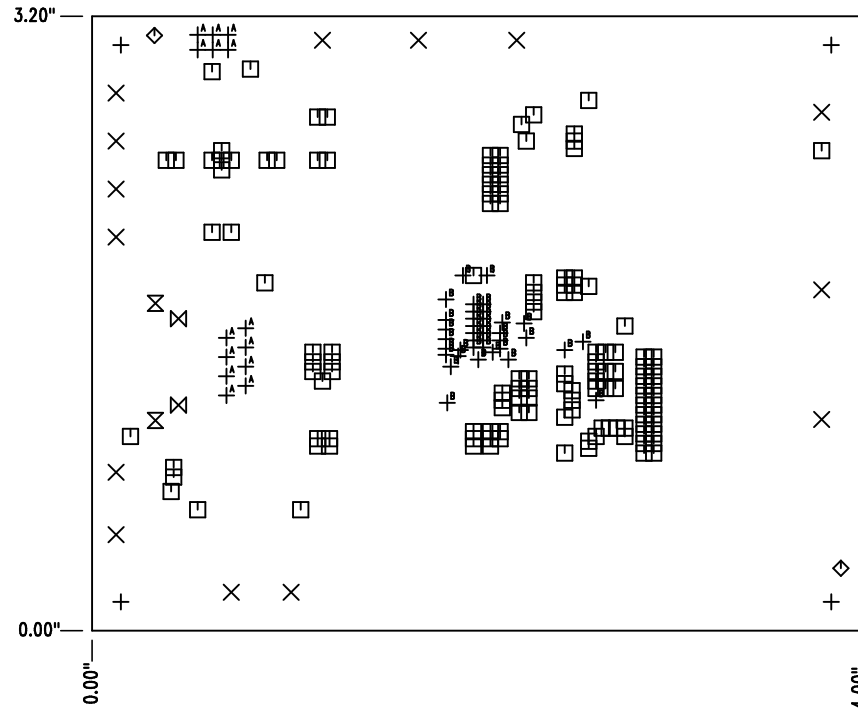
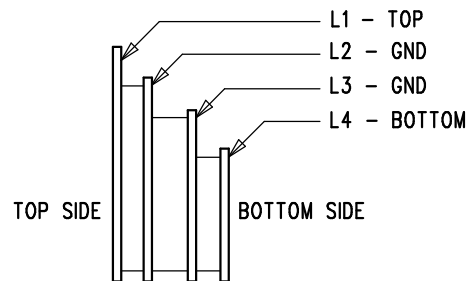


SHOWN FROM COMPONENT SIDE

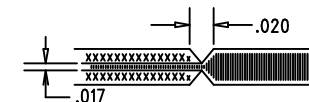




REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
1	2	PRODUCTION REBUILD W CHANGES	RYAN H.	02-18-10

SIZE	QTY	SYM	PLATED	TOL
0.01	38		YES	+/-0.003
0.015	135		YES	+/-0.003
0.035	14		YES	+/-0.003
0.06	2		YES	+/-0.003
0.07	2		NO	+/-0.003
0.094	14		YES	+/-0.003
0.125	2		NO	+/-0.003
0.187	4		NO	+/-0.003

- FAB PER IPC-A-600.
- MATERIAL: -EPOXY FIBERGLASS, NEMA GRADE FR-4
-FINISHED THICKNESS TO BE 0.062" +/- .005"
-TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.
-GOLD IMMERSION BOTH SIDES.
(LEAD FREE SOLDER CAN BE USED FOR PROTOTYPE)
-FOR SILKSCREEN: BOTH SIDES USE WHITE NON-CONDUCTIVE INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING FOR PANELIZED PCB:



UNLESS OTHERWISE SPECIFIED		APPROVALS			
DIMENSIONS ARE IN INCHES TOLERANCES: 0.XX" = ±0.01" 0.XXX" = ±0.005" INTERPRET DIM AND TOL PER ASME Y14.5M-1994 THIRD ANGLE PROJECTION		PCB DES.	KT		
		APP ENG.	RYAN H.	TITLE: FABRICATION DRAWING	
				HIGH POWER, HIGH EFFICIENCY POE PD INTERFACE WITH INTEGRATED SWITCHING REGULATOR	
		SIZE	IC NO.	LTC4269IDKD-1	REV
		N/A		DEMO CIRCUIT 1335B	2
SCALE = NONE		FILENAME: DC1335B.PCB			SHT 1 OF 1

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