

LTC4283 –48V, 400W Hot Swap Controller with Energy Monitor and EEPROM

DESCRIPTION

Demonstration circuit 2480A showcases the [LTC®4283](#) high power, negative hot swap controller with energy monitor and EEPROM in a –48V, 8A (400W) application. DC2480A offers reliable low cost hot plug solution for high power systems where input steps are imminent.

Included onboard is isolation for power good control pins, to enable downstream power converters. LEDs indicate the presence of –48V input and output as well as the

state of both supply feeds and power good signaling. High voltage layout rules are followed throughout for best long-term product reliability.

Headers are provided for three I²C interfaces, providing instant access to voltage, current, power, energy, fault log, and board temperature data.

[Design files for this circuit board are available.](#)

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PERFORMANCE SUMMARY Specifications are at T_A = 25°C

Table 1

PARAMETER	MIN	TYP	MAX	UNITS
Input Valid Operating Voltage	–35.3	–48	–74.5	V
Output Power			400	W
Output Capacitor			400	μF
Current Limit (at –48V Input)	12.19	12.5	12.87	A

DEMO MANUAL DC2480A

QUICK START PROCEDURE

Board Layout

The board is divided into several planes, each separated by a 60mil gap for DC standoff up to 100V. In addition to the basic planes (RTN, -48VIN, VEE and -48VOUT), there are small subplanes for the MOSFET sources. Other isolated regions include the areas around the supply monitor inputs, RTN short pin, and the power good opto-isolators.

Power Connections

User can use 4 AWG (19mm²) welding cable for power supply and load connections. Suitable welding cable is

available from Anixter (877-467-9473). Order ToughFlex™ #4 heavy duty welding cable, part number WC4BK.

In order to minimize the power dissipation and board heat up, for power connections to the PCB, large pads are provided with Panduit S4-14R ring terminals. These are designed for use with 4 AWG welding cable. Crimp all ring terminals using a Thomas & Betts WT115 or equivalent compression crimper. Do not solder.

The ring terminals are attached to the board with stainless 1/4-28 mounting hardware. To prevent damage to the PCB, do not exceed a torque of 5ft/lbs (6.8Nm). The

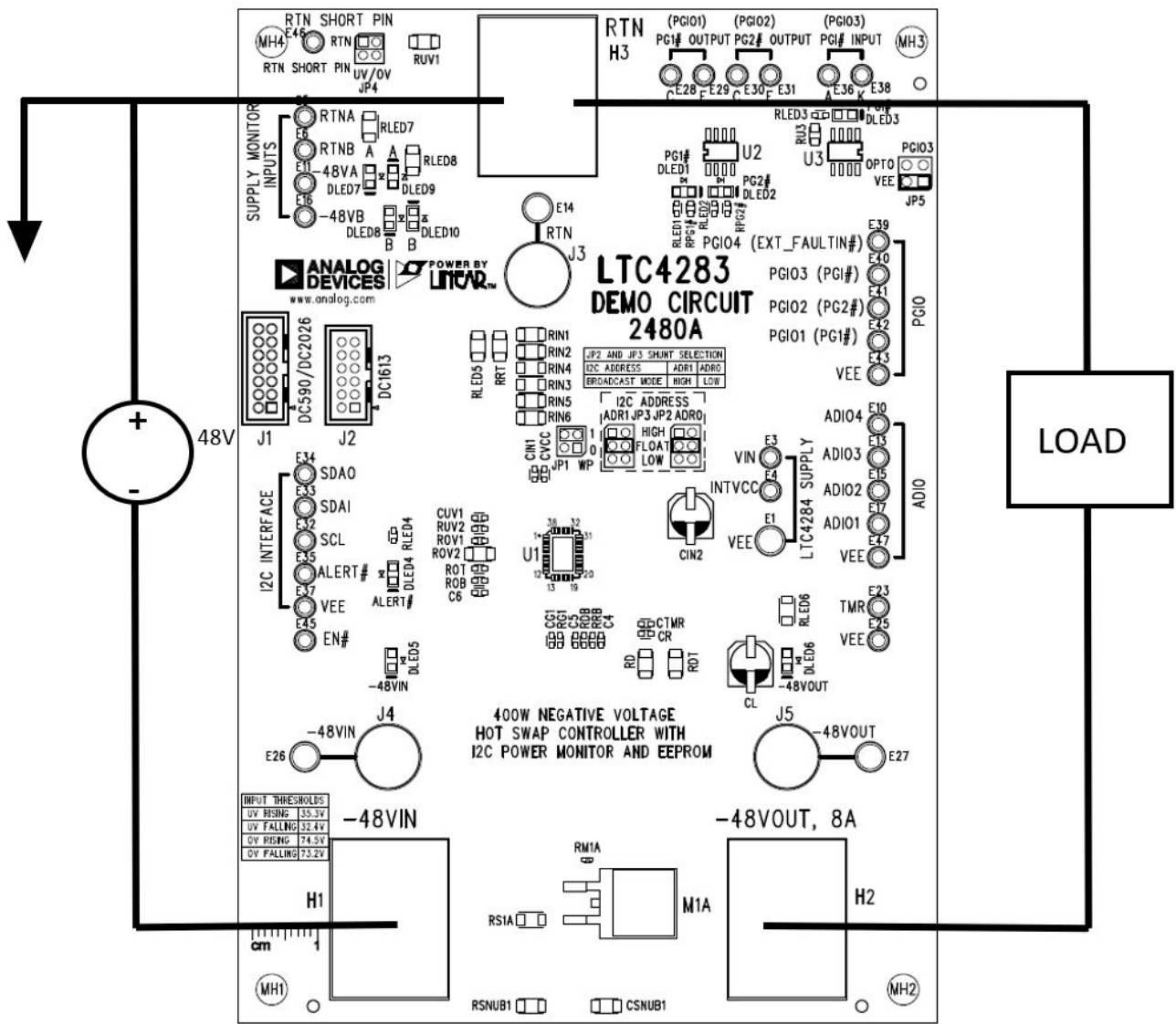


Figure 1. DC2480A Setup

QUICK START PROCEDURE

cap screws require a 3/16" Allen wrench, and the nuts require a 7/16" nut driver. Stainless hardware is subject to galling; lubricate the threads with Lucas Oil Products white lithium grease (product number 10533), or with an equivalent product that meets the NLGI #2 specification.

Power flows through DC2480A from the –48VIN terminal to –48VOUT, through the load, and hence returns to the positive terminal of the power supply. It is not necessary for power to flow through the DC2480A return path; for this reason, there is only one RTN connection on the PCB. Surprisingly, the PCB's return connection can be made with a small test lead to either the load or the power supply.

For minimum loss, the load and power supply returns should be connected together directly, through the shortest possible length of cable. Nevertheless, a high current RTN pad is included to provide a convenient point at which the load and power supply returns can be joined together, in the case where separate cables present themselves.

Power Good Control

DC2480A includes two power good outputs, as well as a power good input, using the PGI01, PGI02 and PGI03 pins of the LTC4283. Initially, 256ms after a successful powerup, Power Good 1 (PG1#) goes low. 256ms later Power Good 2 (PG2#) goes low. The intent of these two outputs is to sequentially enable downstream DC-DC converters, after the MOSFET is fully on. PG1# and PG2# outputs are the photo transistors of U2. These pull low in the "power good" condition and can sink up to 1mA.

Power good input (PGI# INPUT, implemented with the PGI03 pin) must be asserted within 512ms after PG2# goes low, as verification that the secondary supplies have successfully reached regulation. If PGI# INPUT is not asserted in time, the LTC4283 will shut down.

Normally the PGI# INPUT signal is obtained from a supply monitor, or just simply tied to a secondary supply output.

PGI# INPUT (turrets A and K) drives a green indicator LED and the LED in opto isolator U3, each through a 1k Ω resistor, so that PGI# INPUT can be tied directly to a 3.3V or 5V supply (A = +, K = –) to assert a power good condition.

Higher supplies can be monitored with the addition of 500 Ω /V in series with PGI# INPUT's A and K turrets. To avoid the need for PGI# feedback during initial testing, jumper JP7 is provided so that PGI03 can be forced low (PGI03 set to VEE position).

J1, J2 Digital Interface

The LTC4283 features an I²C interface to control the device and to retrieve measurements, status and fault information. Because the LTC4283 uses –48VIN as its "ground" reference, the I²C lines must be isolated in order to communicate with a truly ground-referred control processor. This isolation is not included on DC2480A. Instead, headers are made available for DC590, DC1613 and DC2026 interface boards, all of which feature full galvanic isolation and USB communication with a host computer. A ribbon cable connects J1 or J2 to the interface board; do not use J1 and J2 simultaneously.

An LTpowerPlay® GUI is available at www.analog.com. This GUI operates with DC1613, supplied separately. A 24LC025 EEPROM (U4) located on DC2480A communicates with LTpowerPlay, permitting it to load the corresponding GUI without user input.

Jumpers

JP1: WP. This write protect blocks writes (position 1) to the LTC4283 on-chip EEPROM. 0 enables writes. WP does not block fault logging.

JP3, JP2: I²C Address. These jumpers program the LTC4283's address at the ADR1 and ADR0 pins. Default FLOAT-FLOAT stuffing selects address 2Ah. HIGH-LOW selects broadcast mode (see data sheet for information on broadcast mode).

QUICK START PROCEDURE

JP4: UV/OV. The UV and OV divider strings are joined together and serve as a RTN short pin input. For testing purposes, the short pin function can be bypassed by moving the jumper to the RTN position. To avoid permanent connector damage, high power applications must use a short pin for on/off control during insertion and extraction.

JP5: PGIO3. PGIO3 is configured as a PGI# input (power good input) and is controlled by the PGI# INPUT via opto isolator U3. JP7 bypasses the PGI# function when the jumper is set to the VEE position. Doing so ties PGIO3 low, indicating “power is good” and allowing the LTC4283 to remain on after a successful power-up.

Supply Monitor Inputs

The ADIN1-4 pins are used to measure the individual supply feed terminal voltages relative to the V_{REF} pin (and ultimately, VEE), in a two-supply system. ADIO3 is configured to measure the chassis voltage, also relative to V_{REF} . Thus in a redundant feed system, a total of five connections between DC2480A and RTNA, RTNB, –48VA, –48VB, and CHASSIS are necessary to use this feature. Precision 101:1 dividers connect to these potentials, to measure their respective voltages. The bottom of the

dividers is connected to V_{REF} , allowing measurement of up to $\pm 100V$ relative to VEE. Feed voltage is inferred by subtracting associated –48V and RTN readings. Absolute terminal voltages, relative to chassis, are obtained by subtracting the chassis reading (ADIO3) from the individual terminal readings (ADIN1-4). LTpowerPlay takes care of calculations and shows the differential voltage of the two feeds, and the individual feed terminal voltages relative to ground. The operation of the feed monitor circuit is explained in the data sheet and illustrated in Figure 23, Feed Voltage and Open Fuse Monitoring. If unused, these connections may be simply left open circuit.

Board Temperature

An NTC thermistor (RTHA) and linearizing circuit is connected to the LTC4283’s ADIO4 pin, to measure board temperature. The ADIO4 pin is configured as an ADC input. The LTpowerPlay GUI calculates temperature using the adc measurement of ADIO4’s voltage.

Altered Register Values

Table 2 shows the changes that have been made to the default register values as they listed in the data sheet.

Table 2

PARAMETER NAME	REGISTER VALUE	
ILIM	1010	25mV
FB	11	10%
FTBD_DL	01	512ms
Cooling Delay	100	8.19 sec
DVDT Control During Start-Up	Unchecked	
Power Good Reset	Unchecked	

QUICK START PROCEDURE

Basic Operation

Set JP4 to RTN, and JP7 to VEE. These are the default stuffing positions. Connect an interface cable to DC1613 via J2 and connect a PC to DC1613 via its USB interface.

After first verifying that the supply is off and the load is disabled, connect a 48V supply capable of at least 50A to -48VIN and RTN, and connect a load across -48VOUT and RTN. As previously described, the load RTN may be connected directly to the supply, and DC2480A's RTN terminal connected through a small test lead.

Turn on the supply. The LTC4283 is configured to turn on autonomously after application of power. Once the output is up, as indicated by the -48VOUT LED (DLED6) and the PG1# and PG2# LEDs (DLED1 and DLED2), the load may be enabled. The LTpowerPlay GUI may be started at any time.

If two supplies are available, the Supply Monitor Inputs may be connected to the appropriate terminals ahead of the ORing diodes. The matching negative-side diode OR board is DC2180A, which features the LTC4371.

A Note About Grounding

“Ground” reference for DC2480A is -48VIN and the attached V_{EE} plane, whereas in an actual system RTN closely tracks Earth and chassis ground. For bench testing where the input supply is floating, -48VIN and VEE can serve as the reference ground, such as for oscilloscope probing.

The DC590, DC1613 and DC2026 interface boards are fully isolated and can be used regardless of whether -48VIN or RTN is ground referenced.

DEMO MANUAL DC2480A



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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Rev. 0