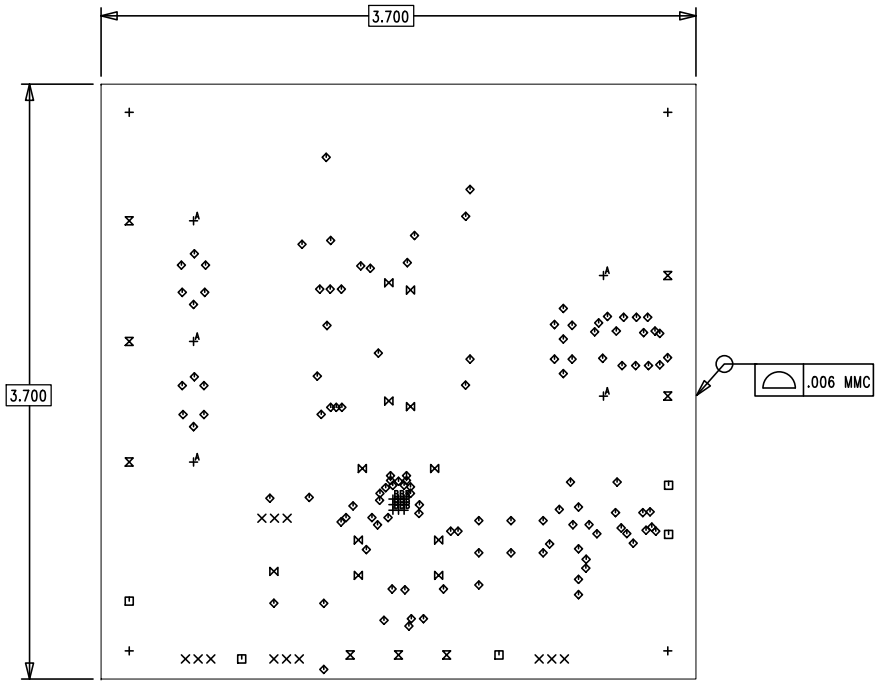


PCB#600-DC2707B REV02

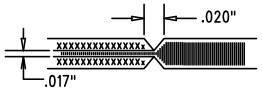
SIZE	QTY	SYM	PLATED	TOL
188	4	+	NO	+/- 3 MILS
35	12	X	YES	+/- 3 MILS
65	5	□	YES	+/- 3 MILS
12	120	◇	YES	+/- 3 MILS
95	8	⧖	YES	+/- 3 MILS
25	11	⋈	YES	+/- 3 MILS
207	5	+A	YES	+/- 3 MILS
13	9	+B	YES	+/- 3 MILS

DRILL CHART

REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE

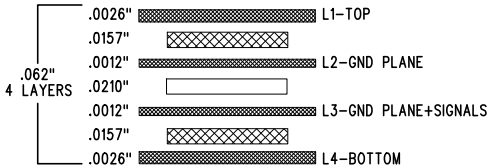
NOTES: UNLESS OTHERWISE SPECIFIED

1. FAB PER IPC-A-600.
2. MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR-370HR OR EQUIVALENT
   -FINISHED THICKNESS TO BE 0.062" +/- .005"
   -TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
   -FLAMMABILITY RATING: 94 V-0 MINIMUM.
3. SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.
4. DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
   -ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
5. FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.
   -ENIG BOTH SIDES.
   -SILKSCREEN LEGENDS SHALL BE WHITE NON-CONDUCTIVE EPOXY INK.
6. DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE. PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
7. PCBS ARE TO BE RoHS COMPLIANT.
8. BOARDS SHALL BE PANELIZED BY SCORING AS PER SPECIFICATION BELOW:



9. ALL ELECTRICAL TEST STAMPS SHALL BE ON BOTTOM SIDE.
10. ALL 13 MIL DIA. VIAS, QTY 9, SHALL BE IPC 4761 TYPE VII FILLED AND CAPPED VIAS. USE NON-CONDUCTIVE FILLER.
11. SOLDER AND PASTE MASK LAYERS ARE PROVIDED AS ZERO-CLEARANCE DATA.
12. STACKUP AS PER FIGURE 1 BELOW.

FIGURE 1- STACKUP DETAILS



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
0.XX" = ±0.01"
0.XXX" = ±0.005"
INTERPRET DIM AND TOL PER ASME Y14.5M-1994
THIRD ANGLE PROJECTION

APPROVALS	
ENG.	M. HAWKINS
APP ENG.	VLADIMIR O.
SCALE = NONE	

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TITLE: FABRICATION DRAWING
DUAL CHANNEL
PRIORITIZED POWERPATH CONTROLLER

SIZE	IC NO.	DWG. REV.
N/A	LTC4418-UF DEMO CIRCUIT 2707B	02

SHT 1 OF 1