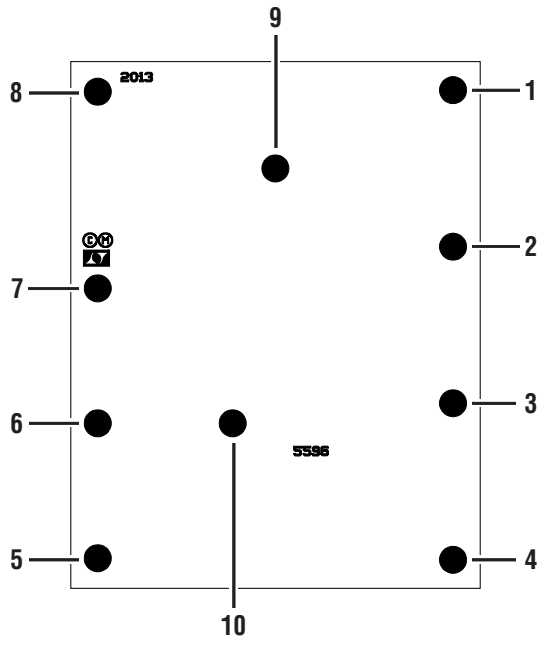
LTC5596
100MHz to 40GHz Linear-in-dB RMS Power Detector with 35dB Dynamic Range



PAD NUMBER	PAD NAME	X-Coordinate (µm)	Y-Coordinate (µm)	X-Coordinate (Mil)	Y-Coordinate (Mil)
1	V_{CC}	460.79	609.00	18.14	23.98
2	OUT	460.79	203.00	18.14	7.99
3	FLTR	460.79	–203.00	18.14	–7.99
4	GND	460.79	–609.00	18.14	–23.98
5	GND	–460.79	–605.00	–18.14	–23.82
6	RF_{IN}	–460.79	–255.00	–18.14	–10.04
7	GND	–460.79	95	–18.14	3.74
8	EN	–460.79	605.00	–18.14	23.82
9	GND	0.00	406.00	0.00	15.98
10	GND	–110.79	–255.00	–4.36	–10.04

DIE CROSS REFERENCE

LTC Finished Part Number	Order Part Number
LTC®5596	LTC5596DICE

Please refer to LTC standard product data sheet for other applicable product information.

PAD FUNCTION

1. V_{CC}
2. OUT
3. FLTR
4. GND
5. GND
6. RF_{IN}
7. GND
8. EN
9. GND
10. GND

Die size: 47mils × 59mils, (1193.8µm × 1498.6µm)
Die thickness: 8mils, ±0.6mils (203.4µm, ±15µm)
Backside material: Silicon
Backside potential: GND
Pad opening: 2.756mils (70µm)

Bonding Recommendations
Bond Force: 20g
Ultrasonic Power: 85mW
Duration: 15ms
Bonding Temperature: 200°C

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) 3.8V
RF_{IN} Input Signal Power – Average.....15dBm
RF_{IN} Input Signal Power – Peak (Note 2).....20dBm
DC Voltage at RF_{IN} ..... –0.3V to 1V
DC Voltage at FLTR..... –0.3V to 0.4V
DC Voltage at EN..... –0.3V to 3.8V
T_{JMAX} ..... 150°C
Storage Temperature Range..... –65°C to 150°C

DICE/DWF ELECTRICAL TEST LIMITS

T_A = 25°C. V_{CC} = 3.3V, EN = 3.3V. CW, 50Ω source at RF_{IN}, f_{RF} = 2140MHz, test circuit is shown in Figure 1. (Note 2).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUT Interface					
Output DC Voltage	No RF Signal Present EN = 1.1V		1.0	5.0	mV
Enable (EN) Low = Off, High = On					
EN Input High Voltage (On)		1.1			V
EN Input Low Voltage (Off)				0.6	V
EN Pin Input Current			50	500	nA
Power Supply					
Supply Voltage		2.7	3.3	3.6	V
Active Supply Current	EN = 3.3V	25	30	35	mA
Shutdown Supply Current	EN = 0V		50	500	nA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. The voltage on all pins should not exceed 3.8V, V_{CC} + 0.3V or be less than –0.3V, otherwise damage to the ESD diodes may occur.

Note 2: Not production tested. Guaranteed by design and correlation to production tested parameters.

PAD FUNCTIONS

V_{CC} (Pad 1): Power Supply Pad. Typical current consumption is 30mA at room temperature. This pad should be externally bypassed with a 100nF capacitor.

OUT(Pad 2): Detector Output. The DC voltage at this pad varies linearly with the RF input power level in dBm. This output is able to drive a 50Ω load. To avoid permanent damage, do not short to V_{CC} or GND. In shutdown mode (EN = Low), this interface become high impedance, to avoid discharge of capacitors in an external ripple filter.

FLTR (Pad 3): An optional capacitor connected between FLTR and OUT (Pad 2) reduces the detector ripple averaging bandwidth. This will also increase the rise and fall times of the detector. To avoid permanent damage to the circuit, the DC voltage at this pad should not exceed 0.4V.

GND (Pads 4, 5, 7, 10): Circuit Ground. All ground pins are internally connected together. Pads 5 and 7 should be used as RF return ground and connected to the transmission line interfacing to RF_{IN} (Pad 6).

RF_{IN} (Pad 6): RF Input. This pad is internally DC-coupled to GND through a 50Ω termination resistor. To avoid damage to the internal circuit, the DC voltage applied to this pad should not exceed 1V. The ground-signal-ground arrangement of Pads 5 through 7 support termination of Pad 6 by a high frequency transmission line, such as a grounded co-planar waveguide (GCPW). No external decoupling capacitor is necessary as long as the DC voltage on Pad 6 is kept below 1V.

EN (Pad 8): Chip Enable. A voltage above 1.1V applied to this pad will bring the device into normal operating mode. A voltage below 0.6V will bring the device into a low power shutdown mode. Do not float this pad.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-5596