Application and Optimization of a 2GHz Differential Amplifier/ADC Driver

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1 INTRODUCTION

Modern high speed analog-to-digital converters (ADC), including those with pipeline or successive approximation register (SAR) topologies, have fast switched-capacitor sampling inputs. The highest performance parts maintain low input noise and low signal distortion (high linearity) while consuming less power with each new generation. At the same time, they are sampling at ever increasing rates, which enables wider signal bandwidths and relaxes the requirements for analog antialias filtering. The switched-capacitor inputs result in significant charge injection with every switch movement, which requires a front end that can absorb that charge and settle to the correct voltage by the time the ADC input switches again, in nanoseconds or less.

The task of the ADC driver amplifier is to meet all of these requirements. A good driver must have the ability to output a signal of full-scale amplitude for the ADC with low distortion and low noise to maintain the dynamic range of the ADC. Also, the ADC driver (and any antialias filtering) must be able to withstand the ADC's switch charge injection and recover before the next switch movement to minimize signal degradation. In the ADC driver, this implies good transient response and wide bandwidth relative to the ADC's sampling frequency.

1.1 LTC6400 Features

Linear Technology's LTC®6400 family of ADC drivers addresses all three issues with a low distortion and low noise ADC driver with reasonable power dissipation. At 70MHz, which is a common IF frequency used in RF/IF signal chains, the LTC6400 family boasts distortion as low as –94dBc (equivalent output IP3 = 51dBm)[1] and input-referred noise density of 1.4nV/$\sqrt{Hz}$. This allows the LTC6400 family to be used with high performance 14-bit and 16-bit ADCs without compromising their performance. The power draw of the LTC6400 family is as low as 120mW on a single 3V supply.

The LTC6400 comes in two versions, one with the highest performance (LTC6400) and another with half the power draw (LTC6401). To facilitate ease of design and layout, there are four fixed-gain options for each (8dB, 14dB, 20dB and 26dB) for a total of eight parts in the family. The input impedances of the parts vary from 50Ω to 400Ω, which is convenient for impedance matching. The LTC6400 family is unconditionally stable with any input and output termination, and in fact the output does not require any impedance-matching components when driving an ADC. The LTC6400 keeps the overall solution size small with its 3mm × 3mm QFN package that requires only a few external power supply bypass capacitors for operation.

This Application Note discusses the features and boundaries of the LTC6400 family and how to achieve optimal performance from the amplifiers in real applications.

1.2 Internal Gain/Feedback Resistors

The LTC6400 is manufactured with internal gain and feedback resistors, for a complete differential amplifier solution that is simple to use and less susceptible to parasitic capacitances on the PCB layout than differential amplifiers without internal resistors. This is because the sensitive amplifier feedback loop nodes are contained within the chip.

The benefit of internal resistors can be visualized in Figure 1-1 and Figure 1-2. The first shows a traditional high speed differential amplifier IC, with parasitic inductance and capacitance affecting the stability and frequency

Note 1. See Section 10.2 for a definition of "Equivalent Output IP3."

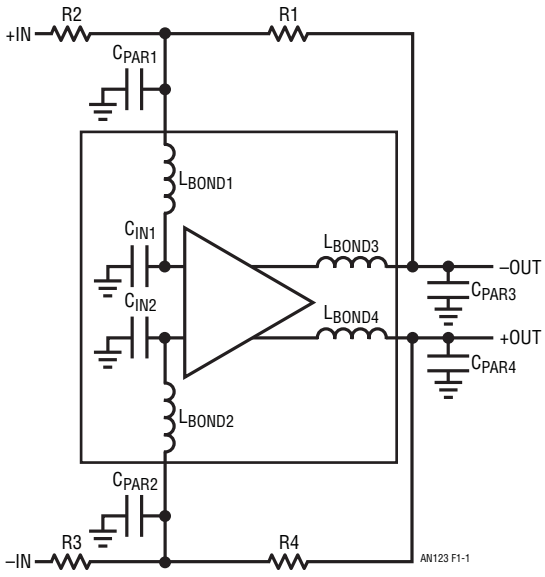


Figure 1-1. A Typical High Speed Differential Amplifier Circuit with Parasitic Elements that Can Degrade Performance. The Differential Amplifier IC is Shown in the Box. The Bond-Wire Inductance of the Package and the Parasitic Capacitances, Both Internal and External, Will Reduce the Phase Margin of the Amplifier. Notice that the Output Load is in the Feedback Path

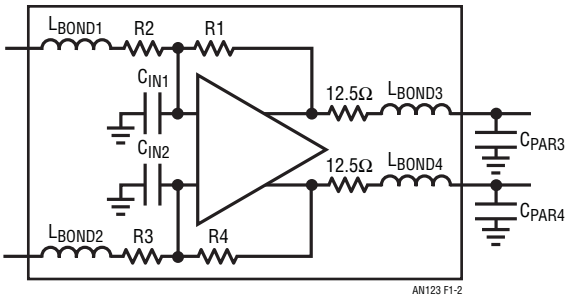


Figure 1-2. A Differential Amplifier IC with Internal Resistors, Such as the LTC6400. Note that the Bond-Wire Inductances are Not Inside the Feedback Loop, and that the Output Load is Isolated from the Feedback Loop Due to the Resistors and Bond-Wire Inductance. The Input Capacitance of the Differential Amplifier Can Still Affect the Performance, but it is Predictable and Can be Compensated for in the IC Design

response of the amplifier. The second shows the same parasitic elements in an LTC6400 style amplifier with internal resistors. The parasitic elements are outside of the critical feedback loop, and actually help to isolate the output load from the amplifier.

With the LTC6400's internal components, the only required external components are bypass capacitors, which should still be located as close to the amplifier's package as physically possible. For more information and recommendations on PCB layout, see the Layout section of this Application Note.

2 LOW DISTORTION

The LTC6400 family is manufactured on a very high frequency silicon germanium process, and crosses the divide between traditional operational amplifiers (op amps) and RF/IF amplifiers. The LTC6400 maintains very low distortion and low noise with the capability of handling signals at high intermediate frequencies (IF). This allows the LTC6400 to be used in demanding IF sampling applications of radio receiver signal chains. However, the LTC6400 is still topologically similar to traditional op amps in the use of feedback to achieve its high gain and DC performance.

The block diagram of the LTC6400-14 (14dB fixed gain), shown in Figure 2-1, shows similarities to traditional differential op amps. The main difference lies in the use of internal resistors and other frequency compensation components. By keeping the most sensitive nodes of the amplifier inside the package, the LTC6400 is able to

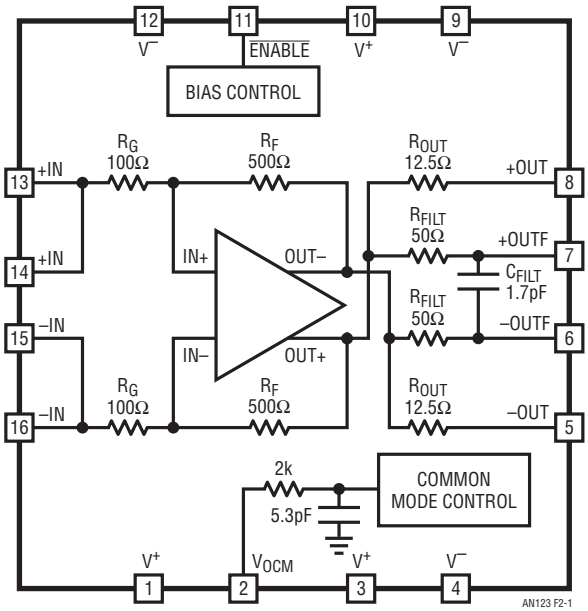


Figure 2-1: Block Diagram of the LTC6400-14. The LTC6400 Delivers IF Amplifier Performance, but is Topologically Similar to a Differential Op Amp in its use of Feedback

provide almost 2GHz of bandwidth while maintaining good stable performance in real-world layouts. In other words, the user does not need to worry about low product yields due to oscillating high frequency amplifiers. The LTC6400 does still require attention to layout (see the Layout section of this Application Note), but the most difficult part is already done.

2.1 Actual Bandwidth vs Usable Bandwidth

The LTC6400 has a very wide bandwidth (approaching 2GHz), but the vast majority of applications will not require frequencies beyond a few hundred Megahertz. The reason lies in the topology. Unlike traditional "open-loop" RF/IF amplifiers, where there is very little or no feedback used in the amplifier circuit, the LTC6400 contains an internal differential op amp with the gain set using a feedback network. The internal amplifier's open-loop gain is much higher than the gain externally, and the amplifier is compensated to push out the overall loop gain roll-off to higher frequencies. The main reason that a "closed-loop" op amp is able to achieve great distortion performance is the combination of feedback and high loop gain, which is able to reduce any distortion created within the amplifier. Once the loop gain begins to roll off at higher frequencies, the distortion performance begins to suffer.

Figure 2-2 shows the 3rd order intermodulation distortion (IMD) products from a 2-tone signal test of the LTC6400-20.[2] At low frequencies, the distortion products approach –100dBc. However, the performance is still good even up to 250MHz-300MHz, which makes the LTC6400 suitable for even mid-to-high IF systems. However, it is important to note that the LTC6400 does not maintain great distortion performance all the way up to its actual –3dB bandwidth.

In other applications, the high bandwidth of the LTC6400 can be a significant advantage. With a slew rate of up to 6700V/µs[3] and a 2V step 1% settling time as fast as 0.8ns, the LTC6400 can be used in high performance video and charge-coupled device (CCD) applications with good results. The wide bandwidth of the LTC6400 results in flat gain to hundreds of Megahertz; Table 4-1 summarizes the gain flatness specifications in the data sheets.

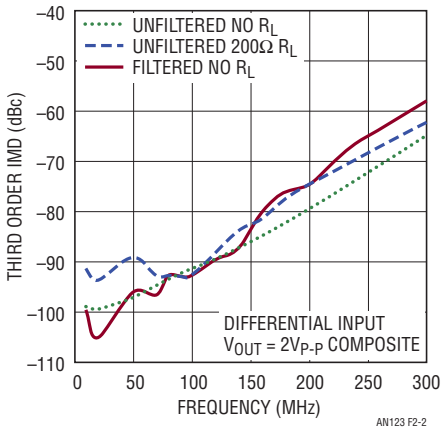


Figure 2-2: LTC6400-20 2-Tone 3rd Order Intermodulation Distortion. The Feedback Topology of the LTC6400 Means that the Distortion Performance Falls with the Loop-Gain Over Frequency

2.2 Low-Frequency Distortion Performance

A standout ability of the LTC6400 among high speed amplifiers is that it can accept inputs down to DC. From Figure 2-2, it can be inferred that the distortion performance approaches or exceeds –100dBc at lower frequencies (10MHz and below). This enables the LTC6400 to be used in very high performance low frequency and baseband systems to provide gain with no measurable degradation in the signal. The low 1/f noise "corner frequency" (on the order of 12kHz) means that the low noise performance of the LTC6400 is maintained well below 1MHz. Although the LTC6400 has low distortion at 100MHz and above, it also has phenomenal distortion performance at 20MHz and below. Figure 2-3 shows measured distortion data with input frequencies as low as 1MHz.

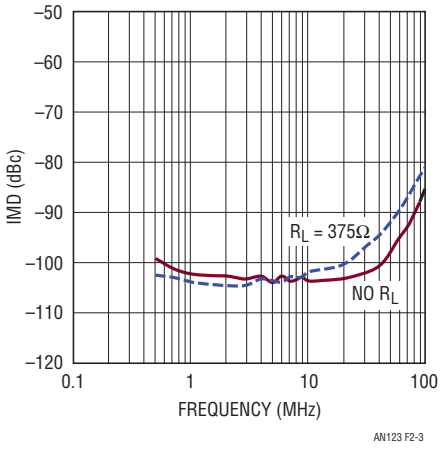


Figure 2-3. LTC6401-14 Low Frequency Distortion. Results Obtained from Lab Experiments Show that the Distortion of the LTC6400 Family is Better than –100dBc at Frequencies Below 40MHz, Making it an Excellent Choice for Lower Frequency Applications

2.3 Distortion Performance Guaranteed

One of the more unique features of the LTC6400 is the guaranteed distortion specification on the data sheet. Each unit is individually tested in production to meet specifications for functionality, which typically includes gain, offset, supply current, etc. The LTC6400 is unusual among available amplifiers in that each unit is also tested for distortion performance. The production test applies a two-tone input signal and measures the 3rd order intermodulation distortion. Table 2-1 lists the guaranteed distortion specification for each member of the family.

Note 2. For a general discussion on how to measure very low intermodulation distortion products, see (Seremeta 2006).

Note 3. A slew rate of 6700V/µs results in a $2V_{P-P}$ full power bandwidth of 1.066GHz

Table 2-1. Typical and Guaranteed 2-Tone 3rd Order IMD Specifications for the LTC6400 Family of Products. These Specifications are Measured and Guaranteed at Room Temperature

PART NUMBER	INPUT FREQUENCIES (MHz)	TYPICAL IMD (dBc)	GUARANTEED IMD (dBc)
LTC6400-8	280, 320 (IMD Measured at 360MHz)	–59	–53
LTC6400-14		–63	–57
LTC6400-20		–70	–64
LTC6400-26		–68	–62
LTC6401-8	130, 150 (IMD Measured at 170MHz)	–75	–67
LTC6401-14		–70	–61
LTC6401-20		–69	–61
LTC6401-26		–70	–62

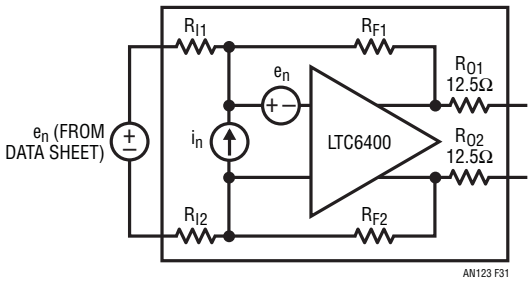


Figure 3-1. Equivalent Noise Sources of the LTC6400. e_n is the Equivalent Input Voltage Noise Source, and i_n is the Equivalent Differential Input Current Noise Source. In This Example, the Resistors Would Not be Considered Noiseless for Noise Calculation Purposes. The Extra Voltage Source External to the LTC6400 is the e_n Value That is Listed in the Data Sheet, Assuming R_S = 0Ω

Typically an amplifier's DC specifications are measured, and the AC performance (including distortion) is simply assumed. However, this means that from part to part there can be large variations in actual performance, which can cause the need to design in large performance margins or potentially sacrifice product yield. With a guaranteed specification in the data sheet for distortion, a design can proceed with more confidence knowing exactly what to expect from the amplifier.

3 LOW NOISE

The challenge of specifying the noise of the LTC6400 family stems from its dual role as a RF/IF signal chain gain block and a traditional voltage-gain differential amplifier. The data sheet specifications of voltage/current noise density (nV/√Hz and pA/√Hz) and noise figure (NF) must be correctly interpreted for the user's application. To make things more complicated, the LTC6400 is flexible in source and load impedance, which means that all the noise specifications can change depending on the circuit used. This section expands on the specifications in the data sheet and further explains how to correctly calculate the noise of the LTC6400 family.

Amplifier noise is typically described by an input equivalent noise voltage density, e_n, and noise current density, i_n. Figure 3-1 illustrates the equivalent noise sources. The voltage noise density can be measured by shorting the amplifier inputs, measuring the output voltage noise density, subtracting the effects of the resistors, and dividing by the amplifier's 'noise gain' for Z_S = 0. Note that in the case of a feedback amplifier, the noise gain may not equal the input/output signal gain[4]. The current noise density can be determined by connecting the amplifier inputs together with a resistor or capacitor (Z_S), measuring the output voltage noise density, subtracting the noise contribution due to e_n and Z_S, and dividing by the noise gain. For simplicity, the subtraction of the e_n and Z_S effects is done in an RMS fashion (square root of the difference of squares), with the assumption that e_n and i_n are uncorrelated noise sources. Through this procedure, input and output equivalent noise are obtained as shown in Table 3-1.

Notice that the e_n values in Table 3-1 differ from those in the LTC6400 data sheet. This is because the data sheet specifies a voltage noise density referred to the resistor inputs with the assumption that the source impedance is zero. In other words, the output voltage noise density from the data sheet is simply divided by the signal gain of the amplifier. This approach makes part-to-part comparison easier, but it does not lend itself well to general noise calculations with differing source and load impedances, etc. Establishing the noise sources in Figure 3-1 supplements the data sheet numbers and allows more general noise calculations to be made.

Note 4. See (Rich 1988) and (Brisebois 2005) for more background on amplifier noise analysis.

Table 3-1: Equivalent Input and Output Noise at 100MHz Based on the Internal Noise Sources in Figure 3-1. The First Two Rows, e_n and i_n, are Calculated Input-Referred Voltage and Current Noise Components of the Amplifier Alone, Excluding the Noise of the Internal Resistors

PART NUMBER	LTC6400-8	LTC6400-14	LTC6400-20	LTC6400-26
e_n (nV/√Hz)	1.12	1.15	1.03	1.01
i_n (pA/√Hz)	4.00	4.02	2.34	2.57
$e_{n(OUT)}$ (nV/√Hz) (R_S = 0, No R_L)	9.4	12.7	22.7	28.2

For source impedance, Z_S, the total output noise can be estimated by power superposition of contributions from resistive part of Z_S, e_n and i_n. However, this result could be misleading when Z_S is considerably high and/or frequency of interest is high.

There are some limitations to the data in Table 3-1 and its usefulness. Most importantly, e_n and i_n will have significant correlation, since they originate from the same physical noise sources inside the circuit. The RMS subtraction used here neglects this fact. The correlation of the voltage and current noise sources will have an impact on the accuracy of the calculations when $R_S > 100\Omega$ and i_n contributes a higher portion of the total noise at the output. This effect is examined in more detail in Appendix C.

Another limitation is that the e_n and i_n values obtained are only valid at 100MHz or below (down to the flicker noise corner frequency, approximately 12kHz), which is more than an order of magnitude lower than the –3dB bandwidth of the LTC6400. In a typical feedback amplifier, the output voltage noise density at higher frequencies can deviate significantly from the low frequency values (not considering 1/f noise). Figure 3-2 shows the output noise voltage of the LTC6400 family, which increase as the frequency approaches the –3dB bandwidth of the part. This increase in noise density is caused by the reduction in amplifier loop gain with frequency, which is affected by the internal amplifier gain, the compensation network, and the source and load impedances seen by the amplifier. At frequencies above the –3dB bandwidth, the output voltage noise density will fall with the gain of the amplifier.

3.1 Noise and NF vs Source Resistance

Figure 3-3 illustrates the measured total output noise voltage for various source resistors at 100MHz. Notice that the LTC6400-8/LTC6400-14/LTC6400-26 output noise curves converge as R_S approaches 1k. This is because all three

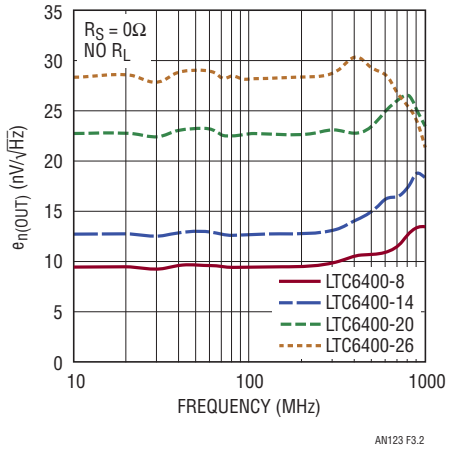


Figure 3-2. Total Output Noise Voltage Density vs Frequency. The Output Noise is Measured with the Differential Inputs Shorted Together and No Resistive Load on the Amplifiers. The Noise Does Not Scale Linearly with the Gain Values Because the Internal Resistor Values are not the Same.

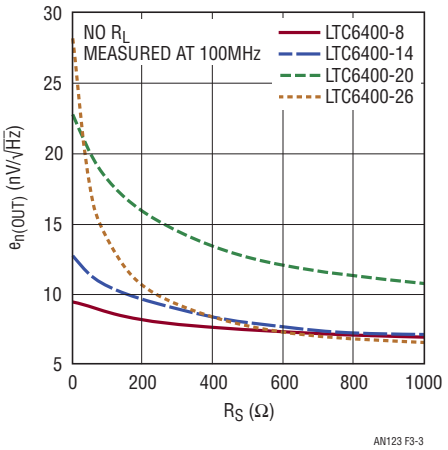


Figure 3-3. Total Output Noise vs Source Resistance at 100MHz. The Source Resistance is Installed Differentially Across the Two Inputs, and the Output Voltage Noise Density is Measured Without Any Load Resistance on the Amplifier. Note the Trend of Decreasing Output Noise with Increasing Source Resistance

versions have 500Ω feedback resistors and very similar internal amplifiers. On the other hand, the LTC6400-20 presents a much higher output noise as R_S approaches 1k. This is because the LTC6400-20 has a 1k feedback resistor, which means the effective noise gain is larger than that of the other parts. In addition, the larger feedback resistor contributes more noise direct to the output.

When the output noise curves in Figure 3-3 are translated to noise figure, producing Figure 3-4 (Equation 10-2), a slightly different story emerges. The amplifiers with a lower total output noise density (i.e., lower gains) do not necessarily have a lower noise figure. This is because NF is a measure of signal-to-noise ratio degradation, not absolute noise

(see Appendix A). Also, the noise figure curves shown in Figure 3-4 are not monotonic as R_S increases, but instead have a local minimum. There are two effects that are contributing to this result. First, the output voltage noise density of the amplifier levels off as R_S increases, but the source resistor noise continues to increase as R_S does. Second, Figure 3-5 and Figure 3-6 illustrate that the noise gain of the amplifier also decreases as the R_S value increases. So there are two terms increasing the noise figure and one term decreasing it, and the combination of these effects causes the NF to have a local minimum.

Another conclusion from Figure 3-6 is that low NF can be achieved with a certain range of R_S, but at the cost of overall voltage gain. The addition of R_{S1} and R_{S2} in Figure 3-5 contributes to additional input resistance, which lowers the gain. The conclusion is that it is not always desirable to use a source termination that yields the absolute lowest noise figure.

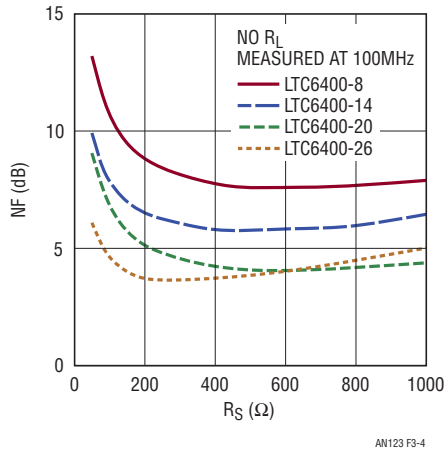


Figure 3-4. Noise Figure vs Source Resistance of the LTC6400. For Each Member of the Family, There is a Range of Source Resistances That Provide the Lowest Noise Figure Values

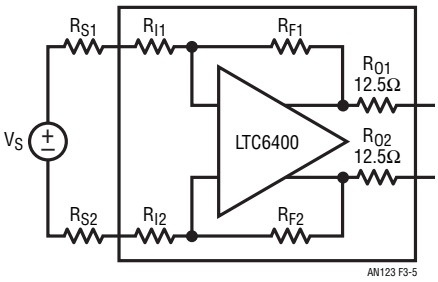


Figure 3-5. Diagram Showing the Effect of Increased Source Resistance on Overall Voltage Gain. The Source Resistance Adds to the Input Resistance, Which Decreases the Gain of the Amplifier

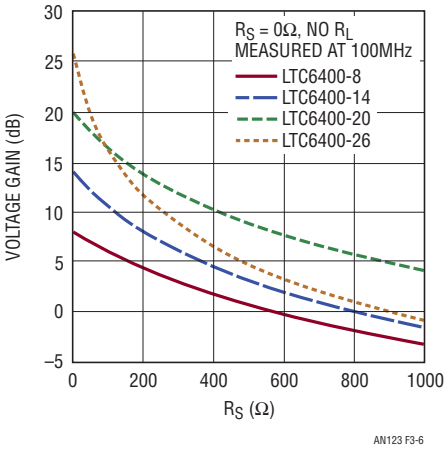


Figure 3-6. Voltage Gain vs Source Resistance for the LTC6400 Family. The Voltage Gain Defined Here is Calculated from the Source Voltage, V_S, in Figure 3-5 and Assumes No Resistive Load at the Output of the Amplifier

3.2 Noise and Gain Circles

The curves in Figure 3-4 show the effect of varying a real source resistance on noise and noise figure, but what happens if a complex source impedance is used? Noise circles are related to the concept of "minimum noise figure," where there is a certain complex input impedance that will yield the minimum noise figure for a given device at a given frequency, temperature and bias. It is also possible to plot circles of constant noise figure on the same Smith chart, so that any complex source impedance on each circle will yield the same NF. For a given source impedance Z_S, the noise factor of a 2-port system can be expressed relative to the minimum noise factor (Fukui 1981):

$$F = F_{MIN} + \frac{G_N}{R_S}\left|Z_S - Z_{OPT}\right|^2 \qquad (3\text{-}1)$$

where F_{MIN} is minimum achievable noise factor, G_N is the device's equivalent noise conductance, R_S is the resistive part of Z_S, and Z_{OPT} is the source impedance required to achieve the minimum noise factor. Figure 3-7 shows the noise circles for the LTC6400-8, and Table 3-2 lists the noise parameters for the entire LTC6400 family. The values indicate that inductive source impedances (with positive reactance) yield the optimal NFs for the LTC6400 family. However, when applying noise matching, it is important to remember that other performance factors such as gain, bandwidth and impedance mismatch are also affected by Z_S.

Table 3-2. LTC6400 Complex Noise Parameters Measured at 100MHz. These Parameters are the Basis for the Noise Figure Circles in Figure 3-7, and Allow the Precise Calculation of NF with Any Complex Source Impedance

	LTC6400-8	LTC6400-14	LTC6400-20	LTC6400-26
NF_{MIN} (dB)	7.12	5.6	4.01	3.55
G_N (mS)	1.13	2.45	2.86	7.23
Z_{OPT} (Ω)	531 + j306	440 + j131	516 + j263	272 + j86

One of the other key factors affected by source impedance is overall gain, and Figure 3-8 shows a set of gain circles for the LTC6400-8 plotted on the Smith chart. Transducer gain (G_T) is simply the ratio between power delivered to the load and power available from the source.

Figures 3-7 and 3-8 illustrate the trade-off between noise figure and transducer gain. Looking at the two plots, the minimum NF and maximum G_T cannot be achieved simultaneously, since they are not located in the same spot on the Smith chart. One common strategy is to connect the two optimal points ($\Gamma_{S,OPT}$ and $\Gamma_{S,GT(MAX)}$) with a straight line and pick a source termination on that line, which comes close to optimizing both NF and G_T. However, in many cases the absolute minimum NF or maximum G_T is not truly necessary. Looking at Figures 3-7 and 3-8, there is a large area of the input reflection Smith chart that will achieve within 1dB of both optimal points. There is even a significant portion of the real axis available (including 400Ω), where reactive elements are not necessary, that would provide good performance as well as a wideband impedance match.

3.3 Signal-to-Noise Ratio vs Bandwidth

Amplifiers such as the LTC6400 family are typically specified in noise voltage density, with units of nanovolts per root Hertz. When used in practical applications, the question often arises about how to interpret this noise metric to figure out exactly how much performance can be achieved in a system design. Depending on the system, there are many ways to characterize the effect of noise on a signal, but one of the most widely used is signal-to-noise ratio (SNR). SNR is simply a ratio of the maximum possible signal to the total amount of noise present, which determines the dynamic range of the system. The implication is that a signal small enough to be "in the noise floor" is not detectable, which is not always true, but SNR allows different designs to be compared side by side.

The LTC6400 family consists of very broadband amplifiers, with –3dB bandwidths over 1GHz. Making the assumption that all the noise is white noise, meaning the noise power density is constant with frequency, the total amount of integrated noise can be calculated by

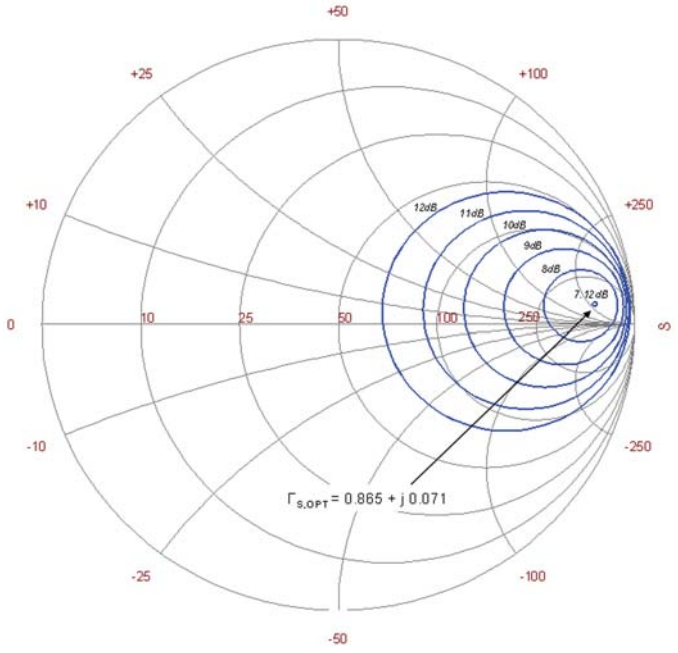


Figure 3-7. LTC6400-8 Noise Circles on the S11 Reflection Plane at 100MHz

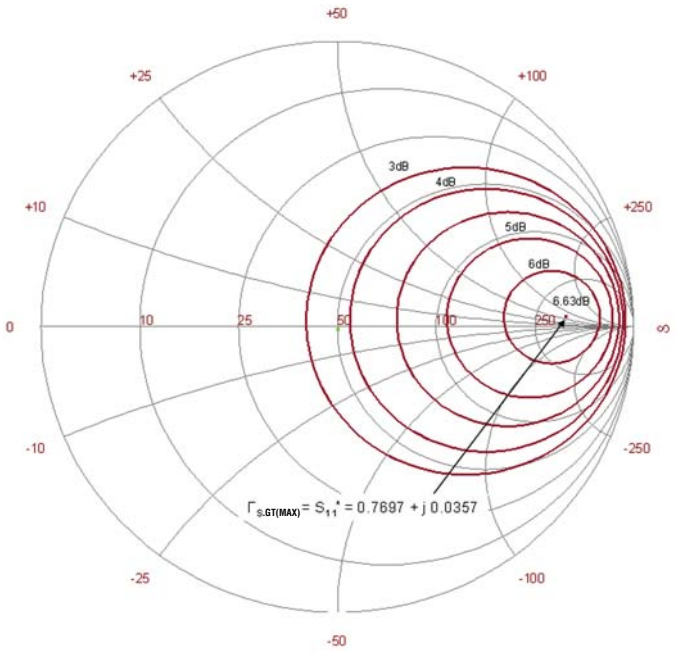


Figure 3-8. LTC6400-8 Gain Circles on the S11 Reflection Plane at 100MHz with R_L = 375Ω

multiplying the noise voltage density by the square root of the total bandwidth.

$$E_{n,TOTAL} = e_n\ (nV/\sqrt{Hz}) \bullet \sqrt{\alpha \bullet BW}\ nV_{RMS} \qquad (3\text{-}2)$$

where α = Scale factor to include the noise outside the BW, approximately 1.57 for a 1st order roll off and 1.11 for a 2nd order roll off.

Wide bandwidth amplifiers like the LTC6400 can have a significant impact on SNR. With a –3dB bandwidth of 1GHz, e_n is multiplied by 40,000 in Equation 3-2, so a 10nV/$\sqrt{Hz}$ amplifier output would contribute 400μV_{RMS} of integrated noise. If the maximum output signal is $2V_{P-P}$ ($0.71V_{RMS}$), as is the case for a typical high speed ADC input, then the maximum theoretical SNR is 1768, or 65dB. This is the SNR of an ADC with 10.5 bits of resolution.

As shown in Table 3-1, the higher gain versions of the LTC6400 have output noise voltage densities up to 28nV/$\sqrt{Hz}$. Although the high gain implies that the input-referred noise is very low, the output noise can be significant. The trend in signal conditioning is toward lower supply voltages, and so the maximum signal level (and thus the achievable SNR) is shrinking. For this reason, when driving a 16-bit (or even a 14-bit) ADC, it is almost always desirable to add some filtering at the output of the LTC6400. The design of this external filter depends on the desired input signal bandwidth and the target SNR that is required.

$$SNR_{TARGET} = 20 \bullet \log\left(\frac{V_{SIGNAL}}{E_{n,TOTAL}}\right) dB \qquad (3\text{-}3)$$

where V_{SIGNAL} = maximum input signal in V_{RMS}, which can be up to 0.88V for a high performance 3V ADC ($2.5V_{P-P}$).

This SNR calculation ignores the contribution of noise from the ADC. The SNR from the amplifier can be one of the dominant factors in determining the effective ADC resolution. Due to the LTC6400's excellent distortion performance, it is often paired with high performance 14-bit and 16-bit ADCs, and so the bandwidth should be limited in order to achieve the best overall performance.

An important phenomenon that occurs in ADCs is aliasing, which effectively "folds" frequency bands on top of each other, making them indistinguishable in the digital domain. Aliasing does not change the SNR calculation above, but it does affect the ability of any additional digital filtering to improve the SNR. If all of the noise is contained in one Nyquist bandwidth (the width of which is $f_{SAMPLE}/2$), then additional digital filtering can remove noise around the desired signal. However, if many Nyquist bandwidths of noise are aliased together with the desired signal band, then the beneficial effect of digital filtering would be diminished.

A sample calculation along with some further explanation of the noise aliasing phenomenon appears in section 11.3.

4 GAIN AND POWER OPTIONS

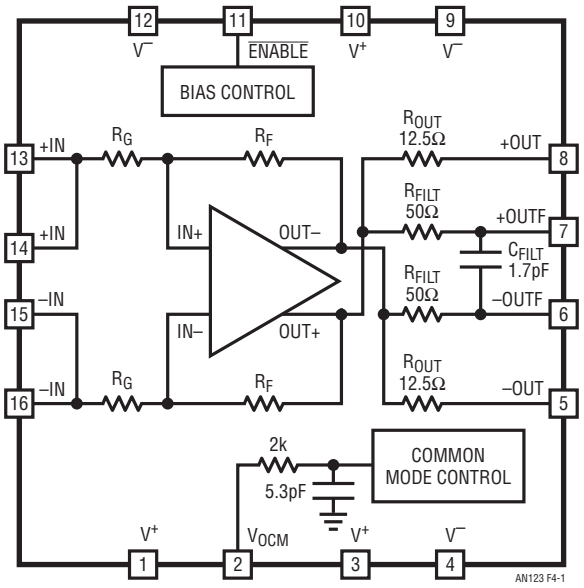
For application flexibility, the LTC6400 and LTC6401 product families come in four different gain versions: 8dB (2.5V/V), 14dB (5V/V), 20dB (10V/V) and 26dB (20V/V). The voltage gain is specified in decibels to maintain consistency with other RF/HF components in the signal chain. Figure 4-1 shows the block diagram of the LTC6400/LTC6400-1.

The gains specified are voltage gains from the input pins to the output pins. Unlike some amplifiers that specify power gain with a known load impedance value, the LTC6400 specifies a voltage gain that does not imply any specific input or output termination.

In addition to the choice of voltage gain, the user also has the choice between the LTC6400 and LTC6401 parts. This choice is mainly a speed/power trade-off; the LTC6400 is the fastest, lowest distortion amplifier and the LTC6401 is a lower power version optimized for lower input frequencies. The LTC6400 maintains good distortion performance out to 300MHz, and the LTC6401 does so out to 140MHz.

4.1 Gain, Phase and Group Delay

Providing the gain and feedback resistors internally also enables optimization in the compensation networks within each amplifier in the product family. Therefore, each gain variation of the LTC6400 has similar bandwidth (>1GHz) and minimal peaking in the gain response. Although the usable low distortion bandwidth of the products are much lower in frequency than the –3dB bandwidths, in certain situations gain flatness and phase linearity can be important. Figure 4-2 shows the gain of the LTC6400-20 to be flat within 0.1dB out to approximately 300MHz, and the phase to be linear out to beyond 1GHz. Table 4-1 summarizes the bandwidths of each LTC6400 and LTC6401 version.



VOLTAGE GAIN	R_G	R_F
8dB	200Ω	500Ω
14dB	100Ω	500Ω
20dB	100Ω	1kΩ
26dB	25Ω	500Ω

FAMILY	SUPPLY CURRENT	INPUT FREQUENCY FOR LOW DISTORTION
LTC6400	85mA TO 90mA AT 3V	DC – 300MHz
LTC6401	45mA TO 50mA AT 3V	DC – 140MHz

Figure 4-1. LTC6400/LTC6401 Block Diagram and Product Information Tables for the Various Gain and Speed/Power Options Available

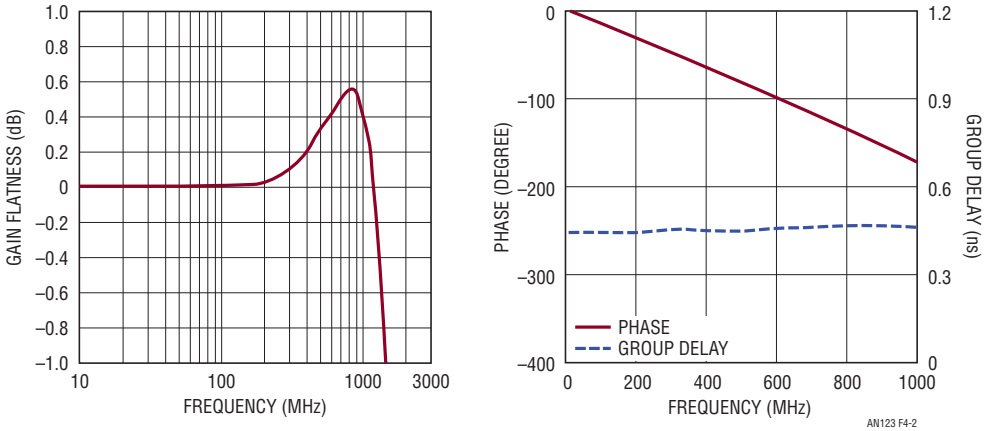


Figure 4-2. Gain Flatness and Phase/Group Delay Plots of the LTC6400-20

4.2 Gain of 1 Configuration

In some situations, a simple buffer may be required to drive an ADC with no gain or even attenuation. In this special case, series resistors can be used in front of the LTC6400-8 or LTC6401-8 to lower the gain to 0dB (1V/V). Due to the unconditional stability of the LTC6400, these resistors at the input will not cause instability or oscillation.

Figure 4-3 demonstrates the configuration. When combined with the internal gain resistors of the LTC6400-8, the amplifier becomes a unity-gain buffer with 1kΩ differential input impedance.

Table 4-1: Typical Bandwidth and 0.1dB/0.5dB Gain Flatness Frequencies for the LTC6400/LTC6401 Product Families

Product	–3dB Bandwidth	0.1dB Bandwidth	0.5dB Bandwidth
LTC6400-8	2.2GHz	200MHz	430MHz
LTC6400-14	2.37GHz	200MHz	377MHz
LTC6400-20	1.84GHz	300MHz	700MHz
LTC6400-26	1.9GHz	280MHz	530MHz
LTC6401-8	2.22GHz	220MHz	430MHz
LTC6401-14	1.95GHz	230MHz	470MHz
LTC6401-20	1.25GHz	130MHz	250MHz
LTC6401-26	1.6GHz	220MHz	500MHz

When combining external series resistors to lower the gain, there will be some temperature and initial accuracy limitations due to the characteristics of the LTC6400 family's internal resistors. While the internal resistors (200Ω and 500Ω in Figure 4-3) are designed to match well over process variations and temperature, their absolute values can vary as much as ±15% (as guaranteed by the LTC6400-8 data sheet). A ±15% variation in the internal resistors, when combined with an ideal 301Ω resistor in our example, will result in less than ±10% variation in the desired gain of the amplifier over temperature and process variations. This does not take into account temperature effects in the external resistor, which should not be expected to track with the internal resistors.

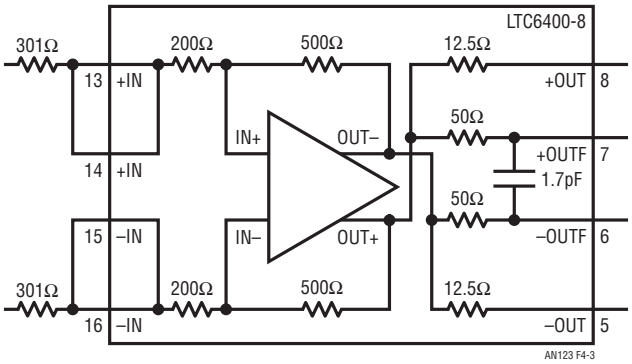


Figure 4-3. LTC6400-8 with Series Resistors to Lower the Gain to 1V/V (0dB)

5 INPUT CONSIDERATIONS

5.1 Input Impedance

The input impedance of a differential amplifier circuit depends on whether it is driven single-ended or differentially. This is significant when performing an impedance match to the amplifier for optimal power transfer or to maximize the voltage signal at the input.

Figure 5-1 shows the LTC6400 with a differential input. To calculate the input impedance, we need to calculate the input current I_{IN} flowing through the input voltage source, V_{IN}. With a fully-differential input and a high gain amplifier, there is very little voltage developed across the internal nodes (INT^+,INT^-). Therefore these nodes act as a differential "virtual short", in a similar fashion to the inverting node of a traditional op amp. Thus, the input impedance is simply the sum of R_{I1} and R_{I2}.

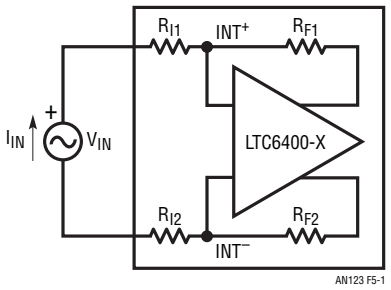


Figure 5-1: LTC6400 with a Fully Differential Input

Figure 5-2 shows the LTC6400 with a single-ended input. Assuming that the input signals are high enough in frequency that the DC blocking capacitors C1 and C2 look effectively like short circuits (these are necessary because of the input common mode voltage requirements of the LTC6400), the assumption of no voltage at the INT^+ and INT^- nodes is no longer valid. The *differential* voltage across (INT^+,INT^-) will still be small, but there will be a *common mode* voltage at the two nodes that is proportional to the input voltage.

$$V_{INT^+} \approx V_{INT^-} \approx V_{OUT^+} \bullet \frac{R_{I2}}{R_{F2}+R_{I2}} = V_{IN} \bullet \frac{R_{F2}}{2R_{I2}} \bullet \frac{R_{I2}}{R_{F2}+R_{I2}} = V_{IN} \bullet \frac{R_{F2}}{R_{F2}+R_{I2}} \quad (5\text{-}1)$$

$$I_{IN} = \frac{V_{IN}-V_{INT^+}}{R_{I1}} = \frac{V_{IN}}{R_{I1}} \bullet \frac{R_{F2}+2R_{I2}}{2\left(R_{F2}+R_{I2}\right)} \quad (5\text{-}2)$$

$$\text{Input Impedance} = V_{IN}/I_{IN} = \frac{2R_{I1}\left(R_{F2}+R_{I2}\right)}{R_{F2}+2R_{I2}} \quad (5\text{-}3)$$

As an example, with the LTC6400-20, which has 100Ω input resistors and 1k feedback resistors, the single-ended input impedance is 183Ω. This would be the input impedance

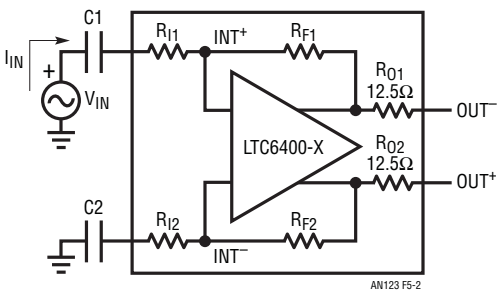


Figure 5-2: LTC6400 with Single-Ended Input

seen by V_{IN} in the example. Note that in the case of a V_{IN} with non-zero source impedance, such as a 50Ω signal source, it is beneficial to terminate the unused input with the same effective impedance to maintain balance. This will change the input impedance, and an updated formula can be found in section 5.6.

5.2 AC Coupling vs DC Coupling

The LTC6400 is tolerant of AC coupling or DC coupling at both the input and the output, but it does have a range of inputs and output voltages that must be adhered to for best performance. At the input, the common mode input voltage range is defined in the data sheet to be approximately 1V to 1.6V (with $V^+ = 3V$). The common mode input voltage is defined as the *average* voltage of the two inputs, and is separate from the *difference* voltage between the inputs. Input voltages that are centered at ground or at V_{CC} must therefore be level-shifted before being applied to the LTC6400. As a point of clarification, the common mode input voltage refers to the voltage at input pins of the IC (Pins 13 to 16), not the *internal* input pins of the op amp which are not accessible. Table 5-1 shows the differences between the data sheet common mode limits and the resultant internal node voltages (see Figure 5-1) that result. The data sheet limits are published with a set V_{OCM} of 1.25V, and assuming no additional source resistance. Changing either would shift the DC voltage at the internal nodes, which are the real determinant of the input common mode limits. However, following the common mode limits established in the data sheet only ensure that the input stage operates in the linear region; it does not imply the same performance will be achieved across the entire voltage range. Section 6.2 addresses the change in distortion for different common mode bias voltages, both at the input and at the output.

The limits in Table 5-1 are based on saturation limits of the input stage, and can be interpreted for the general case of an arbitrary V^+ and V_{OCM}. Changing the V^+ voltage increases the input stage headroom, and changing V_{OCM} changes the bias at the internal nodes, so both will affect the input common mode voltage limits. Referring to the values in Tables 5-1 and 5-2, the input common mode voltage limits can be calculated as:

$$V_{CM,IN(MIN)} = \beta(V_N + V^- - \alpha V_{OCM} - \delta V^+) \quad (5\text{-}4)$$

$$V_{CM,IN(MAX)} = \beta(V_P + (1 - \delta)V^+ - 3.0 - \alpha V_{OCM}) \quad (5\text{-}5)$$

Table 5-1. Limits of Input Common Mode Voltage as Published in the Data Sheet, and the Translated Common Mode Voltage Limits at the Amplifier's Internal Nodes. Knowing the Amplifier's Internal Node Voltages Allows a Design to Stay Within Data Sheet Limts Even with Alternative Configurations. The Internal Node Voltages V_N and V_P Include the Effect of a Small Pull-Up Current in the Amplifier.

		LTC6400-8	LTC6400-14	LTC6400-20	LTC6400-26
Specification from Data Sheet	Input Common Mode Voltage Minimum (I_{VRMIN})	V^- + 1.0	V^- + 1.0	V^- + 1.0	V^- + 1.0
	Input Common Mode Voltage Minimum (I_{VRMAX})	1.8 (V^+ – 1.2V)	1.8 (V^+ – 1.2V)	1.6 (V^+ – 1.4V)	1.6 (V^+ – 1.4V)
Internal Node Voltage Limits (INT^+, INT^-)	Common Mode Voltage Minimum (V_N)	1.24	1.14	1.05	1.02
	Common Mode Voltage Maximum (V_P)	1.76	1.78	1.59	1.59
		LTC6401-8	**LTC6401-14**	**LTC6401-20**	**LTC6401-26**
Specification from Data Sheet	Input Common Mode Voltage Minimum (I_{VRMIN})	V^- + 1.0	V^- + 1.0	V^- + 1.0	V^- + 1.0
	Input Common Mode Voltage Minimum (I_{VRMAX})	1.6 (V^+ – 1.4)	1.6 (V^+ – 1.4)	1.6 (V^+ – 1.4)	1.6 (V^+ – 1.4)
Internal Node Voltage Limits (INT^+, INT^-)	Common Mode Voltage Minimum (V_N)	1.16	1.09	1.05	1.03
	Common Mode Voltage Maximum (V_P)	1.57	1.58	1.59	1.59

Table 5-2. Constants Used to Calculate Input Common Mode Voltage Limits, Based on the Information Provided in the Data Sheet. Changing the Supply Voltage V^+ and the V_{OCM} Bias Voltage will Affect the Limits Published in the Data Sheet Electrical Tables. These Constants Include the Effect of a Small Pull-Up Current at the Internal Nodes of the Amplifier.

	LTC6400-8	LTC6400-14	LTC6400-20	LTC6400-26	LTC6401-8	LTC6401-14	LTC6401-20	LTC6401-26
Alpha (α)	0.261	0.158	0.090	0.047	0.273	0.162	0.090	0.047
Beta (β)	1.533	1.267	1.117	1.054	1.467	1.233	1.117	1.058
Delta (δ)	0.087	0.053	0.015	0.004	0.045	0.027	0.015	0.008

When calculating the input minimum and maximum voltages with the provided equations, it is important to keep the graphs in Figure 6-2 handy, as a cross-reference. The distortion performance of the LTC6400 family is much less sensitive to the input common mode voltage than the output common mode voltage, but the distortion performance will not be constant over the entire range.

If the inputs are AC-coupled with series capacitors, the inputs of the LTC6400 will self-bias to approximately the same voltage as V_{OCM},[5] and there is no need to apply an external bias voltage to the part. It is only when DC coupling the input that the design needs to address the biasing of the inputs. For more information about performance optimization and the input common mode voltage, see section 6.2.

When changing the input and output common mode voltages, it is important to be aware of changing input bias currents. Referring to the block diagram in Figure 2-1, DC bias currents will flow from the outputs back to the inputs through the gain and feedback resistors. The source must be able to source or sink this additional current, which can exceed a milliamp, when setting the DC bias of the LTC6400's input.

The outputs of the LTC6400 will automatically bias to the voltage at the V_{OCM} pin due to an internal common mode loop. This simplifies the task of mating the LTC6400 to Linear Technology's high performance 14-bit and 16-bit ADCs, because the common mode voltage requirements of the ADCs are typically very stringent, and the common mode rejection of the ADC inputs is often not very good.

5.3 Ground-Referenced Inputs

A common case of the DC-coupled application includes having a single-ended ground-referenced input for the ADC driver, where the DC voltage level of the input is at 0V. The LTC6400 has an input common mode range that does not include ground, so level-shifting of some sort is necessary to bring the voltages within the limits shown in Table 5-1 and Table 5-2.

If the input source is 50Ω terminated, one possible solution is shown in Figure 5-3. The inputs are pulled up with 75Ω resistors to the supply. This circuit takes advantage of the source's 50Ω termination to create a voltage divider and effectively level shift the input to within the optimal range for the LTC6400. The 75Ω resistors also act as impedance match resistors, transforming the single-ended input impedance of the LTC6400 to a value close to 50Ω.[6] Therefore, the extra pull-up resistors do not attenuate the input signal any more than necessary. Due to the LTC6400-26's lower intrinsic input impedance, the pull-up resistors should be changed to 100Ω, which will yield an input impedance of 42Ω.

Another method for level shifting employs two LTC6400's in series: one to level shift the signal, and another to add gain. Figure 5-4 shows an LTC6400-8 with 1.1k series input resistors to level shift and attenuate the signal. The internal DC bias level is within the LTC6400's range. At the output, an LTC6400-20 amplifies the signal for the ADC. The 200Ω input impedance is not a heavy load for the LTC6400-8. The total gain from the two amplifiers together is 10.7dB.

Note 5: In reality, the input common mode voltage is increased slightly by internal pull-up resistors to match the optimal values of input and output bias.

Note 6: The input impedance will be 61Ω with the LTC6400-8, 53Ω with the LTC6400-14 and 55Ω with the LTC6400-20. The impedance can be lowered by lowering the 75Ω resistor values at the expense of power dissipation.

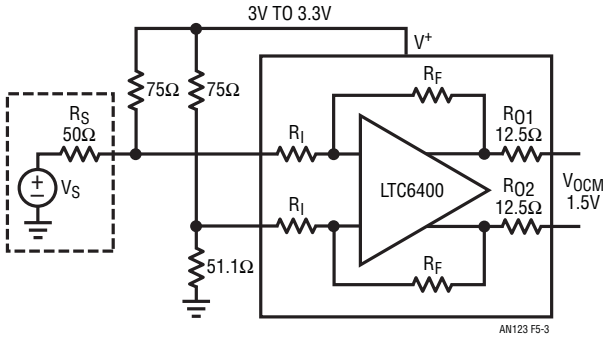


Figure 5-3. Using Pull-Up Resistors at the Input to Level-Shift a Ground-Referenced Signal and Provide Input Impedance Matching at the Same Time. The Unused Input is Similarly Terminated. The Drawback with this Approach is that a DC Bias Current Will Flow Through the Pull-Up Resistors, Dissipating Extra Power and Requiring the Input Source to Sink the Current

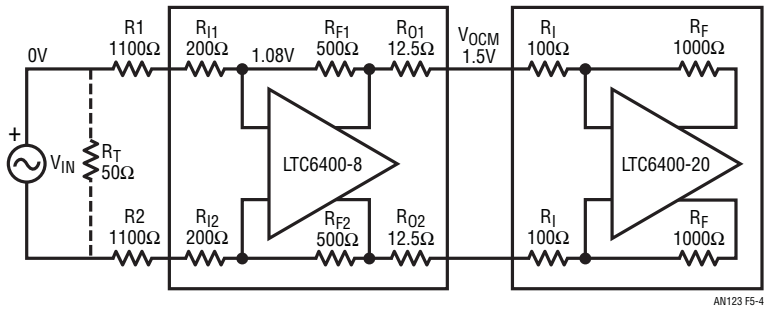


Figure 5-4. Use Two LTC6400 Amplifiers to Level Shift and Amplify an Input Signal. The LTC6400-8 has Series Input Resistors to Attenuate and Level Shift the Input, and the LTC6400-20 Adds Additional Gain at the Output. The Total Gain of this Circuit is 10.7dB, Including the Attenuation from the LTC6400-8 Input Resistors and the Effect of the 12.5Ω Output Resistors

5.4 Impedance Matching

Impedance matching is the art of achieving maximum power transfer from a source to a load. Achieving a good impedance match is beneficial for many reasons: maximum signal reception, no reflections to cause signal distortion, and good predictable behavior from the system. In this section, the LTC6400 family's input and output characteristics are discussed to provide the information necessary for impedance matching. A primer on impedance matching is outside of the scope of this note, but there are myriad texts and resources available that discuss it at length.[7]

The LTC6400 family provides differential input impedances ranging from 50Ω to 400Ω, and a differential output impedance of 25Ω. In applications where impedance matching is desired, such as when receiving or driving a SAW filter, a simple series L and shunt C network will often suffice. Figure 5-5 presents an example circuit to interface to a SAW filter. At operating frequencies below 100MHz, the LTC6400's input and output impedances are almost purely resistive. At frequencies above that, the reactance must be taken into account. Table 5-3 lists the relevant parameters for impedance matching, assuming the circuits in Figure 5-5 and Figure 5-6. To calculate the C and L values, divide the ωC and ωL values by ω (or 2πf), where ω is the frequency in radians/sec and f is the frequency in Hertz. Figure 5-7 shows the impedance match on the Smith chart.

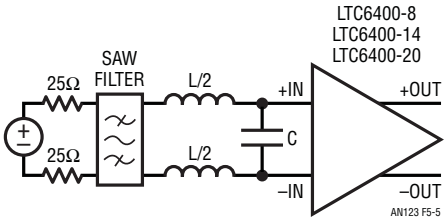


Figure 5-5. Example of Series-Shunt Input Impedance Matching to a SAW Filter. The LTC6400-26 has an Input Impedance of 50Ω, and Typically does not Require any External Elements for a 50Ω Impedance Match. Using an LC Network Provides an Impedance Match at a specific Frequency; for a Wideband Impedance Match, other Methods Such as Transformers and Resistors are Necessary

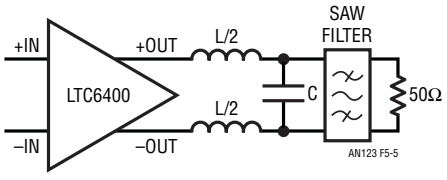


Figure 5-6. Example of Series-Shunt Output Impedance Matching to a SAW Filter. All Members of the LTC6400 Family have a 25Ω Resistive Output Impedance at Lower Frequencies

Table 5-3: Matching Circuit Parameters for the Circuits in Figure 5-5 and Figure 5-6. To Obtain the Capacitor and Inductor Values from this Table, Which are the Frequency-Independent ωC/ωL Values, Simply Divide the Number by ω (or 2πf). Since the Series Inductors are Differential, Each Inductor Will be Half of the Resultant Value. The LTC6400-26 Does Not Require Matching Elements, as its Input Impedance is 50Ω

	INPUT		OUTPUT
	LTC6400-8	LTC6400-14/20	LTC6400 (all) Unfiltered Output
ωC	0.00661	0.00866	0.02
ωL	132	86.6	25

Figure 5-8 and Figure 5-9, which show the input and output reflection coefficients from 10MHz to 1GHz, can provide the right impedance matching circuit to obtain a better impedance match at high frequencies. Note that the input impedance (of the LTC6400-8/LTC6400-14/LTC6400-20) becomes capacitive and the output impedance becomes inductive as the frequency increases above 100MHz.

Note 7: For impedance matching and general RF design, see (Bowick 1982).

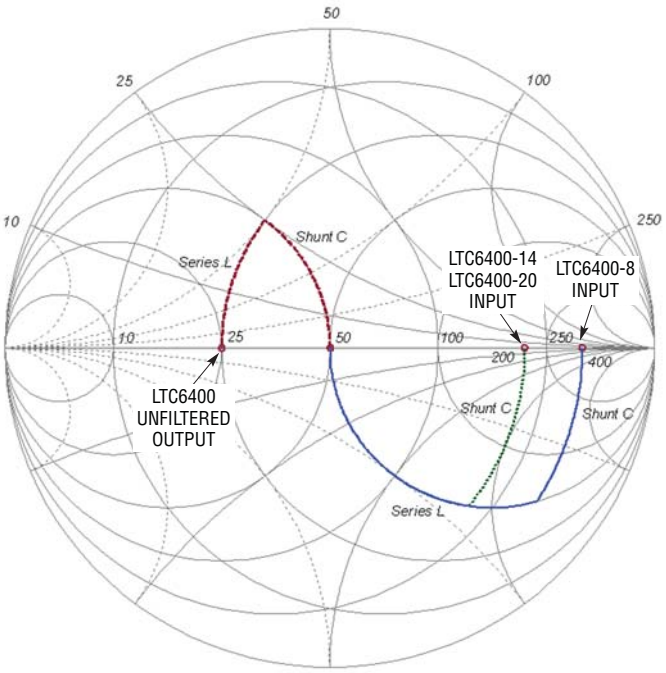


Figure 5-7. Differential Input and Output Impedance Matching to 50Ω. In Most Matches, a Series Inductor/Shunt Capacitor Network will Yield a Satisfactory Impedance Match.

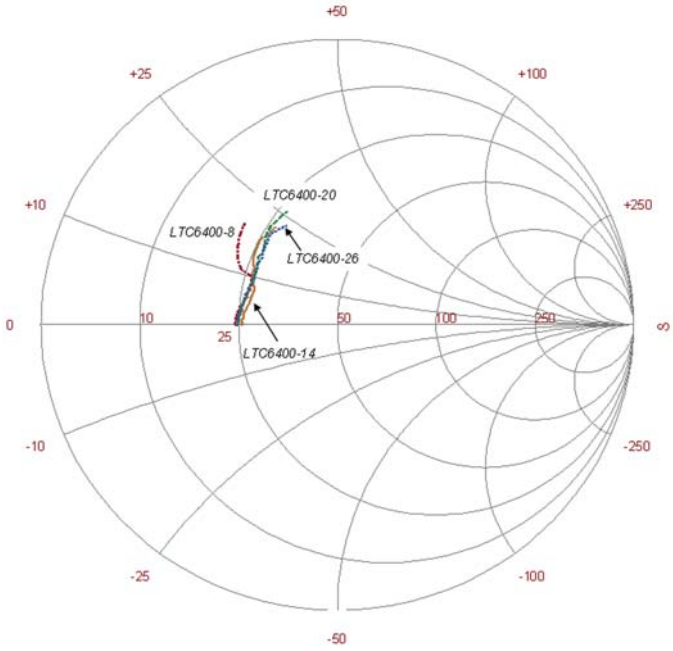


Figure 5-9. Output Reflection Coefficients (S22) of the LTC6400 Family from 10MHz to 1GHz. Below 100MHz or so, the Impedances are Almost Purely Resistive. Above that, the Reactances Must be Considered for Impedance Matching

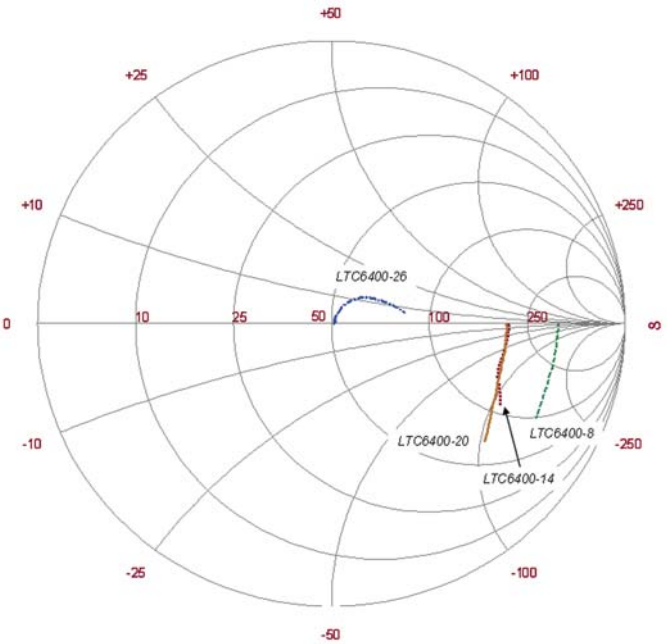
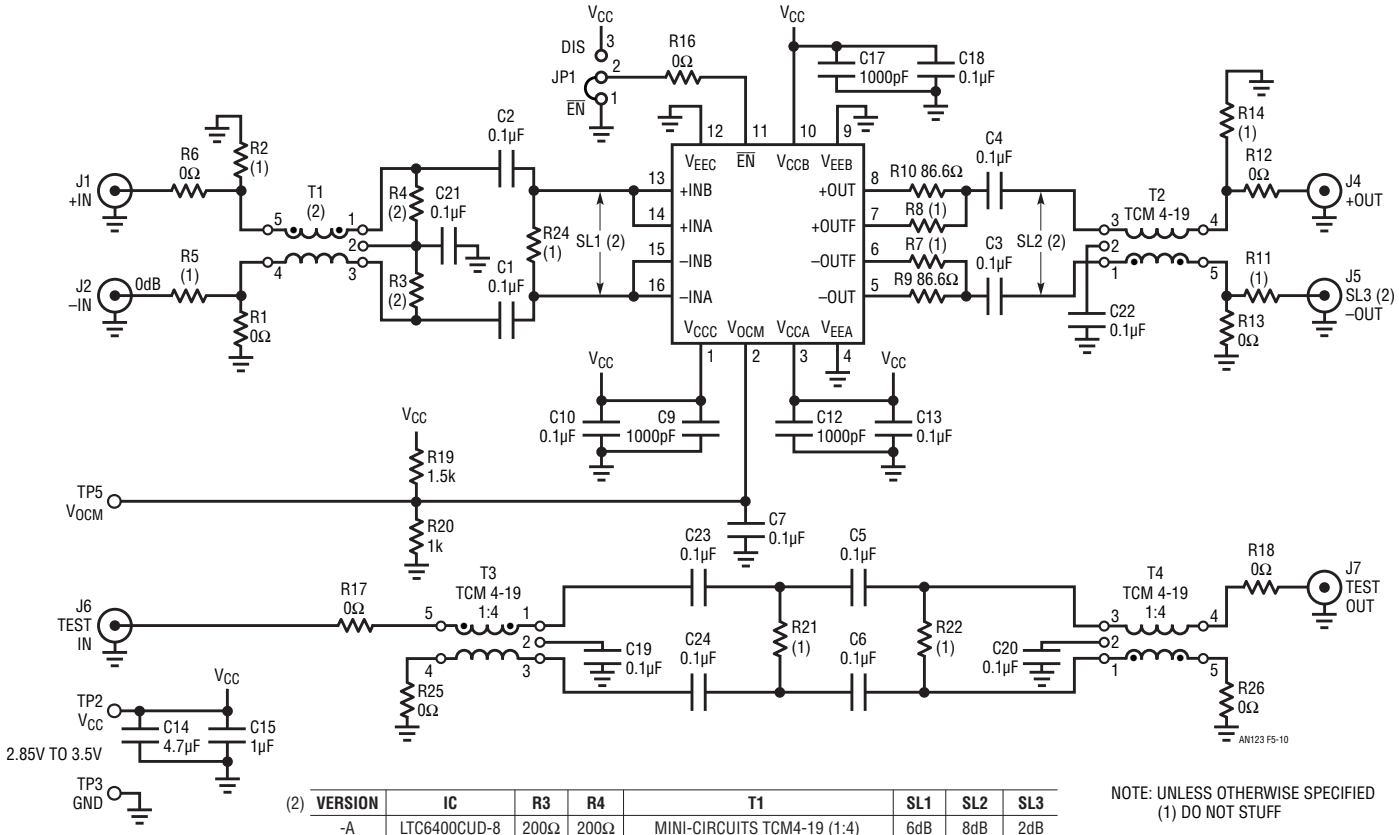


Figure 5-8. Input Reflection Coefficients (S11) of the LTC6400 Family from 10MHz to 1GHz. Below 100MHz or so, the Impedances are Almost Purely Resistive. Above that, the Reactances Must be Considered for Impedance Matching

5.5 Input Transformers

The LTC6400 works well with a variety of RF transformers at the input. Transformers are commonly used on LTC6400 demo boards as baluns and impedance-match elements for ease of evaluation. Figure 5-10 shows the schematic of the DC987B standard demo board of the LTC6400. At the input, a 4:1 wideband transmission-line transformer (TCM4-19+) is used for two purposes: to match a 50Ω signal source to the 200Ω input impedance of the IC, and also to convert the single-ended input signal into a differential signal for evaluation. The performance of the LTC6400 as a single-ended-to-differential converter is very good, but for even better performance it should be used with differential inputs.

At the output, another TCM4-19 transformer is used for converting the differential output to a single-ended output and impedance matching a 50Ω load (such as a network or spectrum analyzer). The load will see a 50Ω source impedance, and the amplifier sees a benign 400Ω load impedance. The LTC6400 is designed to drive higher impedance loads, and will not exhibit the same low distortion performance when driving heavy loads (e.g., 50Ω).



(2)

VERSION	IC	R3	R4	T1	SL1	SL2	SL3
-A	LTC6400CUD-8	200Ω	200Ω	MINI-CIRCUITS TCM4-19 (1:4)	6dB	8dB	2dB
-B	LTC6400CUD-14	OPEN	OPEN	MINI-CIRCUITS TCM4-19 (1:4)	6dB	14dB	8dB
-C	LTC6400CUD-20	OPEN	OPEN	MINI-CIRCUITS TCM4-19 (1:4)	6dB	20dB	14dB
-D	LTC6400CUD-26	OPEN	OPEN	MA-COM MABA-007159-000000 (1:1)	0dB	20dB	14dB
-E	LTC6401CUD-8	200Ω	200Ω	MINI-CIRCUITS TCM4-19 (1:4)	6dB	8dB	2dB
-F	LTC6401CUD-14	OPEN	OPEN	MINI-CIRCUITS TCM4-19 (1:4)	6dB	14dB	8dB
-G	LTC6401CUD-20	OPEN	OPEN	MINI-CIRCUITS TCM4-19 (1:4)	6dB	20dB	14dB
-H	LTC6401CUD-26	OPEN	OPEN	MA-COM MABA-007159-000000 (1:1)	0dB	20dB	14dB

SL = SIGNAL LEVEL (RELATIVE TO 0dB INPUT)

NOTE: UNLESS OTHERWISE SPECIFIED
(1) DO NOT STUFF

Figure 5-10. DC987B Demo Board Schematic. The Layout is Discussed in Section 8

For ADC-driving applications, the LTC6400's differential output will connect to the ADC input either directly or through a discrete filter, but typically will not require an output transformer. At the input of the LTC6400, it will still be desirable in many applications to use input transformers for impedance conversion and single-ended-to-differential conversion. In the case of the LTC6400-8, LTC6400-14 or LTC6400-20, the amplifiers have 200Ω or 400Ω input impedances. If the signal source has a 50Ω characteristic impedance, then the use of a 4:1 or 8:1 transformer for impedance matching has an important benefit. The transformers will provide some "free" voltage gain compared to other methods of impedance matching, such as a shunt resistor. Since a 4:1 impedance-ratio transformer has a 2:1 voltage gain, the input voltage of the LTC6400 is twice as large. This gain comes without any significant noise or power penalty, and in fact, the gain can actually improve the effective noise figure of the LTC6400 (as compared to using a shunt resistor for impedance matching). Although the LTC6400's voltage noise density does not change, the extra gain means that the input-referred voltage noise is reduced by the extra gain factor.

5.6 Resistor Termination

RF transformers are excellent in many impedance-matching situations, and they make convenient baluns for using the LTC6400 differentially. However, their frequency response lower limit is largely determined by the size of the transformer, and there is no hope of achieving consistent frequency response all the way down to DC. Resistors used for impedance matching do not have this limitation. Resistors can yield a much more broadband

impedance match than even the best RF transformers, and the frequency response of resistors extends down to DC. There is a penalty to pay in noise figure as compared to the transformer method, but using resistors also saves significant cost over transformers. Resistors can also be used to impedance match a single-ended input.

The circuit shown in Figure 5-11 uses a resistor to terminate a differential 50Ω input source. Since the system is fully differential, the input impedance of the amplifier by itself is calculated by adding the two input resistances together (in this case 400Ω). The shunt input resistor matches this impedance to 50Ω, from DC to high frequency. Note that the 400Ω low frequency input impedance is only true as long as the amplifier maintains its internal "virtual ground" node, and as the amplifier's loop gain decreases with frequency, the input impedance will also change. The LTC6400 data sheet contains graphs of input impedance versus frequency.

The two downsides of using a resistor for termination are power/signal attenuation and the resultant increase in noise figure (i.e., degradation in noise performance). For the same input power level, a 50Ω input impedance will result in less voltage swing than a 400Ω input impedance, thereby introducing an effective voltage attenuation. By using a transformer, the impedances are matched losslessly, and no attenuation occurs. Since the input noise power density of the LTC6400 remains the same and the input signal is smaller, the noise figure increases proportionally.

Figure 5-12 shows resistor termination used with a single-ended input source. Notice the extra resistor R_{T2}, which balances the source impedances seen by the two inputs. Balancing the input impedances is desirable because the distortion performance of the LTC6400 can be affected by imbalance in the source impedances. Also, the inequality of the feedback factors will also cause a portion of the LTC6400's common mode noise to become differential

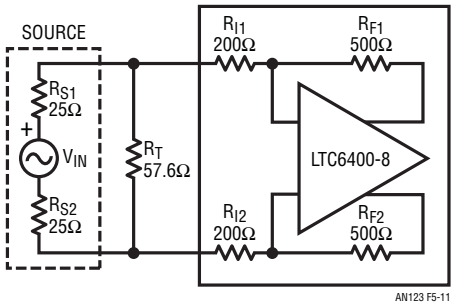


Figure 5-11. Resistor Termination with a Differential Input Source. A Single Shunt Resistor Transforms the 400Ω Input Impedance into a 50Ω Input Impedance. The Benefit of Resistor Termination is Wideband Performance, from DC to the Maximum Bandwidth of the Amplifier. The Drawback is Power Attenuation and the Resultant Increase in Noise Figure

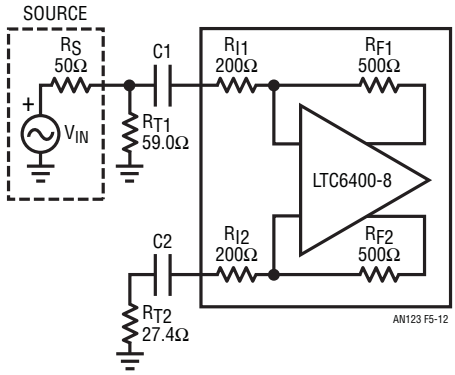


Figure 5-12. Single-Ended Input with Resistor Impedance Match and Balanced Input Impedances

mode noise. The best practice is to always balance the source impedances when working with single-ended inputs.

The addition of R_{T1} and R_{T2} creates additional terms that are not covered in Equation 5-3. The value of R_{T2} is simply the parallel impedance value of R_{T1} together with R_S (the source impedance). The new values of termination resistors can be calculated as shown:

$$R_{T1} = \frac{1}{2} R_S \bullet \frac{R_S R_F + 2R_S R_I + \sqrt{R_S{}^2 R_F{}^2 + 4R_F{}^2 R_I{}^2 + 8R_F R_I{}^3 + 4R_I{}^4}}{R_I{}^2 + R_F R_I - R_S{}^2} \quad (5\text{-}6)$$

$$R_{T2} = \frac{R_{T1} R_S}{R_{T1} + R_S} \quad (5\text{-}7)$$

In Equations 5-6 and 5-7, R_I and R_F are the values of the internal gain and feedback resistors, 200Ω and 500Ω respectively in Figure 5-12. Table 5-4 lists the values for R_{T1} and R_{T2} that apply in the case of a single-ended 50Ω input source (R_S = 50Ω), calculated using Equation 5-6 and Equation 5-7.

Table 5-4. Termination and Balancing Resistors Used to Match the LTC6400 Family to a 50Ω Single-Ended Input Source. The Resistance Values are Rounded to the Nearest 1% Standard Value

	TERMINATION RESISTOR (R_{T1})	BALANCING RESISTOR (R_{T2})
LTC640x-8	59.0Ω	27.4Ω
LTC640x-14	68.1Ω	28.7Ω
LTC640x-20	66.5Ω	28.7Ω
LTC640x-26	150Ω	37.4Ω

The extra source impedance added by R_S and R_{T1}/R_{T2} changes the feedback factor of the differential amplifier, and therefore alters the gain. The overall voltage gain from the ungrounded side of R_{T1} to the differential output can be calculated as follows:

$$\text{Gain} = \frac{2R_F\left(R_{T2}+R_F+R_I\right)}{2R_I^2+2R_I\left(R_F+R_{T2}\right)+R_FR_{T2}} \qquad (5\text{-}8)$$

6 DYNAMIC RANGE AND OUTPUT NETWORKS

The LTC6400 family is fundamentally a very high speed version of the traditional feedback differential amplifier. Therefore, the distortion performance can change dramatically with the choice of output load. The LTC6400 was optimized to drive a high impedance ADC load such as the switched-capacitor inputs of Linear Technology's high performance pipelined ADC families. It was not designed to directly drive a 50Ω load, a characteristic that distinguishes the LTC6400 from other high frequency amplifiers.

6.1 Resistive Loads

Figure 6-1 shows the distortion versus frequency of the LTC6400-20 with two resistive loads: open (no load) and 200Ω. The distortion with a 200Ω load is measurably higher (worse) than with no resistive load, although the performance is still reasonable. However, it is not recommended to use a 50Ω or 100Ω load with the LTC6400, because the distortion performance would be significantly degraded. Note that the HD2 changes very little with R_L changes; this is because the symmetry of the differential outputs tends to cancel even-order harmonics.

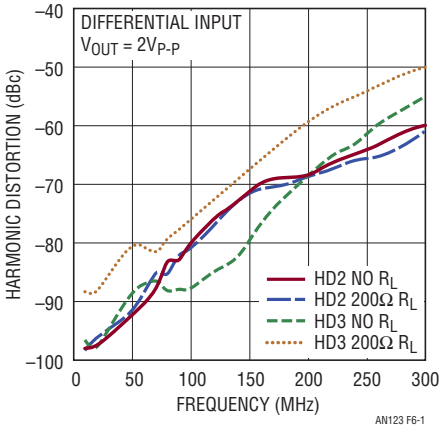


Figure 6-1. Harmonic Distortion Performance Versus Frequency of the LTC6400-20 with Two Different Resistive Loads. Loads of 200Ω or Greater are Recommended for Optimal Performance

Another important consideration is the output current of the LTC6400. Resistive loads from the outputs directly to ground or to the V^+ supply would cause the LTC6400 outputs to sink or source DC bias currents, which is unnecessary for operation and may impair performance.

6.2 V_{OCM} Requirements

The LTC6400 is designed for direct DC-coupled driving of Linear Technology's high speed ADCs. The existing families of 3V and 3.3V ADCs have an optimal input common mode DC bias of 1.25V to 1.5V. Therefore, the LTC6400 is optimized for this range of V_{OCM} voltages. Figure 6-2 shows the distortion performance while varying V_{OCM}. If an ADC requires a common mode bias outside of the optimal range for the LTC6400, the output of the LTC6400 can be AC-coupled with capacitors. The downside of this approach is the limited low frequency response.

The distortion performance of the LTC6400 family, like most amplifiers, is dependent on the input and output common mode voltage bias. Figure 6-2 shows the 2-tone 3rd order intermodulation distortion (IMD3) of the LTC6400 at 100MHz (with 1MHz tone spacing). The graphs demonstrate that there is an optimal range for both input and output common mode bias that provides the best overall distortion performance, and that the distortion performance is more dependent on the output common mode voltage (V_{OCM}) than on the input common mode voltage (V_{ICM}).

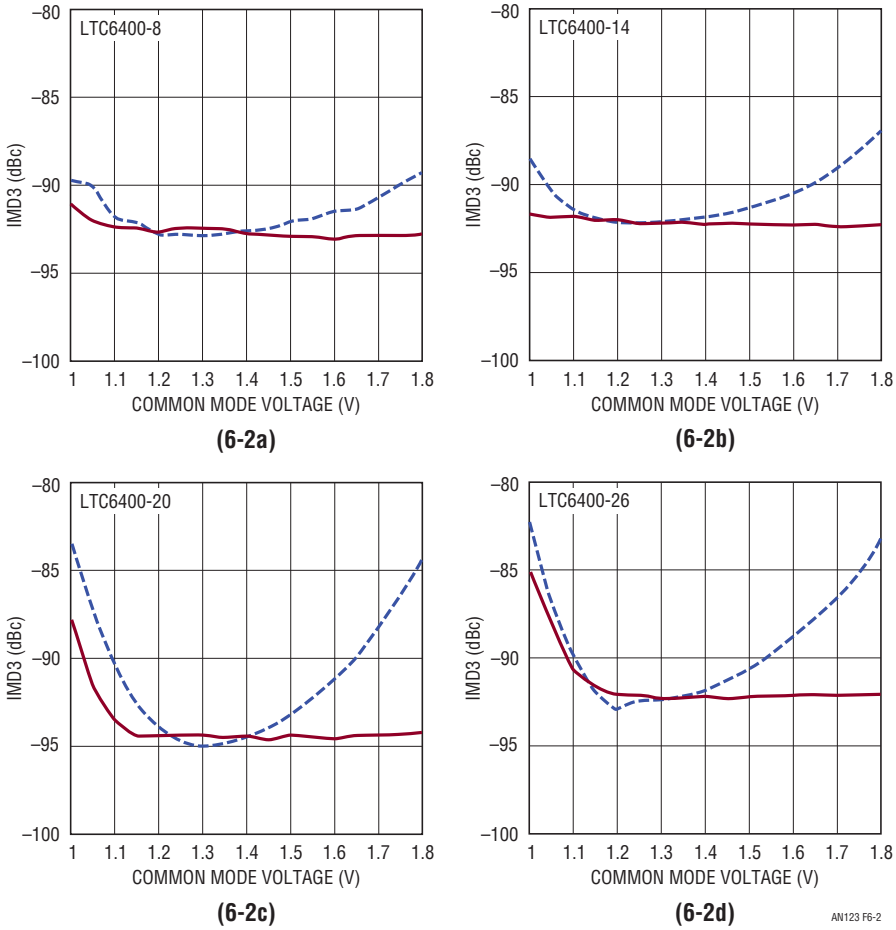


Figure 6-2. 2-Tone 3rd Order Intermodulation Distortion (IMD3) of the LTC6400 Family Versus Input and Output Common Mode Bias Voltages at 100MHz. Conditions: Differential Input, No R_{LOAD}, V_{OUT} = $2V_{P-P}$ Composite. The Solid Line Shows IMD3 Versus V_{ICM} with V_{OCM} = 1.25V. The Dashed Line Shows IMD3 Versus V_{OCM} with an AC-Coupled (Self-Biased) Input. The Distortion Performance Exhibits More Dependence on V_{OCM} than on V_{ICM}

6.3 Unfiltered and Filtered Outputs

The LTC6400 family includes two sets of parallel outputs for added flexibility in applications. The outputs are not independently buffered, and should not be considered as multiple outputs. In order to help ensure unconditional stability, the LTC6400's unfiltered (normal) outputs include 12.5Ω series resistors on the chip. These resistors must be accounted for in the calculation of voltage drop when driving a resistive load and when designing an antialias filter at the LTC6400 output. Additionally, there is approximately 1nH in bond-wire inductance leading from the series resistors to the package pin, which should not have a significant impact on LTC6400 circuits, but may be important for high order LC filter design.

The filtered outputs of the LTC6400 are designed to potentially save some space in the design of antialias filters. While the unfiltered outputs have 12.5Ω series resistors, the filtered outputs have 50Ω series resistors and 2.7pF of shunt capacitance (including package parasitic capacitance) to form a lowpass filter at the output of the LTC6400. This structure can be used as is or as part of an external antialias filter. By itself, the filter would limit the effective noise bandwidth to under 500MHz. This will prevent the LTC6400's full 1.8GHz noise bandwidth from aliasing and reducing the SNR of the system. When using high performance 14-bit or 16-bit ADCs, it may be necessary to limit the noise bandwidth further to prevent degradation of the ADC's SNR performance.

6.4 Output Filters and ADC Driving Networks

It is often desirable to design an output filter for the LTC6400, for antialias or selectivity purposes (or both). Lowpass and bandpass filters are both practical, and the desired bandwidth will usually be determined by the input signal and/or the Nyquist bandwidth of the ADC (half the sample rate). Since the LTC6400 is unconditionally stable with any output load, it is possible to design both RC and LC circuits for this purpose.

Driving a high speed 14-bit or 16-bit ADC that samples at 100 Megasamples per second (and above) is a challenging task. As discussed in section 3.3, the wide bandwidth of the LTC6400-20 means that the noise of the LTC6400-20 can dominate that of a low noise 14-bit or 16-bit ADC. This implies that the configuration shown in Figure 6-3, while highlighting the ease of use of the LTC6400-20, is not sufficient in SNR-critical applications. In order to take advantage of both the low distortion and the low noise of the 16-bit ADC, the noise bandwidth must be limited by a lowpass or bandpass filter.

An ideal drive network for driving a high performance, fast sampling ADC would have low noise, low distortion and low output impedance over frequency. This would allow the network to absorb the charge injection from the ADC's sampling switches and settle in time for the next sample. The frequency content of the charge injection extends out to beyond a GHz, due to the speed with which the sampling switches transition.

The LTC6400 by itself does have low output impedance and the ability to settle relatively quickly after a charge injection event. However, at sampling speeds well above 100Msps, the reduced time for settling may result in incomplete settling from charge injection impulses, which may lead to in increased distortion and noise sampled by the ADC. Fortunately, drive networks can be designed that help to absorb the charge and reduce the impact on the LTC6400. The most basic circuits to do this would be a 1-pole RC lowpass filter or a 2-pole RLC bandpass filter.

The lowpass filter shown in Figure 6-4 is the basic configuration. R_{O1} and R_{O2} represent the frequency dependent output impedance of the LTC6400. R3 and R4 help to absorb the sampling glitches from the ADC input, and are usually sized from 5Ω to 15Ω. The ADC charge injection is typically a common mode event, so C2 and C3 are the dominant charge "reservoirs" that help to absorb the sampling glitches, much like bypass capacitors on a power supply. C1 is a purely differential capacitor, and does not have much effect on the common mode charge injection.

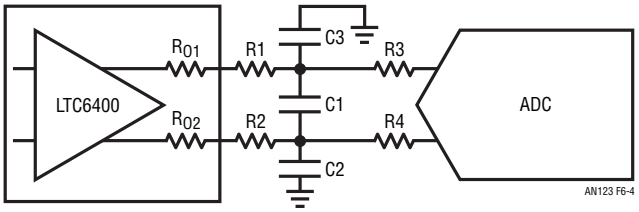


Figure 6-4. Simple RC Lowpass Filter ADC Drive Network

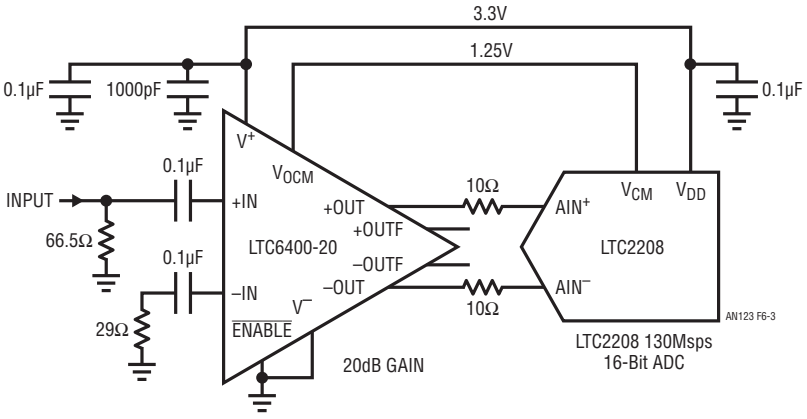


Figure 6-3: Example of Direct ADC Connection from the LTC6400-20 Data Sheet. This Figure Shows the Flexibility and Simplicity Possible in Interfacing the LTC6400 with a High Speed ADC, but Does Not Address the Issue of SNR and Band Limiting the Amplifier's Output. In Most Applications Where SNR is Critical, the Bandwidth of the LTC6400-20 Output Should be Limited by a Lowpass or Bandpass Filter

The size of R1 and R2 is not largely constrained, except for in the case of lower frequency cutoff filters. If the total resistance seen by the ADC is too high, the linearity of the ADC will typically suffer. This characteristic is different with different ADC families, and is difficult to generalize. At the other extreme, if the resistance R1 and R2 are too small then C1-C3 may be large, and the amplifier loses loop gain when presented with too large of a capacitive load. Overall an R1/R2 value between 10Ω and 100Ω will usually be a good starting point for the filter design.

A simple bandpass filter is shown in Figure 6-5 with the addition of L1. Many of the same considerations apply as for the RC lowpass network. The bandwidth of the bandpass filter is determined by the ratio of the inductance to the total parallel capacitance (C1-C3), as well as the values of R1 and R2. Increasing R1/R2 will make the bandwidth narrower and increase the insertion loss of the filter, so a smaller R1/R2 is desirable, as low as 0Ω. The only time when R1 and R2 may be desired is for improved distortion performance for input signal frequencies close to the passband edges of the filter. The impedance of an LC bandpass filter is at its maximum at the center frequency, but drops quickly in the transition to the stopband. If the bandwidth of the input signal extends out to the edges of the passband, the LTC6400 may be driving a low effective impedance, and the intermodulation distortion may be unacceptably high. In this case, it would be better to increase the bandwidth of the filter (by changing the L/C ratio) and also increase the values of R1/R2. This trades off some insertion loss in the filter for more consistent distortion performance across the passband.

The relationship of the RLC passband frequencies to the sample rate of the ADC is also important. If the ADC's sampling frequency or its harmonic multiples are within the passband of the RLC filter, the network will not attenuate the charge injection of the sampling inputs effectively. If the network resonates at the sampling charge injection frequencies, it will not settle completely between samples at higher sample rates.

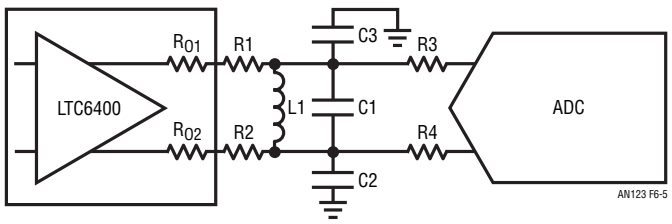


Figure 6-5. Simple RLC Bandpass Filter ADC Drive Network

An important design consideration is that feedback amplifiers such as op amps typically exhibit poor stability with large capacitive loads, and the LTC6400 is no exception. The phase shift and low impedance presented by a capacitive load, though partially isolated from the main feedback loop,[8] will result in greater gain peaking above 1GHz. Although the LTC6400 is designed to be unconditionally stable, the penalty for a capacitive load will show up as inferior distortion performance. When designing higher order LC filters as antialias filters after the LTC6400, they should ideally be designed to have a series inductor in the first section, or if a shunt capacitive section must be first, the capacitor should have as small of a value as possible. Figure 6-6 shows the difference in distortion performance when a differential capacitive load is presented to the LTC6400-20, and also the mitigating effect of some small series resistors prior to the load.

Note 8: See section 1.2 for further explanation of the LTC6400's internal feedback loop.

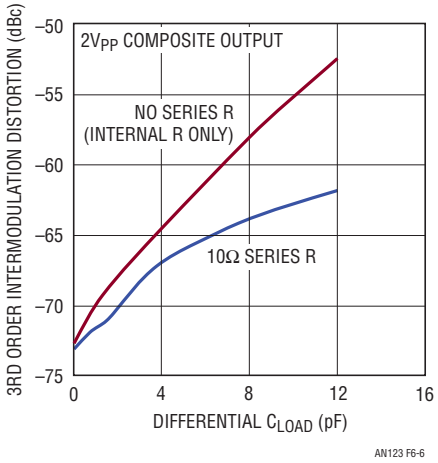


Figure 6-6. 3rd Order 2-Tone Intermodulation Distortion at 240MHz (1MHz Tone Separation) with a Differential Capacitive Load at the Unfiltered Outputs. The Degradation in Performance is Mitigated by an Additional Series Resistor at Each Output Prior to the Load

6.5 Output Recovery and Line Driving

Many feedback amplifiers have difficulty recovering from large input and/or output excursions, which limit their use in high crest factor systems where the output may occasionally be driven to saturation or clipping. In digital drivers and receivers, the output will almost always be at one or the other extreme, which makes the recovery time even more crucial. The LTC6400 family exhibits rapid recovery from an input or output overdrive condition, which enables it to be used in unconventional ways. Figure 6-7 shows a measurement of the LTC6400's propagation delay when used as a digital driver with the inputs and outputs overdriven. The LTC6400 is driving a total 200Ω load, which simulates a terminated 100Ω differential transmission line. The graph demonstrates that even with the inputs overdriven by 1V and the outputs fully clipped, the propagation delay remains less than 3ns. Figure 6-8 is a schematic of the circuit used to measure the data in Figure 6-7.

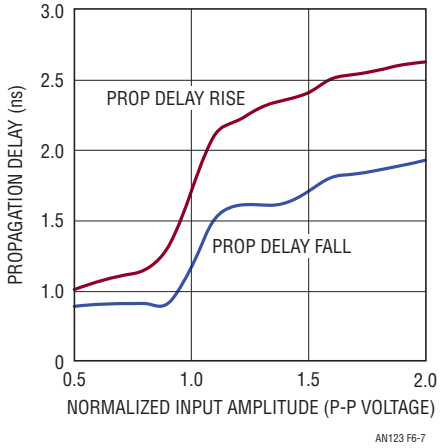


Figure 6-7. Propagation Delay for the LTC6400-20 with Varying Amounts of Input Overdrive. The X-Axis is the Input Pulse Amplitude (Peak-to-Peak), Normalized to the Pulse Amplitude that Causes Output Clipping. The Y-Axis is Propagation Delay in Nanoseconds, Measured from the 50% Transition of the Input to the 50% Transition of the Outputs

7 STABILITY

Stability poses a significant challenge in applications where wideband amplifiers operate at multi-GHz frequencies. Rigorous layout rules, specific feedback components and carefully chosen source/load terminations are often required to guarantee circuit stability. The LTC6400 achieves extraordinary robustness by optimizing the internal compensation networks and isolating sensitive nodes from external parasitic elements. It dramatically reduces the restrictions on user system design and board layout.

If we treat the LTC6400 as a 2-port network, Rollett's stability factor (K factor) can be used as a measurement of overall stability. A circuit is unconditionally stable if both the K-factor is greater than 1 and $|\Delta| < 1$, where (for a 2-port system):

$$K = \frac{1 - |S11|^2 - |S22|^2 + |\Delta|^2}{2|S12||S21|} \quad (7\text{-}1)$$

$$\Delta = S11 \bullet S22 - S12 \bullet S21 \quad (7\text{-}2)$$

Figure 7-1 shows a measurement of the K factor over frequency for LTC6400 (all four gain options), which is based on measured 4-port S parameters. Note that the LTC6400 includes two feedback loops: one for normal differential signals and one to stabilize the common mode bias and reject common mode input signals. Both the differential mode and common mode loops need to be stable to avoid oscillations, and therefore both are presented in Figure 7-1 and Figure 7-2. The requirements of $K > 1$ and $|\Delta| < 1$ are both met by each member of the LTC6400 family.

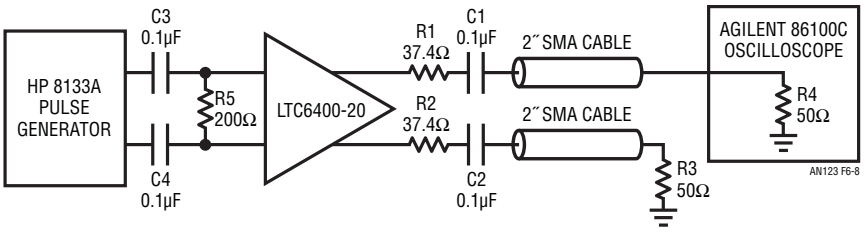
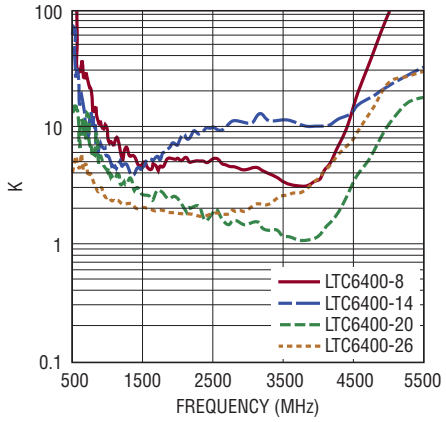


Figure 6-8. Circuit Used to Measure the Propagation Delay of the LTC6400-20. The Amplifier Receives a Differential Input from the HP 8133A Pulse Generator, and its Output is Measured by an Agilent 86100C Sampling Oscilloscope. The Inputs and Outputs are Impedance Matched with Series or Shunt Resistors for Minimum Line Reflections. The Circuit was Built on the LTC6400-20 Demo Board, DC987B-C.

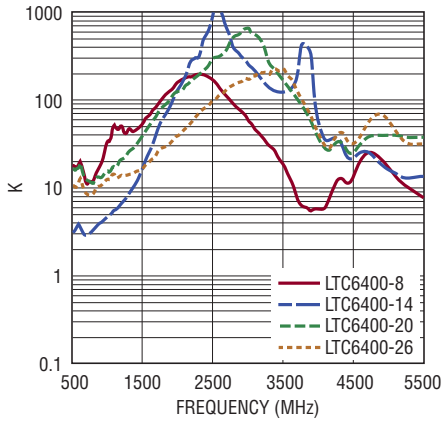
7.1 Limitations of Stability Analysis

The measurements for Figure 7-1 and Figure 7-2 were made at room temperature on a calibrated network analyzer using a PCB with good high frequency layout. As Equations 7-1 and 7-2 show, the stability factors K and Δ are calculated from the 2-port S-parameters of the LTC6400, which can be affected by various factors like temperature, bias, and layout. Similar experiments have shown that the LTC6400 family remains stable over temperature and bias conditions, but care must still be taken in layout to ensure good performance. The sensitivity of LTC6400 stability to various layout issues is difficult to quantify, but various best practices have been identified through experience. See the Layout section for more information and recommendations.

Another limitation of this stability calculation method is that the S-parameters are made with symmetrical inputs and outputs. Due to the fact that the LTC6400 is a fully differential amplifier, there are actually four ports to analyze; for the sake of our analysis, we simplify the model down to two independent 2-port networks. In extreme cases of input and output asymmetry, for example, due to layout and/or differences in termination, the differential mode and common mode loops of the amplifier will interact, creating a "mixed mode" situation. If a situation arises where the LTC6400 will be used in this manner, this stability analysis may not apply. In order to ensure unconditional stability in this new mode, the K and Δ analysis should be repeated under the new conditions.

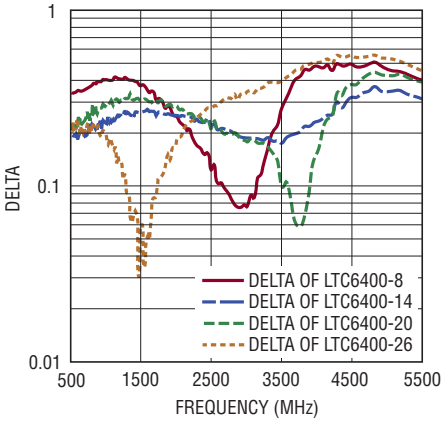


(7-1a)

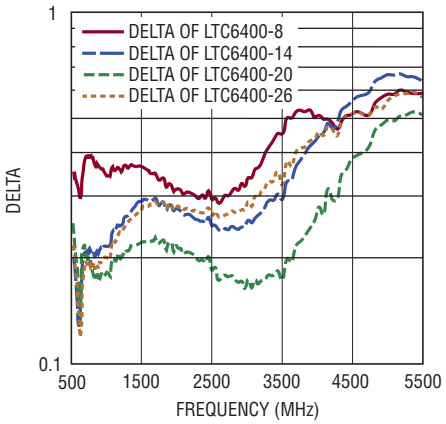


(7-1b)

Figure 7-1. Rollett's Stability Factor (K factor) for the LTC6400 Family of Amplifiers. The K Factor is a Measure of Overall Stability of an Amplifier. (7-1a) is the Differential K factor, and (7-1b) is the K Factor for the Amplifier's Common Mode Loop. A K Factor Value of Greater than 1 at All Relevant Frequencies Implies that the Amplifier is Unconditionally Stable with Any Input or Output Termination



(7-2a)



(7-2b)

Figure 7-2. Delta Calculation for the LTC6400 Family's (7-2a) Differential Mode Loop and (7-2b) Common Mode Loop. Delta is a Part of the Rollett's Stability Factor Calculation. A Delta of Less than 1 (Absolute Value) is Part of the Requirement for an Unconditionally Stable System

8 LAYOUT CONSIDERATIONS

The LTC6400 is a high speed fully differential amplifier with almost 2GHz of small-signal bandwidth. This means that as far as the printed circuit board (PCB) is concerned, the LTC6400 family requires the same care in layout design as do sensitive radio frequency (RF) circuits. Poor layout can and will lead to increased distortion, gain and noise peaking, unpredictable signal integrity issues, and in the extreme case, oscillation. Fortunately, the LTC6400 has some features that help to simplify the design of the PCB layout.

First, the resistors for setting the voltage gain are inside the IC, which makes the LTC6400 a "fixed gain" amplifier. Looking at the block diagram, reproduced in Figure 8-1, the critical feedback loop of the amplifier is contained within the chip and is not made available to the user. Traditionally, this is one of the areas where the layout is most critical, and mistakes are most common. Even a very small amount of capacitance at the feedback nodes would significantly affect the frequency response and stability of the amplifier. By keeping the resistors internal, bond-wire inductance and parasitic reactance on the board will not impair the frequency response of the IC as much as it would if the resistors were external.

Second, the LTC6400 has a "flow-through" pinout that is designed for ease of layout. The inputs and outputs are

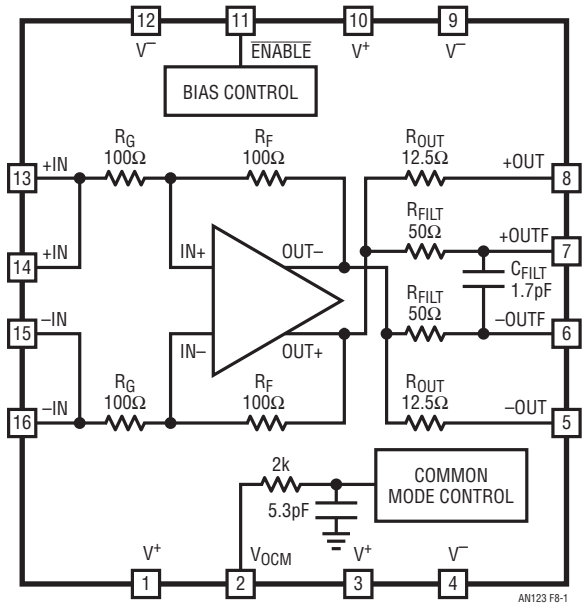


Figure 8-1: Block Diagram of the LTC6400-20

located on opposite sides of the chip, and the power and control pins are located on the remaining two sides. This makes the inputs and outputs easy to route on the board, without the need to route anything around the chip or on internal layers.

One critical aspect of every high speed amplifier layout is the location of the bypass capacitors. The current path from the amplifier's supply pins through the capacitors to the board return and back to the amplifier is critical, because excess inductance or resistance in this path will cause voltage bounce. On the LTC6400, the V^+ and V^- pins are strategically located to allow the customer to place the bypass capacitance in close proximity to the chip, because these components will not hinder the layout of the signal path. Additionally, the LTC6400 family includes approximately 150pF of bypass capacitance on-chip, which makes the layout of the bypass capacitance slightly easier. The external bypass capacitors simply act as a charge reservoir for the on-chip bypass capacitance. Bypass capacitors of 0.1µF are the recommended value to do the job, and are currently available in the 0402 size or smaller.

Note the RC lowpass filter at the input of the V_{OCM} pin, Pin 2 in Figure 8-1. This internal filter makes the layout of the recommended V_{OCM} bypass capacitor less critical. The internal common mode control loop has a bandwidth of over 300MHz, but the V_{OCM} pin itself is much less sensitive to high frequency interference due to this 15MHz lowpass filter. The V_{OCM} bypass capacitor can be located further away from the chip to make room for the more critical V^+ bypass capacitors.

Figure 8-2 shows the layout of the LTC6400 demo board, DC987B. The differential inputs are on the left, and the differential outputs on the right. Users can select either the filtered or unfiltered outputs by changing the resistors on the board. Notice the bypass capacitor groups on the top and bottom sides of the LTC6400—they are located as close as possible with ground vias near the capacitors so that the overall current loop through the capacitors is minimized. Also, the Exposed Pad of the LTC6400 is connected directly to a solid ground with four ground vias, which provides a good thermal and electrical path to board ground.

There are three V^+ (positive voltage supply) pins on the LTC6400, and each of them has its own set of bypass

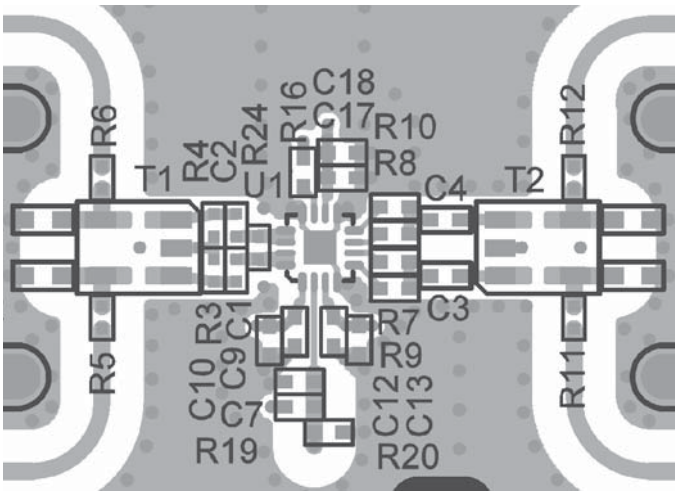


Figure 8-2. DC987B Demo Board Layout, Layer 1. The Schematic is Shown in Figure 5-10

capacitors, as recommended in the product data sheet. There is a small capacitor, typically around 1000pF, located close to the part. Located further away is a larger (0.1µF to 1.0µF) bypass capacitor. There are also three V^- (negative power supply) pins, which are normally connected to board ground and to the Exposed Pad. It's important that the V^+ pins all be connected to the exact same supply, and that the V^- pins and Exposed Pad are all connected together and tied to board ground.

8.1 Thermal Layout Considerations

The LTC6400 dissipates 250mW and the LTC6401 dissipates 130mW, so thermal issues are not as prevalent as with higher power devices; however, if the part is being operated in a high temperature environment, good thermal layout can protect the silicon from overheating. Good thermal layout consists of providing a square of copper on the board to mount the Exposed Pad, and using four vias underneath the Exposed Pad to help conduct heat to the PCB. The inner ground layers of the LTC6400 (layer 2 should be ground, for best high frequency performance) should have as much unbroken ground plane as possible in the vicinity of the IC, because ground plane copper conducts heat much more efficiently than standard PCB dielectric materials.

8.2 Operating with a Negative Voltage Supply

In certain situations, it may be desirable to operate the LTC6400 with a V^- supply that is not the board ground. For example, if operating the LTC6400 with dual ±1.5V supplies, the inputs and outputs can operate at board ground without AC coupling. As long as the V^- pins and Exposed Pad are tied together to the same potential and the absolute voltage from V^+ to V^- does not exceed the data sheet maximum, there is no fundamental problem with this configuration. From a layout point of view, however, it presents a greater challenge to achieve optimal performance.

Besides bypassing the V^+ pins to board ground, it is also necessary to bypass the V^- pins to board ground (or bypass V^+ to V^-). The first step is to squeeze bypass capacitors for V^- onto the top layer in Figure 8-2. There isn't a lot of room for additional capacitors on the topside; however, the close proximity of the V^+ and V^- pins allows for the placement of bypass capacitors directly from V^+ to V^-. This makes for the shortest possible current path, and the use of small-valued 0201 or 0402-sized capacitors (on the order of 1000pF) can serve this function effectively in the layout. In fact, some of the V^+/GND bypass capacitors can be changed to V^+/V^- bypass capacitors without sacrificing performance. Larger-valued bypass capacitors for V^- can be located on the back side of the PCB. Since the LTC6400 layout does not normally require many components on the back of the PCB, there may be ample space to place four or more bypass capacitors around the perimeter of the LTC6400's Exposed Pad area. Figure 8-3 shows a sample top and bottom layout with dual voltage supplies.

Also of concern is thermal layout when the exposed pad is not tied to ground. Ideally, there would be significant V^- copper on one of the internal layers to help spread the heat generated by the part. With the V^- disconnected from board ground, the thermal resistance presented by the PCB will likely be much larger, and even the 250mW dissipated by the LTC6400 may start to present thermal issues at high temperature operation.

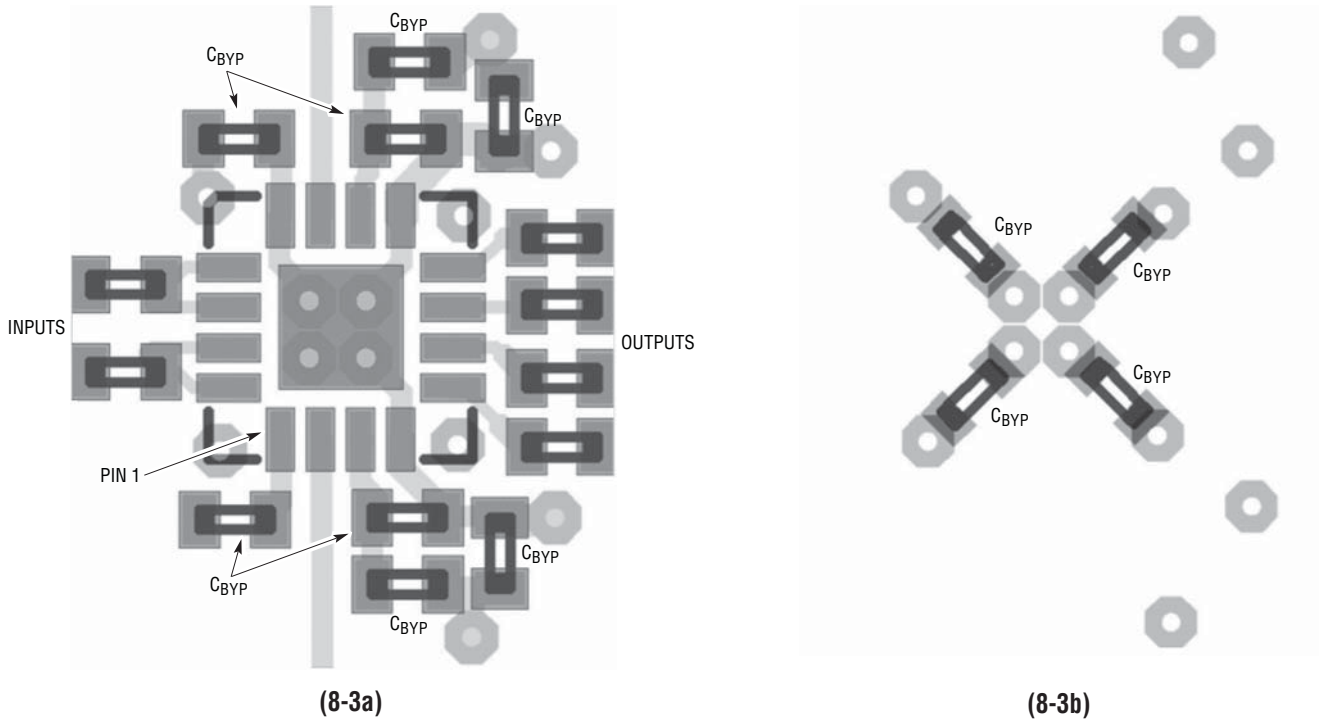


Figure 8-3. Sample Top Layer (8-3a) and Bottom Layer (8-3b) Layout with Dual Voltage Supplies. All Power Supply Bypass Capacitors are Labeled as C_{BYP}

9 CONCLUSION

The LTC6400 takes advantage of a very high speed semiconductor manufacturing process to achieve all of the characteristics necessary for high speed ADC driving, including low distortion, low noise and several gain options up to 26dB. In addition, the LTC6400 includes various ease-of-use features designed to assist in layout and manufacturing: unconditional stability with any input and output terminations, a flow-through layout, and internal resistors to reduce the sensitivity of the layout to parasitic elements.

10 APPENDIX A: TERMS AND DEFINITIONS

This section details some of the more commonly used (and/or misunderstood) terms in the specification and application of the LTC6400 family.

10.1 Noise Figure (NF)

Noise figure (NF) and noise factor (F) are ratiometric calculations that are useful in RF system design. The fundamental idea is that in an electronic system at a given temperature, there is a certain amount of noise due to random thermal motion. This noise is constant for a given system impedance and comes out to –174 dBm/Hz at room temperature. Whenever an amplifier or any other active element is placed into a system, there is an additional noise power added above and beyond the thermal noise floor. Noise factor is defined as the ratio between the input signal noise ratio (SNR) and output signal noise ratio,[10] or in other words the SNR with the additional amplifier and the SNR without it. Noise figure is simply noise factor in decibels:

$$NF = 10\log\frac{SNR_{IN}}{SNR_{OUT}} = 10\log F \qquad (10\text{-}1)$$

The concept behind NF is to quantify the amount of additive noise introduced when adding a device to the system. Note that the input SNR only counts the noise contribution

Note 10: A discussion of noise figure analysis can be found in (Gilmore and Besser 2003).

from the resistive part of the source impedance Z_S, as ideal capacitors and inductors are noiseless. So substituting R_S for the more general Z_S, we define noise figure as:[11]

$$NF = 10\log\frac{e_{n(OUT)}^2}{e_{n(Z_S)}^2 \bullet G^2} \quad (10\text{-}2)$$

where $e_{n(Z_S)}$ is the thermal noise of source resistance and G is the voltage gain of the amplifier for given Z_S.

$$e_{n(Z_S)}^2 = 4kTR_S \quad (10\text{-}3)$$

where k is the Boltzmann constant ($1.3806503 \bullet 10^{-23}$ J/K)

For a fixed-impedance system, such as RF systems that operate in 50Ω, using NF is a simple way to compare the noise performance of devices and calculate how the noise of a new device will affect the system-level noise performance. For voltage measurement systems like an ADC, NF is not always as convenient because the denominator of the ratio changes with impedance. This means that the relatively constant voltage noise density of the ADC will result in a different NF for different source impedances. The amplifier inputs of the LTC6400, as another example, have varying impedances from 50Ω to 400Ω, and the outputs may be driving the ADC's high impedance input. So to make system-level noise calculations may require some conversion of noise terms, from the voltage noise density ($V/\sqrt{Hz}$) specified in the data sheets to an 'equivalent' noise figure that is consistent throughout the system.[12] When comparing two similar ADC drivers, it is often easier to compare them in their "native" noise specification, which is voltage noise density.

10.2 3rd Order Intercept Point (IP3)

Signal distortion is present in all amplifiers to some extent, and in many amplifier data sheets it will be specified as a harmonic distortion. If a single sine wave tone is generated at the amplifier's output, there will also be a certain amount of unwanted distortion at all multiples of the sine wave frequency. The dominant tones will be the second and 3rd order harmonics. There is also another method of characterizing the 3rd order distortion, which is more useful for narrow-band systems: if two sine waves are generated at the output, spaced closely together in frequency, there will be additional spurious tones generated at the same spacing distance on either side of the two tones. The two closest tones are the 3rd order intermodulation distortion (IMD), and they are due to the mixing that occurs from the amplifier's nonlinearity.

The 3rd order intercept point (IP3) is a useful metric for measuring IMD performance in an amplifier. At a given frequency, set of bias conditions and temperature, the IP3 approximately defines the distortion performance at any power level where the amplifier's output is not saturated (Sayre 2001). IP3 can be referred either to the output (OIP3) or the input (IIP3, output IP3 minus the conversion gain). If you plot the output power versus the input power of an amplifier and overlay the 3rd order intermodulation distortion (IMD) curve versus input power on the same graph, as in Figure 10-1, the extrapolated curves would meet at the IP3 point. IP3 is typically specified in dBm, which is a logarithmic decibel unit referred to 1mW of power.

In order to apply the output IP3 metric to a voltage feedback amplifier like the LTC6400, it is necessary to define some specialized terminology. Because the LTC6400 is not designed to drive a resistive load of 50Ω, it is not appropriate to define input and output power in the standard way. The LTC6400 amplifies voltage, not power; the current gain through the device is typically very small. When driving a high speed ADC, the LTC6400 may not have a resistive

Note 11: An example of calculating of noise figure for amplifiers can be found in Section 11 or (National Semiconductor 1974).
Note 12: See (Pei 2008) for an example calculation of equivalent NF.

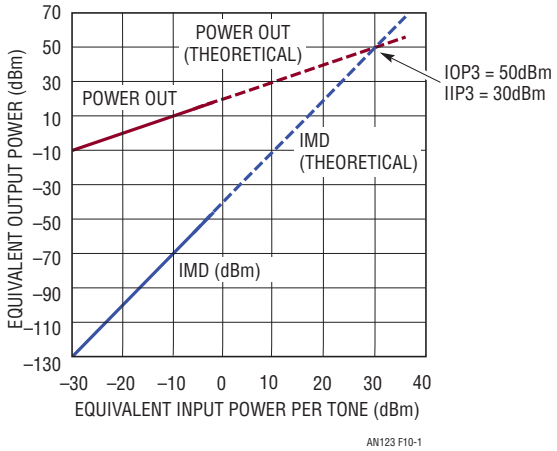


Figure 10-1: Graphically Showing the Equivalent 3rd Order Intercept Point (IP3) for a 20dB Gain Amplifier. The Plotted Curves of Output Power (dBm) and 3rd Order Intermodulation Distortion Power (dBm) Theoretically Meet at a Certain Output Power Which is Termed the IP3. This Power Level is Unattainable in Practice Because the Output of the Amplifier Saturates at Lower Power Levels

load at all. This leads us to define an *equivalent output power* level, which uses the voltage-swing equivalence into a non-existent 50Ω load. For example, a $1V_{P-P}$ voltage swing into 50Ω would equal 4dBm of RMS output power,[13] so we define $1V_{P-P}$ as 4dBm for the purposes of calculating the OIP3. This allows the LTC6400 to be used in the same signal-chain calculations as other devices, since OIP3 (like NF) can be used for cascaded system-level distortion analysis.

Using this equivalent power terminology, refer back to Figure 10-1 which shows the theoretical IMD and output power levels for a 20dB amplifier with a 50dBm OIP3 point, matching the typical specification of the LTC6400-20 at 100MHz. Extrapolating the IMD curve back to a 4dBm equivalent power level, which is defined as $1V_{P-P}$ ($2V_{P-P}$ with both tones together), that the IMD level is shown to be –88dBm, or –92dBc.[14]

10.3 1dB Compression Point (P1dB)

Strictly speaking, the "1dB compression point" of an amplifier is the input power level that causes the gain to deviate by 1dB from the ideal linear gain (Sayre 2001). This textbook definition does not include any restrictions on what type of amplifier or the root cause of the gain non-ideality. For an RF gain block, mixer or other "typical RF device" with a 50Ω impedance, the dominant source of this gain compression at high output power levels is the saturation of the output transistor. This "soft saturation" characteristic causes the gain to roll off as the signal swing of the output limits its ability to produce an ever-increasing output power. Consequently, the distortion of the output signal is also increasing in a predictable way as the input power increases. So in some cases, the P1dB of an RF device has a direct relationship with the 3rd order intercept (IP3) of that device, in which case the P1dB can be used to compare one device with another.

This situation does not apply to the LTC6400 family of amplifiers. Due to the large amount of feedback employed in the amplifier topology, the linearity of the LTC6400 (i.e., the amount of distortion) does not follow exactly the same trend as for an RF device. The feedback and loop gain of the LTC6400 circuit linearizes the amplifier's output, and the gain does not significantly deviate from the ideal value until the amplifier's output is actually saturated. So the signal out versus signal in of the LTC6400 exhibits much higher linearity until the output is up against the limit, at which point the distortion increases dramatically. Knowing the P1dB point of the LTC6400 does not give any inferred knowledge of the distortion performance or IP3.

11 APPENDIX B: SAMPLE NOISE CALCULATIONS

Calculating noise and noise figure for the LTC6400 family is challenging, and there is no one data sheet specification that can completely characterize the noise performance of this family. Due to the gain and feedback resistors being included inside the package, the noise of the amplifier in one configuration (e.g., with the inputs shorted together) will yield different results than with the inputs terminated resistively. This section walks through a few noise calculations in a further attempt to shed light on this topic.

11.1 Noise Analysis For Arbitrary Source Resistance

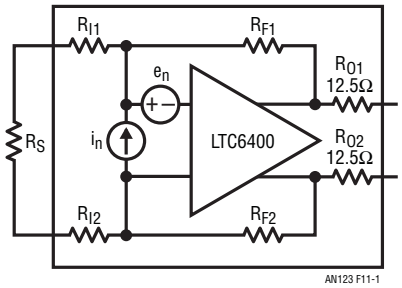


Figure 11-1: Schematic Drawing for Noise Analysis with an Arbitrary Source Resistance R_S. This Analysis Ignores the Noise of the Output 12.5Ω Resistors

Using the noise parameters found in Table 3-1, the differential output noise of the LTC6400 can be calculated for the most generic case, when the gain option and the source resistance are unknown. It is assumed that the source impedance is purely resistive for this exercise.

Note 13: In 2-tone tests, if each tone has $1V_{P-P}$ amplitude, then the combination of the two will produce a $2V_{P-P}$ composite amplitude, which is the standard amplitude for evaluating the LTC6400.

Note 14: dBc means "decibels referred to the carrier," and uses the carrier's power level as the 0dB reference. In this case, the distortion levels are measured relative to the power level of a single tone in the 2-tone test:
–92dBc = –88dBm – 4dBm

$$V_{N(OUT)} = \sqrt{\left[e_n \bullet \left(\frac{1+2R_F}{2R_I+R_S}\right)\right]^2 + \left(2R_F \bullet i_n\right)^2 + \beta \bullet \left(2R_I+R_S\right) \bullet \left(\frac{2R_F}{2R_I+R_S}\right)^2 + \beta \bullet 2R_F} \left(nV/\sqrt{Hz}\right) \quad (11\text{-}1)$$

where:

$\beta = 4kT = 1.6008 \bullet 10^{-20}$ (J), $R_F = R_{F1} = R_{F2}$ (Ω), $R_I = R_{I1} = R_{I2}$ (Ω)

The first term in the equation multiplies the input-referred voltage noise density of the LTC6400's internal amplifier with the noise gain. The second term is the noise gain of the input-referred current noise, which is equal to the feedback resistance. The third term deals with the noise of the input and source resistance, which is multiplied by the signal gain of the amplifier. The fourth term is the feedback resistance noise, which has a unity-gain factor.

To use a numeric example, examine the configuration of Figure 4-3, which shows the LTC6400-8 with extra source resistance to lower the effective voltage gain. The terms in the noise equation are: $R_F = 500\Omega$, $R_I = 280\Omega$, $R_S = 602\Omega$. Equation 11-1 and the values in Table 3-1 are used to calculate the estimated output noise at 100MHz (Equation 11-2).

The result in Equation 11-2 matches well with the curve in Figure 3-3. To convert this result to an equivalent noise figure, we refer back to Equation 10-2, with the assumption that the 602Ω resistors are the source resistance, with a voltage noise of $\sqrt{X_N} \bullet 602$ nV/$\sqrt{Hz}$:

$$NF = 10\log\frac{\left(7.3 \bullet 10^{-9}\right)^2}{\left(\beta \bullet 602\right) \bullet 1^2} = 7.4dB \quad (11\text{-}3)$$

The resultant NF matches well with the curve in Figure 3-4. The gain used in the above equation is the signal gain of the LTC6400-8 circuit, which was reduced to 1V/V by the series resistors.

$$V_{N(OUT)} = \sqrt{\left(1.12 \bullet 2\right)^2 + \left[1000 \bullet \left(4.00 \bullet 10^{-3}\right)\right]^2 + \beta \bullet 1000 \bullet 1^2 + \beta \bullet 1000} = 7.3nV/\sqrt{Hz} \quad (11\text{-}2)$$

11.2 DC987B Demo Board Noise Analysis

This section extends the noise calculations to the LTC6400 demo board, DC987B. A good example is the LTC6400-20, which has 200Ω differential input impedance and 1k feedback resistors. Figure 11-2 contains a noise representation of the board. The transmission line transformers (used mainly for impedance matching) are modeled here as ideal 1:4 impedance transformers together with a –1dB block. This allows the separation of the insertion loss of the transformer from its ideal behavior.

To calculate the noise figure of this system, calculate the noise in the chain for two situations: a noiseless LTC6400-20, which simply amounts to a noiseless gain block, and the real LTC6400-20. That way, the signal gain throughout the chain remains the same, and the difference in the noise will reveal the ratio of the signal-to-noise ratios in these two situations, which is by definition the noise figure. Table 11-1 shows the step-by-step noise calculations that match the locations shown in Figure 11-2.

Use Equation 10-2 to calculate the overall NF from these two cases:

$$NF = 10\log\left(\frac{3.61^2}{1.78^2}\right) = 6.14dB \quad (11\text{-}4)$$

This is the overall noise figure for the demo board DC987B.[15] However, there is still the –1dB loss from the transformer at the input of the LTC6400. For this, use the Friis formula (Friis 1944):

$$F_{TOT} = F1 + \frac{F2-1}{G1} \quad (11\text{-}5)$$

To apply the formula, translate the decibel NFs back to the linear noise factor (F). In our case, 6.14dB becomes 4.113, –1dB loss becomes 0.7943, and 1dB noise figure becomes 1.259 (the NF of an attenuator is just the inverse of the attenuation).

$$F_{TOTAL} = F_{LOSS} + \frac{F_{AMP} - 1}{G_{LOSS}} \quad (11\text{-}6)$$

$$4.113 = 1.259 + \frac{F_{AMP} - 1}{0.7943} \quad (11\text{-}7)$$

$$F_{AMP} = 3.267 \quad (11\text{-}8)$$

$$NF_{AMP} = 10\log(F_{AMP}) = 5.14dB \quad (11\text{-}9)$$

This new calculation subtracts out the effect of the attenuation from the input of the LTC6400, which will give us the true amplifier noise figure. Note that this result is consistent with the data in Figure 3-4.

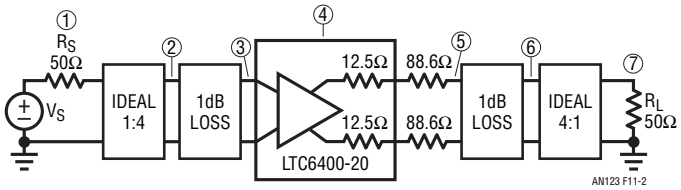


Figure 11-2. Equivalent Demo Board Schematic for Noise Analysis. This View Ignores the DC-Blocking Capacitors and Bypass Capacitors of the LTC6400, Which are Inconsequential to the Noise Analysis. The 88.6Ω Resistor at the LTC6400 Output Creates an Approximate 100Ω Source Resistance (or a Differential 200Ω), Which is an Impedance Match for the Reflected R_L

11.3 SNR Calculation and Aliasing Example

This example attempts to shed light on the tradeoffs between amplifier bandwidth and SNR, including the effects of ADC aliasing. Table 11-2 lists the important specifications for this example, for both the amplifier and the ADC.

Table 11-2. Specifications for SNR Calculation Example

Amplifier Specifications	Output Noise Density	8nV/√Hz
	Effective Noise BW	100MHz
ADC Specifications	Signal-to-Noise Ratio	80dB
	Effective Resolution	(80dB – 1.76)/6.02 = 13 bits
	Sample Rate	100Msps
	Input Span Voltage	$2V_{P-P}$ ($0.707V_{RMS}$ Sine Wave)

The first step is to calculate the noise floor of the ADC. Since the ADC samples at 100Msps, its noise can be represented as a constant noise floor extending from DC-50MHz, which is the Nyquist bandwidth. The industry standard for ADC specification is to list SNR with a full-scale sine wave tone. Using the maximum input sine wave amplitude of $0.707V_{RMS}$, and the 80dB SNR, calculate the ADC's intrinsic noise floor:

Note 15: This value approximates the value of NF published in the LTC6400-20 data sheet. To avoid confusion, the measured demo board NF values were used instead of the true amplifier NF value, as calculated in Equation 11-9.

Table 11-1. Noise Calculations for the DC987B Demo Board, According to Figure 11-2. The First Column Corresponds to the Numbered Locations in the Figure. The Second Column Assumes a Noiseless LTC6400-20, and the Third Column Includes the Noise of the LTC6400-20. The End Values of the Two Columns are Compared to Calculate the Noise Figure of the LTC6400-20

LOCATION (Fig 11-2)	NOISE WITH NOISELESS LTC6400-20 (nV/√Hz)	NOISE WITH ACTUAL LTC6400-20 (nV/√Hz)	COMMENT/DESCRIPTION
1	0.894	N/A	Noise of Source Resistance at 290K (17°C)
2	0.894	N/A	The 1:4 Transformer Results in a Voltage Doubling, but the Resistive Divider Formed by 200Ω Input Impedance Results in the Voltage Being Halved Again
3	0.80	N/A	After Subtracting the 1dB Loss
4	8.0	16.2	After Gain of 20dB, or 10V/V. For the Noisy Case, Look to Figure 3-3 for the Total Output Noise of the LTC6400-20 with a 200Ω Source Resistance, Which Matches the Situation in Figure 11-2. The Noise Output in the Figure Includes the Source Resistance Noise, Which is Reduced by the 1dB Loss in the Transformer
5	4.0	8.1	Reflected R_L Across Transformer is 200Ω, Which Creates a 1:1 Voltage Divider with the Resistors at the LTC6400 Output. For the Sake of Calculations, Treat This Resistance as 200Ω Instead of 101.1Ω
6	3.57	7.22	Subtracting Another 1dB Loss
7	1.78	3.61	Total Noise at Load (Ignoring R_L Noise). Transformer Reflects Voltage as 2:1, so the Voltage is Halved

$$SNR_{LIN} = 10^{80/20} = 10{,}000 \quad (11\text{-}10)$$

$$NOISE_{ADC} = \frac{0.707V}{10{,}000} = 70.7\mu V_{RMS} \quad (11\text{-}11)$$

$$e_{n(ADC)} = \frac{70.7\mu V}{\sqrt{50MHz}} = 10nV/\sqrt{Hz} \quad (11\text{-}12)$$

The next step is to look at the amplifier's contribution to the overall noise. Since the amplifier's total noise bandwidth is wider than the Nyquist bandwidth of the ADC, then aliasing will occur. See Figure 11-3 for a visualization of what happens when the ADC samples the amplifier's noise. The ADC has its own noise floor (flat from DC-Nyquist), and the amplifier has flat wideband noise from DC-f_{SAMPLE}, which is two full Nyquist bandwidths. Since the amplifier noise is uncorrelated with the ADC noise, both bands of amplifier noise can be added in an RMS fashion to the ADC's noise floor.

Adding the ADC's $10nV/\sqrt{Hz}$ to the amplifier's $8nV/\sqrt{Hz}$ (twice due to the aliasing), we arrive at the final noise floor of the combined circuit:

$$e_{n(TOTAL)} = \sqrt{10^2 + 8^2 + 8^2} = 15.1nV/\sqrt{Hz} \quad (11\text{-}13)$$

Working backward through the previous equations, we arrive back at the new SNR for the system:

$$SNR_{NEW} = 20\log\frac{0.707}{15.1 \bullet 10^{-9} \bullet \sqrt{50MHz}} = 76.4dB \quad (11\text{-}14)$$

Adding an amplifier with less noise than the ADC but more bandwidth resulted in an overall SNR 3.6dB less than the capability of the ADC. In order for the amplifier to be "transparent," meaning the system SNR is approximately the same as the ADC's SNR, the amplifier needs to have lower output noise density and/or lower bandwidth.

The preceding analysis and Figure 11-3 assume the alias bands are the same width as the Nyquist bandwidth. If this is not the case, then the resulting noise floor will have a multi-tiered shape, with a rise in the noise floor where the extra aliased noise occurs in frequency. This would also be the case if the amplifier's bandwidth or the anti-alias filter bandwidth was less than one Nyquist band, where the wideband noise rolls off before the Nyquist frequency of the ADC. However, an anti-alias filter would not affect the above calculations, except to change the amplifier's effective noise.

The visual analysis above indicates that once noise is "aliased" into the original Nyquist bandwidth, it is indistinguishable from lower-frequency noise. The two solutions presented so far focus on reducing the noise presented to the ADC input. If digital filtering is possible, there is a third solution, which would be to increase the ADC's sample rate. If the sample rate is increased so that the Nyquist bandwidth exceeds the input bandwidth, there is extra bandwidth that can be removed through digital filtering. Also, for a given analog bandwidth, there would be fewer bands of noise that are aliased, so the resulting noise floor would be lower as well.

12 APPENDIX C: OPTIMIZING NOISE PERFORMANCE BY CALCULATION OF VOLTAGE AND CURRENT NOISE CORRELATION

In order to understand the true interaction between current noise and voltage noise at the input of the LTC6400, it is necessary to consider the correlation between the two types of noise. Since the current and voltage noise source elements in the LTC6400 are largely the same, there

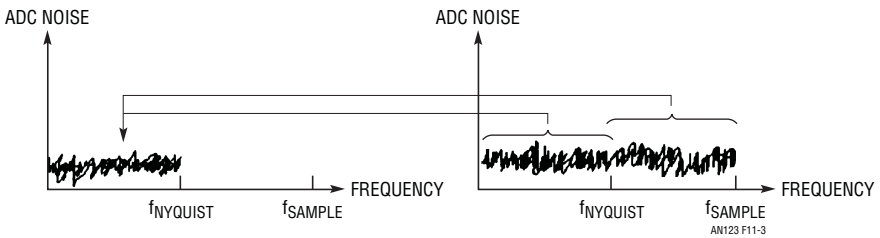


Figure 11-3. Representative ADC and Amplifier Noise Floors. Any Amplifier Noise that Exceeds the ADC's Nyquist Bandwidth Will be Aliased Back into the Nyquist Band and Combined with That Noise. In This Example, There are Two Full Nyquist Bands of Amplifier Noise That Will be Summed with the ADC's Noise. Since the Noise is Uncorrelated, the RMS Method (Square Root of Sum of Squares) Can Be Used to Add Them Together

should be some level of correlation between the two. If there is significant correlation, then it should be possible to find source impedances that would cause the current noise to partially cancel out the voltage noise (or add to it). The current noise source of the LTC6400 can be split into two separate noise sources: i_{nu} for the uncorrelated current noise, and i_{nc} for the correlated current noise. The uncorrelated current noise can be defined by an equivalent noise conductance, and is independent of the voltage noise. The correlated current noise has a complex (vector) relationship with the voltage noise.

$$i_{nu} = \sqrt{4kTG_U} \quad (12\text{-}1)$$

$$i_{nc} = Y_C \bullet e_n \quad (12\text{-}2)$$

G_U is a conductance that converts voltage to current, k is the Boltzmann constant, Y_C is the complex admittance defined as $Y_C = G_C + jB_C$, and e_n is the total input voltage noise density from the data sheet. The complex admittance (Y) is the inverse of the complex impedance Z = R + jX. From the Smith Chart and the values in Table 3-2, there is a relationship between the optimal noise factor and the desired values:[16]

$$F_{MIN} = 1 + 2R_N (G_{OPT} + G_C) \quad (12\text{-}3)$$

$$B_C = -B_{OPT} \quad (12\text{-}4)$$

$$G_U = R_N \bullet G_{OPT}^2 - R_N \bullet G_C^2 \quad (12\text{-}5)$$

Since F_{MIN} is the linear form of NF_{MIN} and R_N is the inverse of G_N, G_C can be found with the values in Table 3-2. As an example, the LTC6400-8 values will be used to solve for the current noise components.

$$Y_{OPT} = 1/Z_{OPT} = 0.001414 - j0.0008147 \quad (12\text{-}6)$$

$$F_{MIN} = 5.152 = 1 + 2 \bullet 885 \bullet (0.001414 + G_C) \quad (12\text{-}7)$$

$$G_C = 0.0009318 \quad (12\text{-}8)$$

$$Y_C = G_C + B_C = 0.0009318 + j0.0008147 \quad (12\text{-}9)$$

$$G_U = 885 \bullet 0.0014142 - 885 \bullet 0.00093182 = 0.001 \quad (12\text{-}10)$$

$$i_{nc} = Y_C \bullet e_n = Y_C \bullet 3.7nV/\sqrt{Hz} = 3.45 + j3.01\ pA/\sqrt{Hz} \quad (12\text{-}11)$$

$$i_{nu} = \sqrt{(4 \bullet k \bullet 290 \bullet 0.001)} = 4.00\ pA/\sqrt{Hz} \quad (12\text{-}12)$$

Equation 12-11 shows that the correlated current noise has a significant reactive component. If voltage noise were ignored, the total current noise is simply the RMS sum of inu and the magnitude of inc (they are not correlated to each other). However, a complex source impedance Z_S could result in the current noise adding to or partially cancelling the voltage noise (depending on the phase of $i_{nc} \bullet Z_S$), so the total noise varies with source impedance. This happens even if Z_S has no reactive component. The source impedance for optimal noise figure is $\Gamma_{S,OPT}$ in Figure 3-7, where the imaginary part of i_{nc} is cancelled to create a noise minimum.

13 APPENDIX D: WORKS CITED

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Note 16: The mathematical derivation for F_{MIN} can be found in (Ludwig, Bretchko and Bogdanov 2008). B_C is also derived from the same formulas, based on a minimization of the noise factor equation.

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