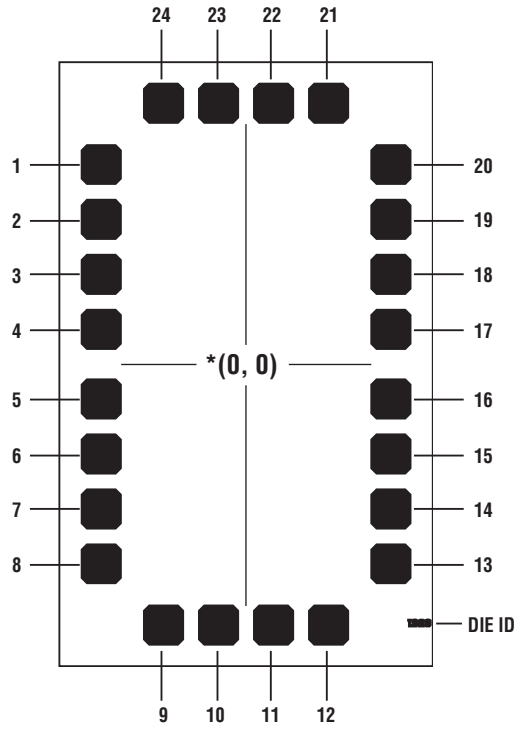
Four-Channel Multiplexed Transimpedance Amplifier with Output Multiplexing



Die Size: 36mils (914.4µm)× 55mils (1397µm)
Bond Pad Size: 4mils (102µm)× 4mils (102µm)
Bond Pad Opening: 3.2mils (82µm)× 3.2mils (82µm)
Bond Pad Metal Thickness: 0.29mils (7.4µm)
Wafer Saw Street Width: 2.4mils (61µm)
Wafer/Die Thickness: 8mils (200µm)
Backside Metal: None
Backside Potential: V^-

PAD #	PAD NAME	X COORDINATE (µm)	Y COORDINATE (µm)
1	CHSEL1	417.9	303.24
2	V_{CCO}	302.9	303.24
3	CHSEL0	187.9	303.24
4	V_{CC1}	72.9	303.24
5	V_{REF1}	–72.9	303.24
6	GND	–187.9	303.24
7	IN1	–302.9	303.24
8	GND	–417.9	303.24
9	IN2	–546.21	172.5
10	V_{REF2}	–546.21	57.5
11	V_{REF3}	–546.21	–57.5
12	IN3	–546.21	–172.5
13	GND	–417.9	–303.24
14	IN4	–302.9	–303.24
15	GND	–187.9	–303.24
16	V_{REF4}	–72.9	–303.24
17	V_{CC2}	72.9	–303.24
18	O_MUX	187.9	–303.24
19	V_{CCO}	302.9	–303.24
20	DNC	417.9	–303.24
21	OUTTERM	546.21	–172.5
22	GND	546.21	–57.5
23	GND	546.21	57.5
24	OUT	546.21	172.5

*Die center coordinate (0, 0)

FEATURES

- **220MHz –3dB Bandwidth with 2pF Input Capacitance**
- **Single-Ended Output**
- **74kΩ Transimpedance Gain**
- **4.8pA/√Hz Input Current Noise Density at 200MHz (2pF)**
- **64nA$_{RMS}$ Integrated Input Current Noise Over 200MHz (2pF)**
- **Linear Input Range 0µA to 30µA**
- Overload Current > ±400mA Peak
- Fast Overload Recovery 12ns, 1mA
- Fast Channel Switchover < 50ns
- Single 5V Supply
- 200mW Power Dissipation for 4 Channels
- 2V$_{P-P}$ Output Swing on 100Ω Load
- Output MUX Combines Multiple 4-Channel Devices to Create 4, 8,12,16, 24, 32 Channel Solutions

APPLICATIONS

- LIDAR Receiver
- Industrial Imaging

DESCRIPTION

The LTC®6561 is a low-noise, four-channel, transimpedance amplifier (TIA) with 220MHz bandwidth. The LTC6561 multi-channel transimpedance amplifier's low noise, high transimpedance, and low power dissipation are ideal for LIDAR receivers using Avalanche Photodiodes (APDs). The amplifier features 74kΩ transimpedance gain and 30µA linear input current range. Using an APD input circuit with a total capacitance of 2pF, the input current noise density is 4.8pA/$\sqrt{Hz}$ at 200MHz. With lower capacitance, noise and bandwidth improve further. Only a 5V single supply is needed and the device consumes only 200mW. Utilizing the internal 4-to-1 MUX along with the LTC6561's output MUX; multiple 4-channel LTC6561 devices can be combined to directly interface with 12-, 16- and 32-channel APD arrays. The LTC6561's fast overload recovery and fast channel switchover make it well suited for LIDAR receivers with multiple APDs. Its single-ended output can swing $2V_{P-P}$ on a 100Ω load while its low impedance op amp style output can drive back-terminated 50Ω cables.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V_{CC1}, V_{CC2}, V_{CCO} to GND).....5.5V
Input Voltage (CHSEL0, CHSEL1, O_MUX).....–0.3V to 5.5V
Amplifier Reference Current (V_{REF1}, V_{REF2}, V_{REF3}, V_{REF4}).....±10mA
Amplifier Input Current (IN1, IN2, IN3, IN4) ..... ±400mA RMS ±2A Transient (10ns)
Amplifier Output Current (OUT, OUTTERM).....+80mA
Operating Temperature Range
LTC6561.....–40°C to 125°C
Storage Temperature Range.....–65°C to 150°C
Junction Temperature .....150°C

DIE CROSS REFERENCE

FINISHED PART NUMBER	ORDER PART NUMBER
LTC6561	LTC6561 DICE/DWF

Please refer to ADI standard LTC6561 product data sheet for other applicable product information and typical performance information.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, $V_{CC1,2}$ = V_{CCO} = 5V, O_MUX = 0V, GND = 0V, Z_{LOAD} = 100Ω. Output taken from OUT pin.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BW	–3dB Bandwidth	200mV_{P-POUT} and $C_{IN,TOT}$ = 2pF			220		MHz
R_T	Small Signal Transimpedance	I_{IN} < 2µA_{P-P}		63	74	85	kΩ
R_{IN}	Input Resistance	f = 100kHz			236		Ω
R_{OUT}	Output Resistance	f = 100kHz			3		Ω
I_n	Input Current Noise Density	f = 100MHz, $C_{IN,TOT}$ = 2pF			4.3		pA/$\sqrt{Hz}$
		f = 200MHz, $C_{IN,TOT}$ = 2pF			4.8		pA/$\sqrt{Hz}$
	Integrated Input Current Noise	f = 0.1MHz to 100MHz, $C_{IN,TOT}$ = 2pF			43		nA_{RMS}
		f = 0.1MHz to 200MHz, $C_{IN,TOT}$ = 2pF			64		nA_{RMS}
	Adjacent Channel to Channel Isolation	f = 100MHz			–45		dB
	Non Adjacent Channel Isolation	f = 100MHz			–65		dB
$t_{RECOVER}$	Overload Recovery Time	Input Pulse <1mA			12		ns
t_{SWITCH}	Channel Switchover Time				50		ns

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, $V_{CC1,2}$ = V_{CC0} = 5V, O_MUX = 0V, GND = 0V, Z_{LOAD} = 100Ω.
Output taken from OUT pin.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN1,2,3,4 Pins and $V_{REF1,2,3,4}$ Pins							
V_{IN}	Input Bias Voltage	Active Channel Inactive Channel		1.43 0.78	1.55 0.93	1.64 1.38	V V
V_{REF}	Input Reference Voltage	Active Channel Inactive Channel		1.43 1.34	1.55 1.50	1.63 1.67	V V
Offset	$V_{IN} – V_{REF}$	Active Channel Inactive Channel		–12 –741		12 –116	mV mV
OUT Pin							
V_{OUT}	Output Default Voltage	O_MUX = 0V (Output Enabled) O_MUX = 3.3V, Standalone Device		0.83 0.32	1.10 0.60	1.47 0.88	V V
OVR	Output Voltage Range	I_{IN} Current Range = 0 to –50µA		1.22	1.90	2.58	V_{P-P}
OUTTERM	Internal Series Resistor for Optional Output			44	56	70.8	Ω
CHSEL0, CHSEL1, O_MUX Pins with Internal Pull-Down Resistors							
V_{IL}						0.7	V
V_{IH}				1.5			V
I_{IL}	Pin Voltage = 0.7V			16.9	20.7	26.0	µA
I_{IH}	Pin Voltage = 1.5V			37	47	57	µA
C_{IN}					1.5		pF
R_{IN}				22	29	35	kΩ
Power Supply							
V_S	Operating Supply Range			4.75	5	5.25	V
$I_{CC1,2}$	Input Supply Current	V_{CC1} & V_{CC2} are Internally Tied Together		29	36.3	44	mA
I_{CC0}	Output Supply Current	Both V_{CC0} Pins are Internally Tied Together		1.8	2.3	2.8	mA
I_S	Total Supply Current ($I_{S(VCC1,2)}$ + $I_{S(VCC0)}$)			30.8	38.6	46.8	mA
PSRR($V_{CC1,2}$)	Input Power Supply Rejection Ratio	$V_{CC1,2}$ = 4.75V to 5.25V, V_{CC0} = 5V		21	25		dB
PSRR(V_{CC0})	Output Power Supply Rejection Ratio	V_{CC0} = 4.75V to 5.25V, $V_{CC1,2}$ = 5V		34	40		dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All measurement were conducted in the dark.

PAD FUNCTIONS

CHSEL1: MSB for Channel Selection. CMOS input. The CHSEL1 pad has a 29kΩ internal pull-down resistor. Default value is 0V.

V_{CCO}: Positive Power Supply for the Output Stage. Typically 5V. V_{CCO} can be tied to V_{CC1} or V_{CC2} for single supply operation. Between the positive supply and ground, bypass capacitors of 1000pF and 0.1µF should be placed as close to the part as possible. V_{CCO} pads are internally tied together.

CHSEL0: LSB for Channel Selection. CMOS input. The CHSEL0 pad has a 29kΩ internal pull-down resistor. Default value is 0V.

V_{CC1}, V_{CC2}: Positive Power Supply. Typically 5V. Between the positive supply and ground, bypass capacitors of 1000pF and 0.1µF should be placed as close to the part as possible. V_{CC1} and V_{CC2} are internally tied together.

V_{REF1}, V_{REF2}, V_{REF3}, V_{REF4}: Reference Voltage Pad for Transimpedance Amplifier in Channel 1, 2, 3, and 4 Respectively. This pad sets the input DC voltage for each transimpedance amplifier. The V_{REF} pad has a Thevenin equivalent resistance of approximately 1.4k and can be overdriven by an external voltage. If no voltage is applied to V_{REF}, it will float to a default voltage of approximately 1.55V on a 5V supply. Each V_{REF} pad should be bypassed with a high quality ceramic bypass capacitor of at least 0.1µF. The bypass cap should be located close to its V_{REF} pad.

GND: Negative Power Supply. Normally tied to ground.

IN1, IN2, IN3, IN4: Input Pad for Transimpedance Amplifier for Channels 1, 2, 3, and 4 Respectively. This pad is internally biased to 1.55V.

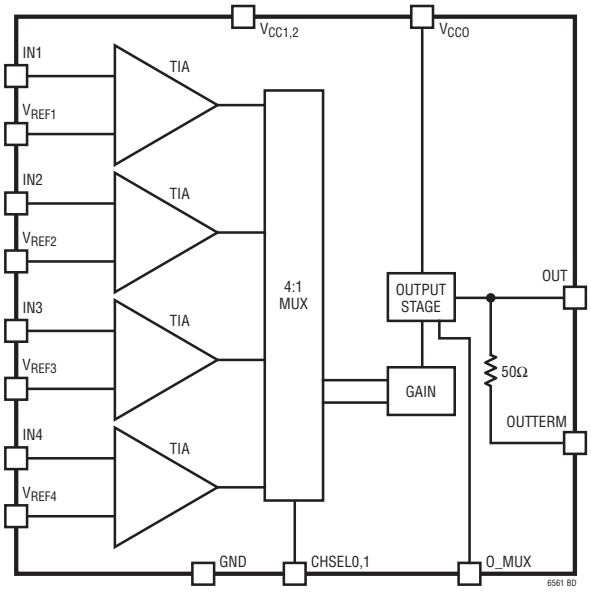
O_MUX: Output MUX. CMOS Input. This pad is functional when multiple LTC6561s are combined at the output. When O_MUX is low, the output is enabled. When O_MUX is high, all 4 inputs are decoupled from the output. Default value is 0V. This MUX pad is ineffective unless a 2nd LTC6561 is DC-coupled at the output. See Applications section on how to use O_MUX to expand the channel count with multiple LTC6561's. The O_MUX pad has a 29kΩ internal pull-down resistor.

DNC: Do not connect.

OUTTERM: TIA Output with an Internal Series 50Ω Resistor.

OUT: TIA Output without an internal series 50Ω Resistor.

BLOCK DIAGRAM



Wafer level testing is performed per indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-6561