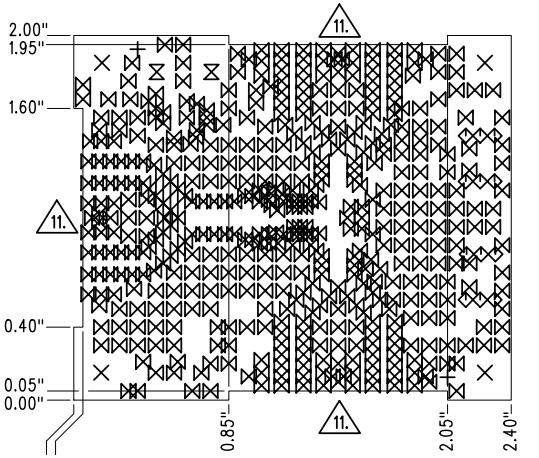
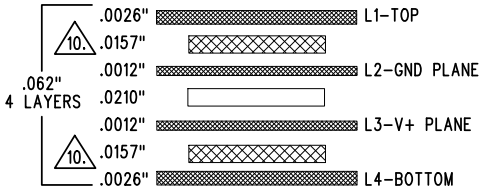
REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
–	3	PRODUCTION	MICHEL A.	08-15-12



DRILL DRAWING LAYER
LINEAR TECHNOLOGY
DC1765A-3 LTC6957HMS-1/-2 DATE: 08-15-12
LOW PHASE NOISE, DUAL LVPECL OR LVDS OUTPUT
BUFFER/ DRIVER/ LOGIC CONVERTER

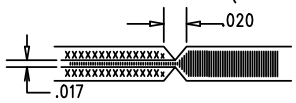
SIZE	QTY	SYM	PLATED	TOL
0.07	2	+	NO	+/-0.003"
0.187	4	X	NO	+/-0.003"
0.035	12	◇	YES	+/-0.003"
0.094	2	⧖	YES	+/-0.003"
0.012	493	⋈	YES	+/-0.003"

LAYER STRUCTURE



NOTES: UNLESS OTHERWISE SPECIFIED

1. FAB PER IPC-A-600.
2. MATERIAL: -EPOXY FIBERGLASS, NELCO 4000-13
   -FINISHED THICKNESS TO BE 0.062" +/- .005"
   -TOTAL OF 4 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.
   -FLAMMABILITY RATING: 94 V-0 MINIMUM.
3. SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN. 0.00" ARE PRIMARY DATUMS.
4. DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
   -ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
   -HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
5. FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.
   -GOLD IMMERSION BOTH SIDES.
   -FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
6. DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE. PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
7. PCBS ARE TO BE RoHS COMPLIANT.
8. SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):

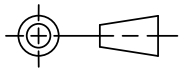


9. CONTROLLED 50 OHM +/-5% IMPEDANCE FOR LAYERS 1-2 USING 0.03" TRACE.

10. SUBJECT TO CHANGE BY MANUFACTURER, DEPENDING ON DIELECTRIC CONSTANT DEVIATIONS. PLEASE CONSULT LTC.

11. INNER AND OUTER LAYER COPPER SHALL BE EXPOSED ALONG BOARD EDGES. DO NOT MODIFY INNER LAYER COPPER BACKOFF OUTLINE (SMA CONNECTOR).

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
0.XX" = ±0.01"
0.XXX" = ±0.005"
INTERPRET DIM AND TOL PER ASME Y14.5M-1994
THIRD ANGLE PROJECTION



APPROVALS	
PCB DES.	KIM T.
APP ENG.	MICHEL A.

SCALE = NONE

LINEAR TECHNOLOGY
1630 MCCARTHY BLVD
MILPITAS, CA 95035
PH: (408)432-1900
www.linear.com
LTC CONFIDENTIAL-
FOR CUSTOMER USE ONLY

TITLE: FABRICATION DRAWING
LOW PHASE NOISE, DUAL LVPECL OR LVDS OUTPUT BUFFER/ DRIVER/ LOGIC CONVERTER

SIZE	IC NO.	REV
N/A	LTC6957HMS-1/-2 DEMO CIRCUIT 1765A	3

FILENAME: DC1765A-3.PCB SHT 1 OF 1