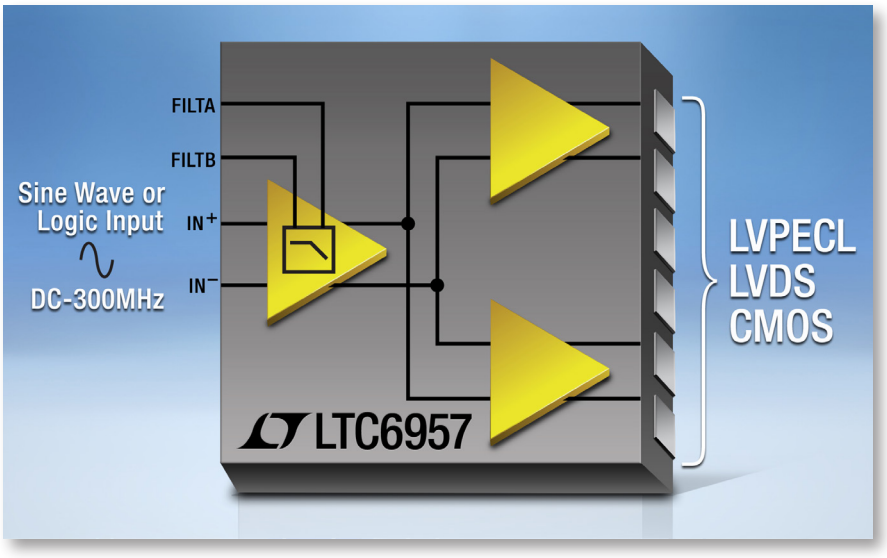
Low Phase Noise Reference Buffer/Logic Converter



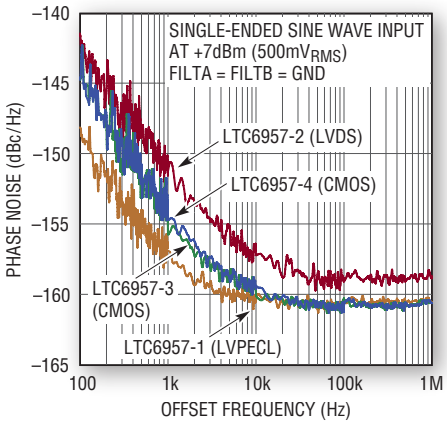
Converts Sine Waves to Logic Levels with Lowest Additive Jitter

The LTC®6957 is a dual output buffer/driver/logic translator, ideal for converting sine waves into low phase noise logic level signals. The device converts any DC to 300MHz reference frequency into dual LVPECL, LVDS or CMOS outputs with exceptionally low additive jitter (less than 200fs$_{RMS}$ total jitter). The LTC6957 also features a proprietary, selectable, input stage bandwidth-limiting feature, which substantially improves the additive phase noise for slow slewing signals by up to 3dB to 4dB.

Features

- Low Phase Noise Buffer/Driver
- Three Logic Output Types Available:
  - LVPECL (LTC6957-1)
  - LVDS (LTC6957-2)
  - In-Phase CMOS (LTC6957-3)
  - Complementary CMOS (LTC6957-4)
- Additive Jitter: <45fs$_{RMS}$ (LVPECL)
- 3.3V Supply Operation
- Low Output Skew: 3ps Typical
- Fully Specified from –40°C to 125°C
- Available in 12-Pin MSOP & 3mm × 3mm DFN Packages

Additive Phase Noise at 100MHz



LINEAR TECHNOLOGY

The LTC6957 includes input filtering with three narrowband settings in addition to the full bandwidth limitation of the circuit design (Table 1). For slow slewing signals (ie <100MHz sine wave signals), substantially lower additive phase noise can be achieved using this feature.

The optimal filter setting depends on the clock frequency, amplitude, and waveform shape, with the major determinant being the slew rate at the input of the LTC6957. Table 2 shows the slew rate ranges most suitable for the four specific filter settings.

Another way to look at this is to consider the case of sine waves, for which the frequency ranges will depend on the input amplitudes, as shown in Table 3.

The LTC6957-1 100MHz phase noise plots in the figures below illustrate the trade-offs between filter settings at various input slew rates. For a 100MHz sine wave, a 10dBm input level results in a slew rate of 628V/µs. Table 2 indicates the best filter setting to use is FILTA = FILTB = L which is supported by the blue trace in Figure a.

With 0dBm at 100MHz, the input slew rate is 198V/µs. Table 2 indicates that the best filter setting is FILTA = H, FILTB = L which is supported by the green trace in Figure b. As the input decreased 10dB from Figure a to Figure b, the blue trace rose 5dB while the green trace only rose 3dB.

With –10dBm at 100MHz, the input slew rate is 63V/µs. Table 2 recommends the best filter setting is FILTA = L, FILTB = H which is supported by the red trace in Figure c. As the input decreases 10dB from Figure a to Figure b, then 10dB from Figure b to Figure c, the red trace rose 3dB, then 4dB, while the blue and green traces rose much faster.

Table 1

FILTA	FILTB	BANDWIDTH
Low	Low	1200MHz (Full Bandwidth)
High	Low	500MHz (–3dB)
Low	High	160MHz (–3dB)
High	High	50MHz (–3dB)

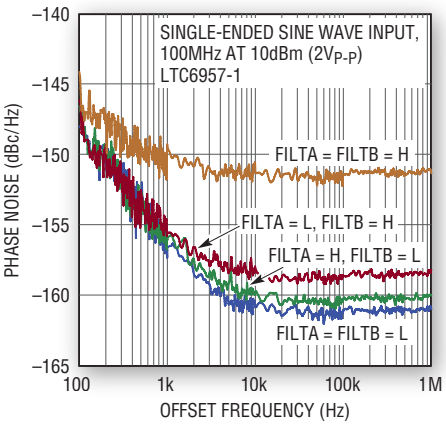
Table 2

FILTA	FILTB	INPUT SLEW RATE (V/µs)
Low	Low	>400
High	Low	125 to 400
Low	High	40 to 125
High	High	<40

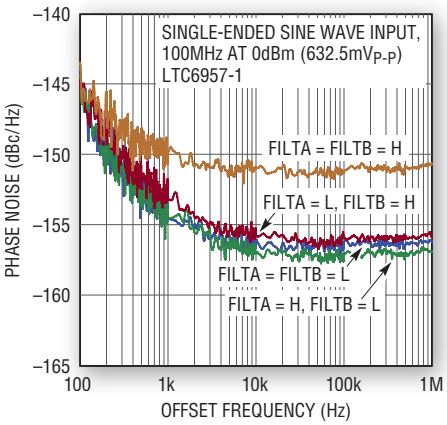
Table 3

	FREQUENCY RANGE			
INPUT AMPLITUDE (dBm)	FILTA = L, FILTB = L (MHz)	FILTA = H, FILTB = L (MHz)	FILTA = L, FILTB = H (MHz)	FILTA = H, FILTB = H (MHz)
10	>63	20 to 63	6.3 to 20	<6.3
5	>112	35 to 112	11 to 35	<11
0	>200	63 to 200	20 to 63	<20
–5		>112	35 to 112	<35
–10		>200	63 to 200	<63

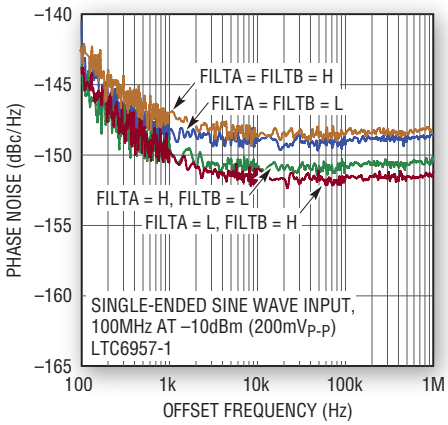
LTC6957-1 (LVPECL) Additive Phase Noise at 100MHz with Varying Input Amplitudes



(a)



(b)



(c)