40V, Low I_Q, 3MHz, 2-Phase Synchronous Boost Controller

FEATURES

- **2-Phase Operation Reduces Required Input and Output Capacitance and Power Supply Induced Noise**
- **Synchronous Operation for Highest Efficiency and Reduced Heat Dissipation**
- **Wide Input Voltage Range: 4.5V to 40V, Operates Down to 1V After Start-Up**
- **Output Voltage Up to 40V**
- **Low Operating Quiescent Current: 18µA**
- **PassThru™ Operation: 100% Duty Cycle Capability for Synchronous MOSFET**
- **R_{SENSE} or Inductor DCR Current Sensing**
- **Spread Spectrum Operation**
- Programmable Fixed Frequency (100kHz to 3MHz)
- Phase-Lockable Frequency (100kHz to 3MHz)
- Selectable Continuous, Pulse-Skipping, or Low Ripple Burst Mode® Operation at Light Loads
- Input Current Monitor Output
- Internal LDO Powers Gate Drive from V_{BIAS} or $EXTV_{CC}$
- Low Shutdown I_Q: 1.5µA
- Side Wettable 28-Lead 4mm × 5mm QFN Package
- AEC-Q100 Automotive Qualification in Process

APPLICATIONS

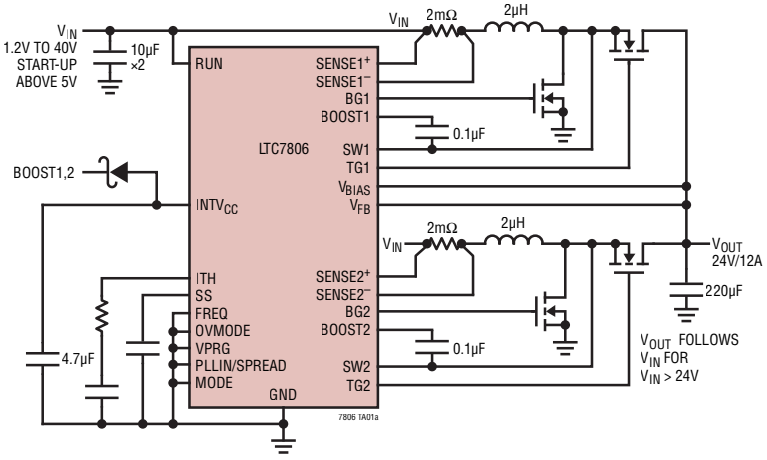
- Automotive and Transportation
- Audio and RF Power Amplifiers
- Industrial and Medical
- Communications

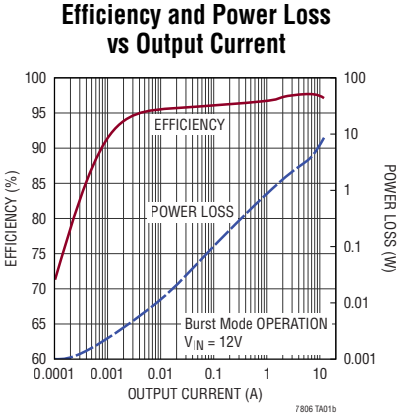
DESCRIPTION

The LTC®7806 is a high performance 2-phase single output synchronous boost converter controller that drives two N-channel power MOSFET stages out-of-phase. Its constant-frequency current mode architecture allows a phase-lockable switching frequency of up to 3MHz. High frequency 2-phase operation reduces input and output capacitor requirements and allows the use of smaller inductors compared to the single-phase equivalent. Synchronous rectification increases efficiency, reduces power losses, and eases thermal requirements, simplifying high power boost applications. The synchronous PassThru capability also minimizes losses in automotive start-stop applications.

The LTC7806 operates from a wide 4.5V to 40V input supply range. When biased from the boost converter output, the LTC7806 can operate from an input supply as low as 1V after start-up. The very low no-load quiescent current extends operating run time in battery powered systems. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The LTC7806 features a precision 1.2V reference, a power good output indicator, and an inductor current monitor.

TYPICAL APPLICATION





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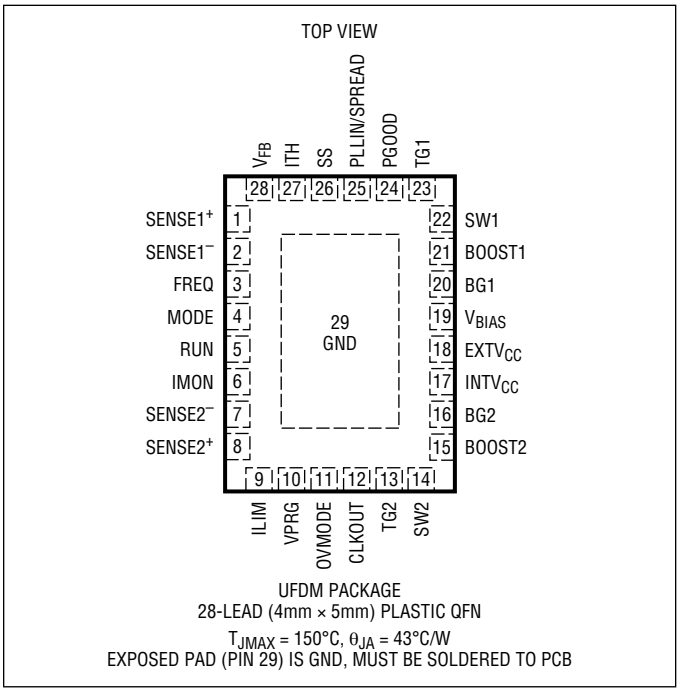
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Bias Input Supply Voltage (V_{BIAS}) ..... –0.3V to 40V
RUN Voltage ..... –0.3V to 40V
BOOST1, BOOST2 Voltages ..... –0.3V to 46V
Switch Voltage (SW1, SW2) ..... –5V to 40V
(BOOST1 – SW1), (BOOST2 – SW2) ..... –0.3V to 6V
SENSE1+, SENSE1– Voltages ..... –0.3V to 40V
SENSE2+, SENSE2– Voltages ..... –0.3V to 40V
V_{FB} Voltage ..... –0.3V to 40V
$EXTV_{CC}$ Voltage ..... –0.3V to 30V
$INTV_{CC}$ Voltage ..... –0.3V to 6V
SS, CLKOUT, VPRG, IMON Voltages ..... –0.3V to 6V
MODE, PGOOD, OVMODE Voltages ..... –0.3V to 6V
PLLIN/SPREAD, FREQ, ILIM Voltages ..... –0.3V to 6V
ITH Voltage ..... –0.3V to 2V
BG1, BG2, TG1, TG2 ..... (Note 8)
Operating Junction Temperature Range (Notes 2, 7)
LTC7806I ..... –40°C to 125°C
LTC7806R, LTC7806J ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Maximum Junction Temperature (T_J) ..... 150°C

PIN CONFIGURATION



UFDM PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7806RUFDM#PBF	LTC7806RUFDM#TRPBF	7806	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LTC7806IUFDM#WPBF	LTC7806IUFDM#WTRPBF	7806	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC7806JUFDM#WPBF	LTC7806JUFDM#WTRPBF	7806	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{BIAS} = 12V, RUN > 1.25V, $EXTV_{CC}$ = 0V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input and Output Supplies							
V_{BIAS}	Bias Supply Operating Range			4.5		40	V
V_{IN}	Input Supply Operating Range	$V_{BIAS} \geq 4.5V$		1		40	V
V_{OUT}	Output Voltage Operating Range			V_{IN}		40	V
Controller Operation							
V_{FB}	Regulated Feedback Voltage	(Note 3) V_{BIAS} = 4.5V to 40V, ITH Voltage = 0.6V to 1.2V,					
		VPRG = FLOAT	●	1.185	1.200	1.212	V
		VPRG = 0V	●	23.5	24	24.5	V
		VPRG = $INTV_{CC}$	●	27.5	28	28.5	V
	Feedback Current in Regulation	VPRG = FLOAT			±5	±50	nA
		VPRG = 0V or $INTV_{CC}$			4		µA
	Feedback Current in Shutdown	RUN = 0V			±5	±50	nA
	Overvoltage Protection Threshold	OVMODE = 0V, V_{FB} Rising Relative to Regulated V_{FB}		8	11	14	%
g_m	Transconductance Amplifier g_m				1.8		mmho
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{FB} = 1.1V, $V_{SENSE1,2}^+$ =12V					
		ILIM = 0V	●	21	25	29	mV
		ILIM = FLOAT	●	44	50	55	mV
		ILIM = $INTV_{CC}$	●	66	75	83	mV
	Matching Between Channels	$V_{SENSE1,2}^+$ = 12V		–3.3	0	3.3	mV
$I_{SENSE1,2}^-$	SENSE1,2⁻ Pin Currents	$V_{SENSE1,2}^-$ = 12V				±1	µA
I_{SENSE1}^+	SENSE1⁺ Pin Current	$V_{SENSE1}^+ \leq 2.8V$			1		µA
		$3.2V \leq V_{SENSE1}^+ < INTV_{CC} – 0.5V$			50		µA
		$V_{SENSE}1^+ > INTV_{CC} + 0.5V$			750		µA
I_{SENSE2}^+	SENSE2⁺ Pin Current	$V_{SENSE2}^+ < INTV_{CC} – 0.5V$				±2	µA
		$V_{SENSE2}^+ > INTV_{CC} + 0.5V$			700		µA
	Soft-Start Charge Current	V_{SS} = 0V		10	12.5	15	µA
	RUN Pin ON Threshold	V_{RUN} Rising	●	1.15	1.20	1.25	V
		Hysteresis			100		mV
DC Supply Current (Note 4)							
	V_{BIAS} Shutdown Current	RUN = 0V			1.5		µA
	V_{BIAS} Sleep Mode Current	$SENSE1^+ < 3.2V$, $EXTV_{CC}$ = 0V			18		µA
	Sleep Mode Current	$SENSE1^+ \geq 3.2V$					
		V_{BIAS} Current, $EXTV_{CC}$ = 0V			5	11	µA
		V_{BIAS} Current, $EXTV_{CC} \geq 4.8V$			1	4	µA
		$EXTV_{CC}$ Current, $EXTV_{CC} \geq 4.8V$			7	14	µA
		$SENSE1^+$ Current			12	22	µA
	Pulse-Skipping or Forced Continuous, V_{BIAS} or $EXTV_{CC}$ Current	V_{FB} = 1.25V			5		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{BIAS} = 12V, RUN > 1.25V, $EXTV_{CC}$ = 0V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Drivers							
	TG or BG On-Resistance	Pull-Up Pull-Down			1.2 0.6		Ω Ω
	TG or BG Transition Time Rise Time Fall Time	(Note 5) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 15		 ns ns
	TG Off to BG On Delay Time	C_{LOAD} = 3300pF Each Driver			15		ns
	BG Off to TG On Delay Time	C_{LOAD} = 3300pF Each Driver			15		ns
$t_{ON(MIN)1,2}$	BG Minimum On-Time	(Note 6)			105		ns
	Maximum Duty Factor for BG	f_{OSC} = 750kHz			93		%
	Maximum Duty Factor for TG	OVMODE = 0V, in Overvoltage			100		%
	Boost Charge Pump Available Output Current	$V_{BOOST1,2}$ = 16V, $V_{SW1,2}$ = 12V, FREQ = 0V, Forced Continuous Mode		100	180		µA
	IMON Current Monitor Output Voltage	ILIM = $INTV_{CC}$ or FLOAT $V_{SENSE2+} - V_{SENSE2^-} = V_{SENSE(MAX)}$ $V_{SENSE2+} - V_{SENSE2^-} = 0.3 \bullet V_{SENSE(MAX)}$		 1.34 0.6	 1.4 0.7	 1.46 0.8	 V V
		ILIM = 0V $V_{SENSE2+} - V_{SENSE2^-}$ = 25mV $V_{SENSE2+} - V_{SENSE2^-}$ = 7.5mV		 1.25 0.5	 1.4 0.7	 1.55 0.9	 V V
$INTV_{CC}$ Low Dropout (LDO) Linear Regulator							
	$INTV_{CC}$ Regulation Point			5.2	5.4	5.6	V
	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 100mA, $V_{BIAS} \geq$ 6V I_{CC} = 0mA to 100mA, $V_{EXTVCC} \geq$ 6V			1 1	3 2	% %
	$EXTV_{CC}$ LDO Switchover Voltage	$EXTV_{CC}$ Rising Hysteresis		4.5	4.65 0.25	4.8	V V
UVLO	Undervoltage Lockout	$INTV_{CC}$ Rising $INTV_{CC}$ Falling	● ●	4.1 3.8	4.2 3.9	4.4 4.1	V V
Spread Spectrum Oscillator and Phase-Locked Loop							
f_{OSC}	Low Fixed Frequency	V_{FREQ} = 0V, PLLIN/SPREAD = 0V		320	370	420	kHz
	High Fixed Frequency	V_{FREQ} = $INTV_{CC}$, PLLIN/SPREAD = 0V	●	2.0	2.25	2.5	MHz
	Programmable Frequency	R_{FREQ} = 374kΩ, PLLIN/SPREAD = 0V R_{FREQ} = 75kΩ, PLLIN/SPREAD = 0V R_{FREQ} = 12.1kΩ, PLLIN/SPREAD = 0V		 450	100 500 3	 550	kHz kHz MHz
	Synchronizable Frequency Range	PLLIN/SPREAD = External Clock	●	0.1		3	MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{BIAS} = 12V, RUN > 1.25V, $EXTV_{CC}$ = 0V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	PLLIN Input High Level PLLIN Input Low Level		● ●	2.2		 0.5	V V
	Spread Spectrum Frequency Range (Relative to f_{OSC})	PLLIN/SPREAD = $INTV_{CC}$ Minimum Frequency Maximum Frequency			 0 +20		 % %
PGOOD Output							
	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.2	0.4	V
	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
	PGOOD Trip Level V_{FB} Relative to Set Regulation Point	V_{FB} Rising Hysteresis		8	11 3	14	% %
		V_{FB} Falling Hysteresis		–14	–11 3	8	% %
	PGOOD Delay for Reporting a Fault				25		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7806R is specified over the –40°C to 150°C operating junction temperature range, the LTC7806I is guaranteed over the –40°C to 125°C operating junction temperature range, and the LTC7806J is guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: The LTC7806 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 5: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

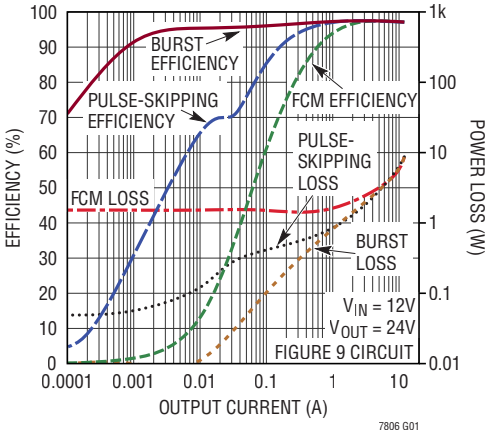
Note 6: See Minimum On-Time Considerations in the Applications Information section.

Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

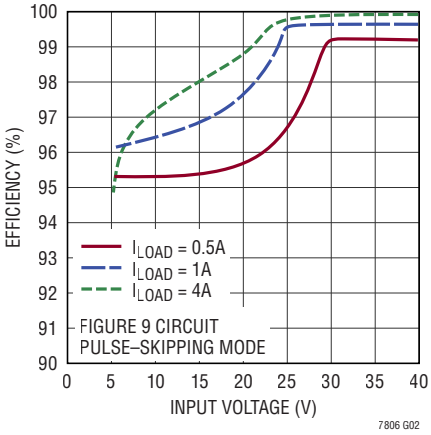
Note 8: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only otherwise permanent damage may occur.

TYPICAL PERFORMANCE CHARACTERISTICS

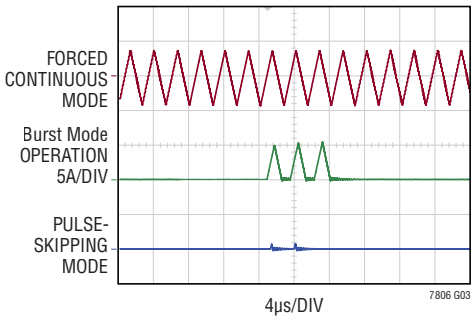
Efficiency and Power Loss vs Output Current



Efficiency vs Input Voltage

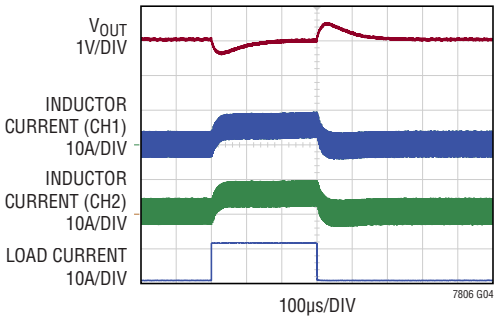


Inductor Current at Light Load



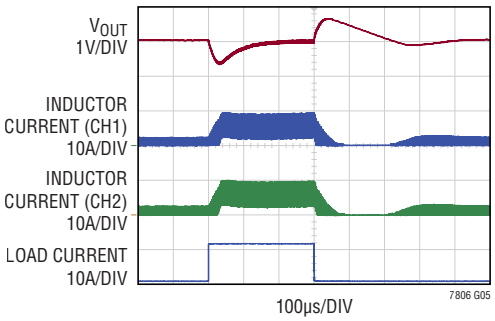
VIN = 12V
NO LOAD
FIGURE 9 CIRCUIT

Load Step Forced Continuous Mode



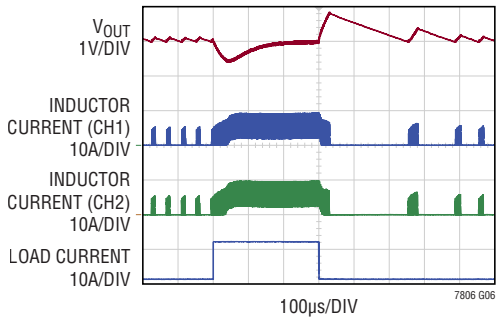
VIN = 12V
400mA TO 12A LOAD STEP
FIGURE 9 CIRCUIT

Load Step Pulse-Skipping Mode



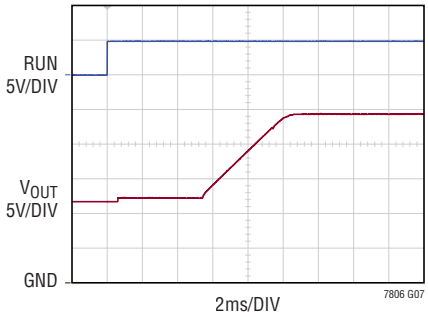
VIN = 12V
400mA TO 12A LOAD STEP
FIGURE 9 CIRCUIT

Load Step Burst Mode Operation



VIN = 12V
400mA TO 12A LOAD STEP
FIGURE 9 CIRCUIT

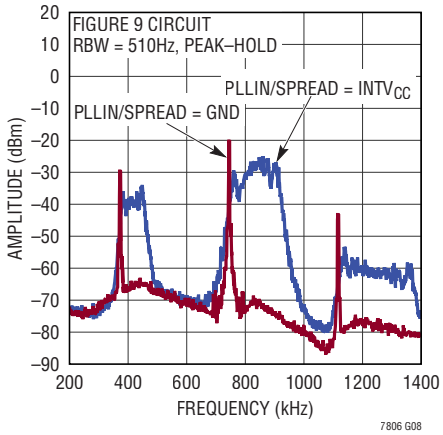
Soft Start-Up



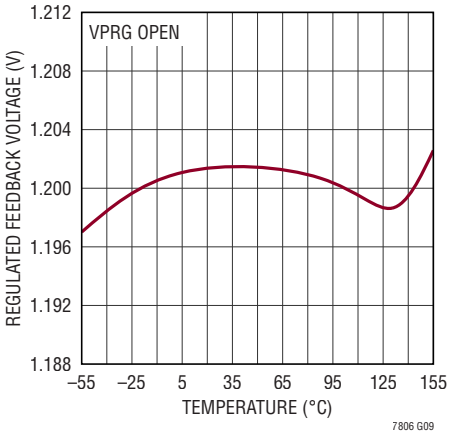
VIN = 12V
FIGURE 9 CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS

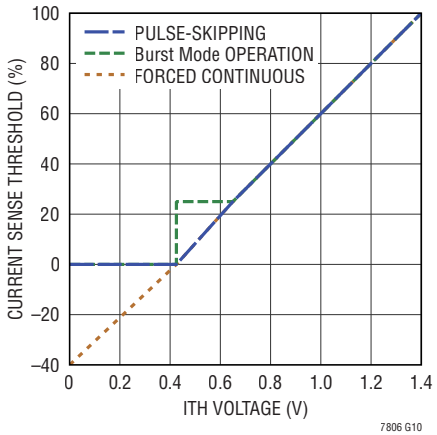
Output Voltage Noise Spectrum



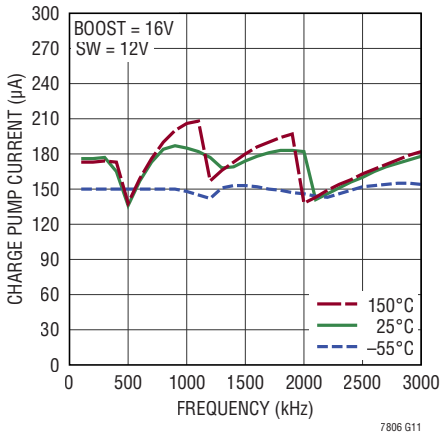
Regulated Feedback Voltage vs Temperature



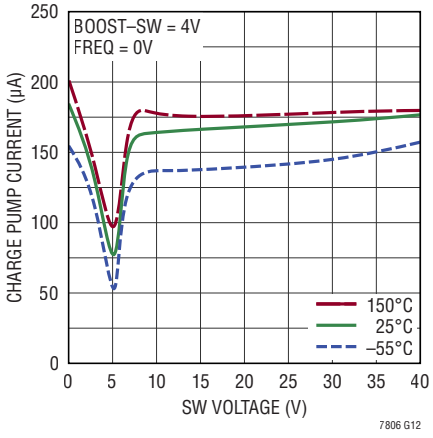
Current Sense Threshold Relative to $V_{SENSE(MAX)}$ vs I_{TH} Voltage



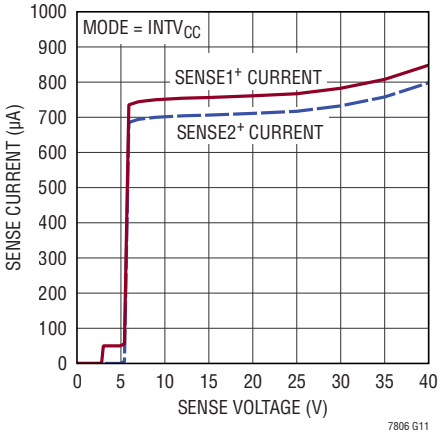
Boost Charge Pump Output Current vs Frequency



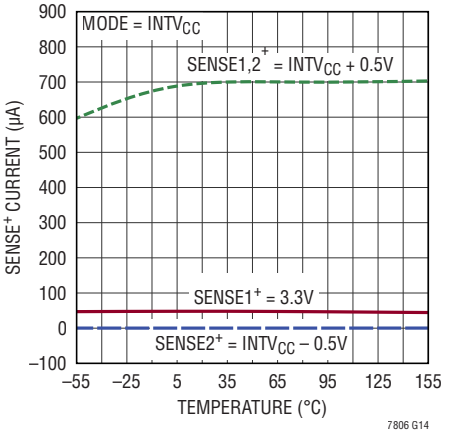
Boost Charge Pump Output Current vs SW Voltage



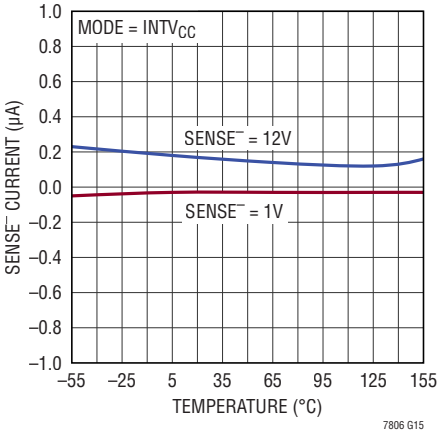
SENSE1,2⁺ Current vs Voltage



SENSE1,2⁺ Current vs Temperature

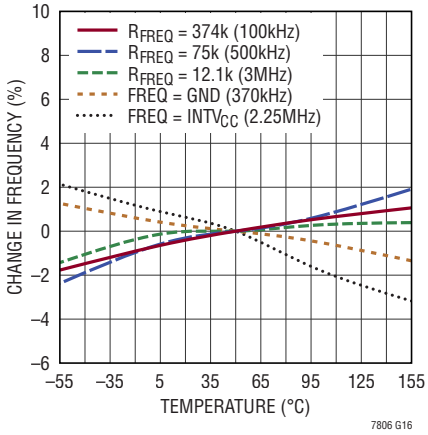


SENSE1,2⁻ Current vs Temperature

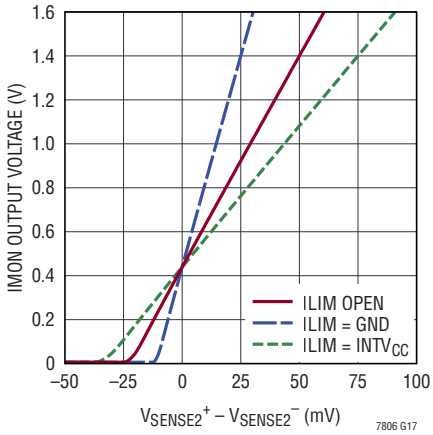


TYPICAL PERFORMANCE CHARACTERISTICS

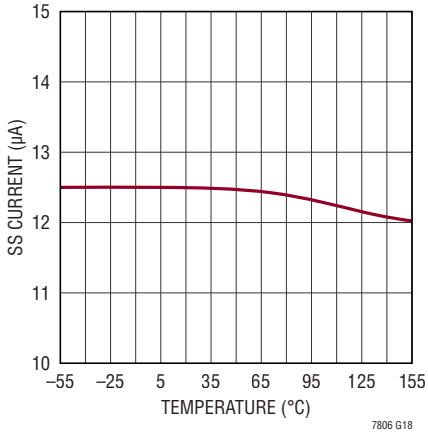
Oscillator Frequency vs Temperature



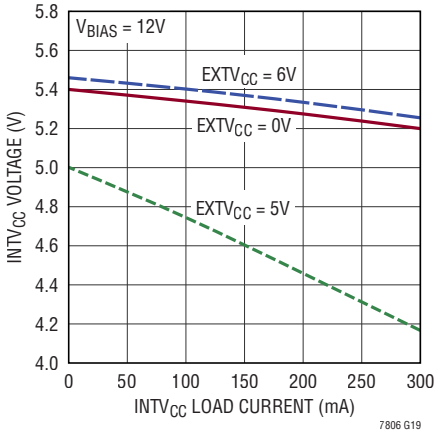
IMON Current Monitor Voltage vs Sense Voltage



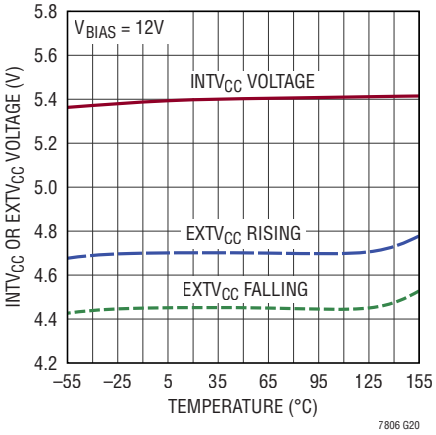
SS Pull-Up Current vs Temperature



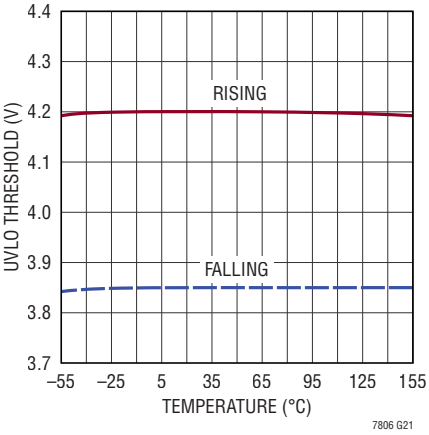
$INTV_{CC}$ Load Regulation



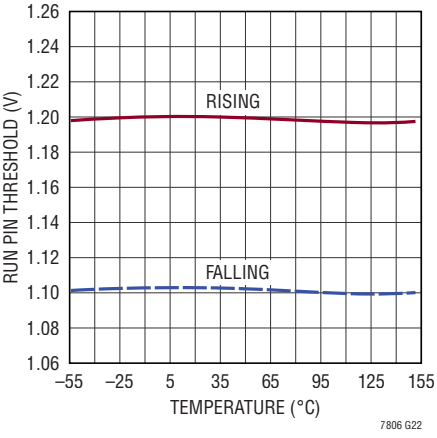
$EXTV_{CC}$ Switchover and $INTV_{CC}$ Voltage vs Temperature



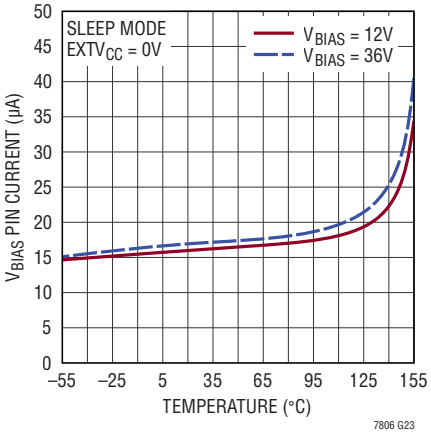
$INTV_{CC}$ Undervoltage Lockout Thresholds vs Temperature



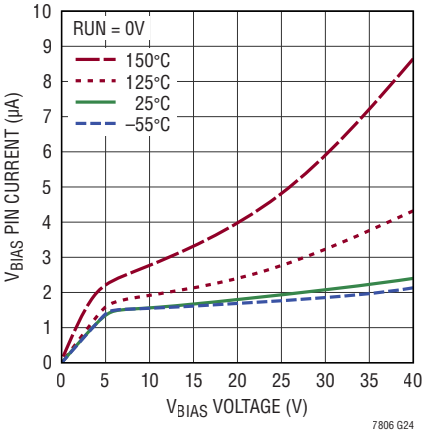
Run Pin Thresholds vs Temperature



V_{BIAS} Quiescent Current vs Temperature



Shutdown Current vs V_{BIAS} Input Voltage



PIN FUNCTIONS

SENSE1$^+$, SENSE2$^+$ (Pins 1, 8): The Positive (+) Input to the Differential Current Comparators. The ITH pin voltage and controlled offsets between the SENSE$^+$ and SENSE$^-$ pins in conjunction with R_{SENSE} set the current trip threshold. The SENSE$^+$ pins supply current to the current comparators when they are greater than $INTV_{CC}$. When SENSE1$^+$ is 3.2V or greater, it also supplies the majority of the sleep mode quiescent current instead of V_{BIAS}.

SENSE1$^-$, SENSE2$^-$ (Pins 2, 7): The Negative (–) Input to the Differential Current Comparators.

FREQ (Pin 3): Frequency Control Pin for the Internal Oscillator. Connect to ground to set the switching frequency to 370kHz. Connect to $INTV_{CC}$ to set the switching frequency to 2.25MHz. Frequencies between 100kHz and 3MHz can be programmed using a resistor between FREQ and ground. Minimize capacitance on this pin.

MODE (Pin 4): Mode Select Input. This input determines how the LTC7806 operates at light loads. Pulling this pin to ground selects Burst Mode operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floating. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to $INTV_{CC}$ through a 100k resistor selects pulse-skipping operation.

RUN (Pin 5): Run Control Input. Forcing this pin below 1.2V disables switching. Forcing the RUN pin below 0.7V shuts down the entire LTC7806, reducing quiescent current to approximately 1.5µA. This pin can be tied to V_{IN} or V_{BIAS} for always-on operation. Do not float the RUN pin.

IMON (Pin 6): Inductor Current Monitor. This pin generates a voltage between 0.4V and 1.4V that corresponds to the channel 2 inductor current between zero current and full load. Optionally place a capacitor from this pin to ground to average the inductor current reading.

ILIM (Pin 9): Current Comparator Sense Voltage Range Input. This pin is used to set the peak current sense voltage in the current comparator. Floating this pin, tying it to ground, or tying it to $INTV_{CC}$ sets the maximum current sense threshold $V_{SENSE(MAX)}$ to one of three different levels (50mV, 25mV, or 75mV, respectively).

VPRG (Pin 10): Output Voltage Programming Pin. This pin sets the output to adjustable output voltage or to a fixed output voltage. Floating this pin allows the output to be programmed through the V_{FB} pin using external resistors, regulating the voltage on V_{FB} to the 1.2V reference. Connecting this pin to GND or $INTV_{CC}$ programs the output to 24V or 28V (respectively) with V_{FB} directly connected to the output.

OVMODE (Pin 11): Overvoltage Mode Selection Input. This pin is used to select how the LTC7806 operates when the output feedback voltage (V_{FB}) is overvoltage (11% above its normal regulation point). When OVMODE is tied to ground, overvoltage protection is enabled and the top MOSFETs are turned on continuously until the overvoltage is cleared. When OVMODE is tied to $INTV_{CC}$, overvoltage protection is disabled and the top MOSFETs are not forced on during an overvoltage event. Instead, the state of the top MOSFETs is determined by the mode of operation selected by the MODE pin and the inductor current. See the Operation section for more details.

When set for Burst Mode operation and synchronized to an external clock through the PLLIN/SPREAD pin, the operating mode changes to pulse-skipping if OVMODE is tied to $INTV_{CC}$ or to forced continuous if OVMODE is grounded.

CLKOUT (Pin 12): Digital Clock Output Used for Daisy-chaining Multiple LTC7806 ICs in Multiphase Systems. The CLKOUT output is phase shifted 90 degrees from the BG1 rising edge. This output swings between $INTV_{CC}$ and ground.

TG2, TG1 (Pins 13, 23): High Current Gate Drives for Top (Synchronous) N-Channel MOSFETs. These are the outputs of floating drivers with a voltage swing of $INTV_{CC}$ superimposed on the switch node voltage SW.

SW2, SW1 (Pins 14, 22): Switch Node Connections to Inductors.

PIN FUNCTIONS

BOOST2, BOOST1 (Pins 15, 21): Bootstrapped Supplies to the Top Side Floating Drivers. Connect capacitors between the corresponding BOOST and SW pins for each channel. Also connect external Schottky diodes between the BOOST pins for each channel and $INTV_{CC}$. Voltage swing at the BOOST pins is from $INTV_{CC}$ to (V_{OUT} + $INTV_{CC}$).

BG2, BG1 (Pins 16, 20): High Current Gate Drives for Bottom N-Channel MOSFETs. Voltage swing at these pins is from GND to $INTV_{CC}$.

$INTV_{CC}$ (Pin 17): Output of the Internal 5.4V Low Dropout Regulator. The driver and control circuits are powered by this supply. Must be decoupled to ground with a minimum of 4.7µF ceramic or tantalum capacitor.

$EXTV_{CC}$ (Pin 18): External Power Input to an Internal LDO Connected to $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power, bypassing the internal LDO powered from V_{BIAS} whenever $EXTV_{CC}$ is higher than 4.65V. See $INTV_{CC}$ Regulators in the Applications Information section. Do not exceed 30V on this pin. Connect this pin to ground if the $EXTV_{CC}$ LDO is not used.

V_{BIAS} (Pin 19): Main Bias Input Supply Pin. A bypass capacitor should be tied between this pin and GND.

PGOOD (Pin 24): Power Good Open-Drain Logic Output. The V_{FB} pin is monitored to ensure that V_{OUT} is in regulation. When V_{OUT} is not within ±11% of its regulation point, the PGOOD pin is pulled low.

PLLIN/SPREAD (Pin 25): External Synchronization Input and Spread Spectrum Enable. When an external clock is applied to this pin, the phase-locked loop will force the rising BG1 signal to be synchronized with the rising edge of the external clock. When an external clock is present, the regulator operates in pulse-skipping mode or forced continuous mode if selected by the MODE pin. When an external clock is present and Burst Mode operation is selected, the OVMODE pin determines how the LTC7806 operates at light load. When not synchronizing to an external clock, tie this input to $INTV_{CC}$ to enable spread spectrum dithering of the oscillator or to ground to disable spread spectrum.

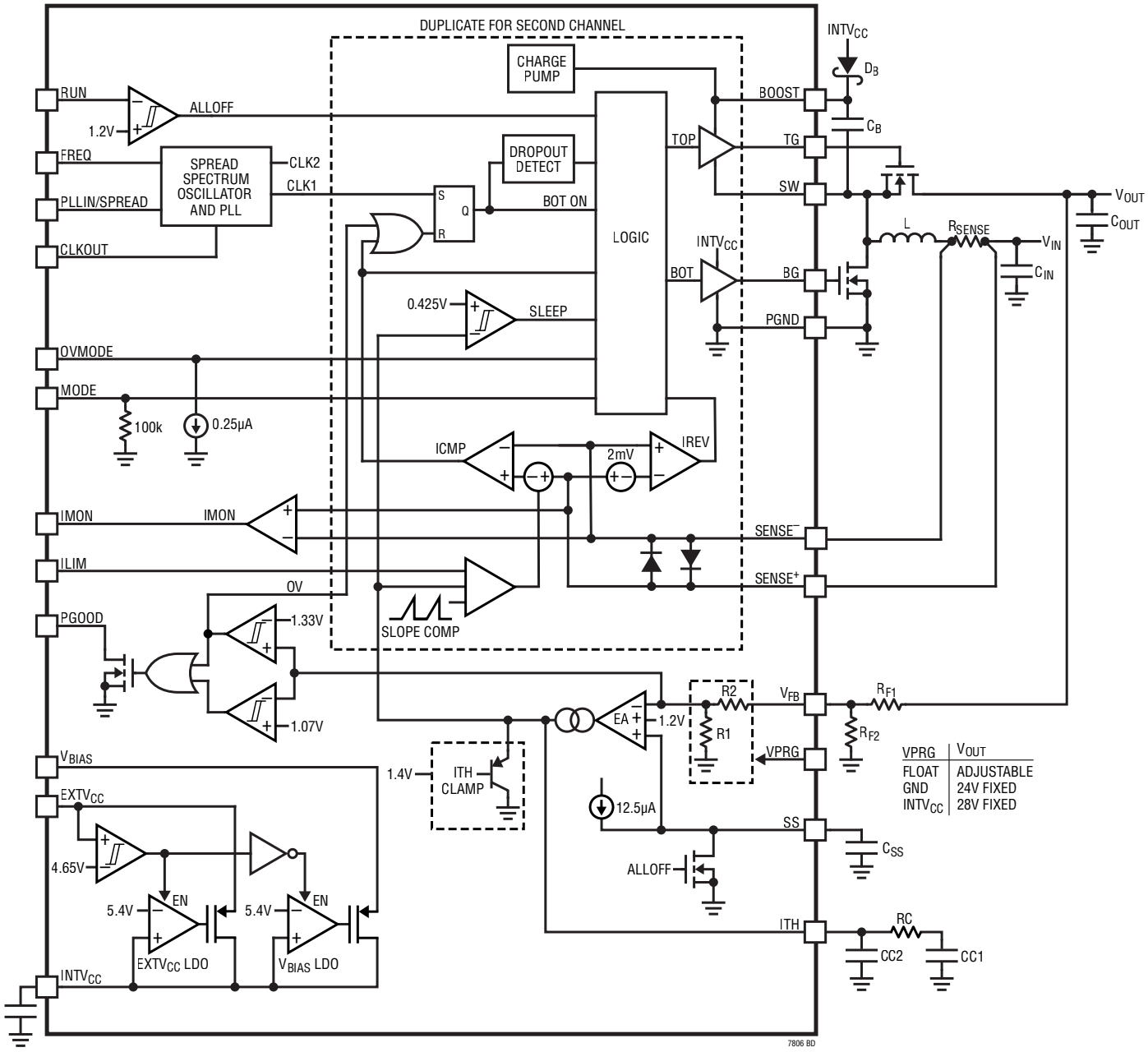
SS (Pin 26): Soft-Start Input. The LTC7806 regulates the negative input to the error amplifier (EA) to the lesser of 1.2V or the voltage on the SS pin. An internal 12.5µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to the final regulated output voltage. The ramp time is equal to 1ms for every 10nF of capacitance.

ITH (Pin 27): Error Amplifier Output and Switching Regulator Compensation Point. The current comparator trip point increases with this control voltage. Place compensation components between the ITH pin and ground.

V_{FB} (Pin 28): Output Voltage Feedback. When VPRG is floating, connect an external resistor divider between the output voltage and the V_{FB} pin to set the regulated output voltage. When VPRG is connected to ground or $INTV_{CC}$, tie V_{FB} directly to the output.

GND (Exposed Pad Pin 29): Signal and Power Ground. The exposed pad must be soldered to PCB ground for rated electrical and thermal performance.

BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC7806 is a synchronous two-phase step-up (boost) controller utilizing a constant-frequency, peak current mode architecture with the two channels operating 180° out-of-phase. During normal operation, the main switch (external bottom MOSFET) is turned on when the clock for that channel sets the SR latch, causing the inductor current to increase. The main switch is turned off when the main current comparator, ICMP, resets the SR latch. After the main switch is turned off each cycle, the synchronous switch (external top MOSFET) is turned on which causes the inductor current to decrease until either the inductor current starts to reverse, as indicated by the current comparator IREV, or the beginning of the next clock cycle.

The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier EA. The error amplifier compares the output voltage feedback signal at the V_{FB} pin, (which is generated with a resistor divider connected across the output voltage, V_{OUT}, to ground) to the internal 1.2V reference. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

Power and Bias Supplies

The $INTV_{CC}$ pin supplies power for the top and bottom MOSFET drivers and most of the internal circuitry. LDOs (low dropout linear regulators) are available from both the V_{BIAS} and $EXTV_{CC}$ pins to provide power to $INTV_{CC}$, which has a regulation point of 5.4V. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 4.65V, the V_{BIAS} LDO supplies power to $INTV_{CC}$. If $EXTV_{CC}$ is taken above 4.65V, the V_{BIAS} LDO is turned off and an $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies power to $INTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source.

Each top MOSFET driver is biased from the floating bootstrap capacitor C_B, which normally recharges when the bottom MOSFET turns on each cycle through an external low-leakage Schottky or PN-junction diode, D_B.

During start-up, if the bottom MOSFET is not turned on within 100µs after the internal UVLO goes low, the bottom MOSFET will be forced to turn on for a cumulative on-time of ~400ns to initially charge the Boost supply. This forced refresh generates enough voltage on the bootstrap capacitor C_B to allow the top MOSFET to be fully enhanced.

During dropout, when V_{IN} increases to a voltage close to V_{OUT} and the top MOSFET is turned on continuously, each channel also has an internal charge pump that maintains bias on the Boost supply. The charge pump always operates in both forced continuous mode and pulse-skipping mode. In Burst Mode operation, the charge pump is turned off during sleep and enabled when the chip wakes up. The internal charge pump can typically supply a charging current of 180µA.

Shutdown and Start-Up (RUN, SS Pins)

The LTC7806 main control loop can be shut down by pulling the RUN pin below 1.1V. Pulling the RUN pin below 0.7V also disables most internal circuits, including the $INTV_{CC}$ LDOs. In this state, the LTC7806 draws only 1.5µA of quiescent current.

When the LTC7806 is shutdown, the top MOSFETs are turned off and the load current flows through their body diodes. Do not apply a heavy load for an extended time while the chip is in shutdown, as this may cause excessive power dissipation in the body diodes.

The RUN pin may either be externally pulled up or driven directly by logic. This pin can tolerate up to 40V (absolute maximum), so it can be conveniently tied to V_{BIAS} or to an input supply in always-on applications where the controller is enabled continuously and never shut down. Additionally, a resistive divider from the input supply to the RUN pin can be used to set a precise input undervoltage lockout so that the power supply does not operate below a user-adjustable level.

OPERATION

The start-up of the controller's output voltage V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 1.2V internal reference, the LTC7806 regulates the V_{FB} voltage to the SS pin voltage instead of the 1.2V reference. This allows the SS pin to be used as a soft-start which smoothly ramps the output voltage on start-up, thereby limiting the input supply inrush current. An external capacitor from the SS pin to GND is charged by an internal 12.5µA pull-up current, creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 1.2V (and beyond), the output voltage V_{OUT} rises smoothly to its final value.

Light Load Operation: Burst Mode Operation, Pulse-Skipping or Forced Continuous Mode (MODE Pin)

The LTC7806 can be set to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode, or forced continuous conduction mode at low load currents.

To select Burst Mode operation, tie the MODE pin to GND. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V. An internal 100k resistor to GND invokes Burst Mode operation when the MODE pin is floating and pulse-skipping mode when the MODE pin is tied to $INTV_{CC}$ through an external 100k resistor.

When the controller is configured for Burst Mode operation, the minimum peak current in the inductor is set to approximately 25% of the maximum even when the voltage on the ITH pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier, EA, decreases the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and all external MOSFETs are turned off. The ITH pin is then disconnected from the output of the EA and parked at 0.45V, and much of the internal circuitry is turned off, reducing the LTC7806's quiescent current to only 18µA.

When Burst Mode operation is selected and $V_{IN} > V_{OUT}$, be aware that the LTC7806 will remain in sleep mode regardless of the load current through the body diodes of the top MOSFETs. These MOSFETs could potentially overheat due to this power dissipation in the body diodes. If large load currents are anticipated when $V_{IN} > V_{OUT}$, either operate the controller in pulse-skipping or forced continuous mode so that the top MOSFETs are enhanced or place a high current Schottky diode in parallel with the top MOSFETs.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the bottom external MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator, IREV, turns off the top external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation.

In forced continuous mode the inductor current is allowed to reverse at light loads or under large transient conditions. The efficiency at light loads is lower than in Burst Mode operation; however, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the inductor current ripple is independent of load current.

When the MODE pin is connected for pulse-skipping mode, the LTC7806 operates in PWM pulse-skipping mode at light loads. In this mode, constant-frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator, ICMP, may remain tripped for several cycles and force the external bottom MOSFET to stay off (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple

OPERATION

as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher light load efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Unlike forced continuous mode and pulse-skipping mode, Burst Mode operation cannot be synchronized to an external clock. Therefore, if Burst Mode operation is selected and the PLLIN/SPREAD pin is clocked to use the phase-locked loop, the LTC7806 switches from Burst Mode to either pulse-skipping (if OVMODE is tied to $INTV_{CC}$) or forced continuous mode (if OVMODE is grounded).

Frequency Selection, Spread Spectrum and Phase-Locked Loop (FREQ and PLLIN/SPREAD Pins)

The free-running switching frequency of the LTC7806 controllers is selected using the FREQ pin. Tying FREQ to GND selects 370kHz while tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 100kHz and 3MHz.

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve EMI, the LTC7806 can operate in spread spectrum mode, which is enabled by tying the PLLIN/SPREAD pin to $INTV_{CC}$. This feature varies the switching frequency within typical boundaries of 0% to +20% greater than the frequency set by the FREQ pin.

A phase-locked loop (PLL) is available on the LTC7806 to synchronize the internal oscillator to an external clock source connected to the PLLIN/SPREAD pin. The LTC7806's PLL aligns the turn-on of controller 1's external bottom MOSFET to the rising edge of the synchronizing signal. Thus, the turn-on of controller 2's external bottom MOSFET is 180° out-of-phase to the rising edge of the external clock source.

The PLL frequency is prebiased to the free-running frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL only needs to make slight changes in order to synchronize the rising edge of the external clock to the rising edge of BG1. For more rapid lock-in to the external clock, use the FREQ pin to set the internal oscillator to approximately the frequency of the external clock. The LTC7806's PLL is guaranteed to lock to an external clock source whose frequency is between 100kHz and 3MHz.

The PLLIN/SPREAD pin is TTL compatible with thresholds of 1.6V (rising) and 1.1V (falling) and is guaranteed to operate with a clock signal swing of 0.5V to 2.2V.

PolyPhase Applications (CLKOUT Pin)

The LTC7806 features a CLKOUT pin that allows another controller IC to be daisy-chained with the LTC7806 in PolyPhase® applications. The clock output signal on the CLKOUT pin can be used to synchronize additional power stages in a multiphase power supply solution feeding a single, high current output or multiple separate outputs. The CLKOUT signal is 90 degrees out-of-phase from the rising edge of the bottom gate driver output of channel 1 (BG1), enabling easy configuration of two LTC7806 controllers to achieve a 4-phase solution with BG rising edge phases of 0°, 90°, 180°, and 270°. CLKOUT is disabled when the controller is in shutdown or in sleep mode.

Overvoltage Mode Selection (OVMODE Pin)

The OVMODE pin is used to select how the LTC7806 operates during an overvoltage event, when the output voltage is greater than 111% of the set regulation point. When OVMODE is tied to ground, overvoltage protection is enabled and the top MOSFETs are turned on continuously until the overvoltage condition is cleared. If the output voltage is greater than the input voltage, this can cause large negative inductor currents to flow from the output to the input supply. Note that in Burst Mode operation, the LTC7806 is in sleep during an overvoltage condition which disables the Boost supply charge pump. The Boost voltage may discharge if the overvoltage conditions persists indefinitely, which turns off the top MOSFETs. When Burst Mode operation is selected and OVMODE is grounded, the LTC7806 operates in forced continuous mode when synchronized to an external clock.

OPERATION

OVMODE should be tied to ground in circuits such as automotive applications where the input voltage can often be above the regulated output voltage and it is desirable to turn on the top MOSFETs to "pass through" the input voltage to the output.

When OVMODE is tied to $INTV_{CC}$, overvoltage protection is disabled and the behavior of the controller when V_{OUT} is overvoltage depends on the selected operating mode. In Burst Mode operation, the LTC7806 goes to sleep and all MOSFETs are turned off. In pulse-skipping mode, the top MOSFETs will turn on if the inductor current is positive. In forced continuous mode, the top and bottom MOSFETs will continue to switch, but with a negative peak current (corresponding to ITH = 0V) which will discharge the output back down to the regulation point. When Burst Mode operation is selected and OVMODE is tied to $INTV_{CC}$, the LTC7806 operates in pulse-skipping mode when synchronized to an external clock.

Operation When V_{IN} > Regulated V_{OUT}

When V_{IN} rises above the regulated V_{OUT} voltage, the boost controller behaves differently depending on the mode, inductor current and V_{IN} voltage. In forced continuous mode, the loop works to keep the top MOSFET on continuously. An internal charge pump delivers current to the boost capacitor from the BOOST pin to maintain a sufficiently high TG voltage.

In pulse-skipping mode, if V_{IN} is between 100% and 111% of the regulated V_{OUT} voltage, TG turns on if the inductor current rises above approximately 8%, 5%, or 3% of the programmed current limit when the ILIM pin is grounded, floating, or tied to $INTV_{CC}$, respectively. If the controller is configured for Burst Mode operation in this same V_{IN} window, then TG remains off regardless of the inductor current.

If the OVMODE pin is grounded and V_{IN} rises enough to pull V_{OUT} above 111% of its regulation point, the controller turns on TG continuously regardless of the inductor current. At this operating point in Burst Mode operation, the controller is asleep and consequently the charge pump is disabled. Therefore, even though the controller is attempting to turn on TG, the boost capacitor may discharge, resulting in an insufficient TG voltage needed to keep the top MOSFET completely on. To prevent excessive power dissipation in the body diode of the top MOSFET in this situation, the chip can be switched over to forced continuous or pulse-skipping mode to enable the charge pump, or a high current Schottky diode can be placed in parallel with the top MOSFET.

Operation at Low Input Voltage

The LTC7806 features a rail-to-rail current comparator which functions down to zero volts. The minimum boost converter input voltage is therefore determined by the practical limitations of the boost converter architecture. Since the input voltage could be lower than the 4.5V V_{BIAS} minimum operating range, V_{BIAS} can be connected to the output of the boost controller, as illustrated on the front page application circuit. This allows the boost controller to handle very low input voltage transients while maintaining output voltage regulation.

Power Good (PGOOD Pin)

The LTC7806 has a PGOOD pin that is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the V_{FB} pin voltage is not within ±11% of its regulation point. The PGOOD pin is also pulled low when the RUN pin is low (shut down). When the output voltage is within the ±11% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source no greater than 6V, such as $INTV_{CC}$.

APPLICATIONS INFORMATION

The Typical Applications on the first page is a basic LTC7806 application circuit. External component selection is largely driven by the load requirement and begins with the selection of the inductor, current sense components, operating frequency, and light load operating mode. The remaining power stage components, consisting of the input and output capacitors, and power MOSFETs can then be chosen. Next, feedback resistors are selected to set the desired output voltage. Then the remaining external components are selected, such as for soft-start, biasing and loop compensation. Note that the two controller channels of the LTC7806 should be designed with the same components.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered. The inductor value has a direct effect on ripple current.

For a boost regulator, the maximum average inductor current in continuous conduction mode is equal to the maximum average output current multiplied by a factor of V_{OUT}/V_{IN}, or $I_{L(MAX)} = I_{OUT(MAX)} \bullet V_{OUT}/V_{IN}$. Be aware that the maximum output current from a boost regulator decreases with decreasing V_{IN}. The choice of $I_{L(MAX)}$ therefore depends on the maximum load current for a regulated V_{OUT} at the minimum normal operating V_{IN}. If the load current for a given V_{IN} is exceeded, V_{OUT} will decrease until the $I_{L(MAX)} = I_{OUT(MAX)} \bullet V_{OUT}/V_{IN}$ equation is satisfied. Additionally, when the output is in overvoltage ($V_{IN} > V_{OUT}$), the top switch is on continuously and the maximum load current is equal to $I_{L(MAX)}$. The inductor ripple current ΔI_L for a boost regulator increases with higher V_{OUT} as given by Equation 1.

$$\Delta I_L = \frac{1}{(f_{OSC})(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

Accepting larger values of ΔI_L allows the use of low inductances but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3 \bullet I_{L(MAX)}$. The maximum ΔI_L occurs at $V_{IN} = V_{OUT}/2$.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency regulators generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate! The inductor saturation design margin should account for the tolerance and temperature effects on the saturation current.

Current Sense Selection

The LTC7806 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and

APPLICATIONS INFORMATION

accuracy. DCR sensing has become popular because it saves expensive current sensing resistors and is generally more power efficient, particularly in high current applications. However, current sensing resistors provide the most accurate current limits for the controller.

The SENSE+ and SENSE– pins are the inputs to the current comparators. The common mode voltage range on these pins is 0V to 40V (absolute maximum), enabling the LTC7806 to regulate from input voltages up to a nominal 36V (allowing margin for tolerances and transients). The SENSE– pins are high impedance, drawing less than ≈1µA. This high impedance allows the current comparators to be used in inductor DCR sensing. The impedance of the SENSE+ pins changes depending on the common mode voltage. When less than $INTV_{CC}$ – 0.5V, these pins are relatively high impedance, drawing ≈2µA. When above $INTV_{CC}$ + 0.5V, a higher current (≈700µA) flows into each pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current. Channel 1's SENSE1+ pin has an additional ≈50µA current when its voltage is above 3.2V to bias internal circuitry from V_{IN} instead of V_{BIAS}, which decreases the quiescent current when V_{BIAS} is connected to the output.

Filter components mutual to the sense lines should be placed close to the LTC7806, and the sense lines should run close together to Kelvin connections underneath the current sense elements (as shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 2b), resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

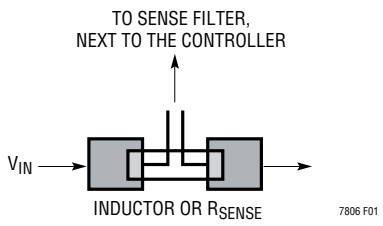


Figure 1. Sense Lines Placement with Inductor or Sense Resistor

The current comparators have a maximum threshold $V_{SENSE(MAX)}$ programmed by the ILIM pin. When the ILIM pin is grounded, floating or tied to $INTV_{CC}$, the maximum threshold is set to 25mV, 50mV or 75mV, respectively. The current comparator threshold sets the peak of the inductor current, yielding a maximum average inductor current, $I_{L(MAX)}$, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. A higher voltage threshold selection gives better current limit and current sharing accuracy, but a lower threshold allows for a smaller, less dissipative current sense resistor, or lower inductor winding losses in the case of DCR current sensing.

Low Value Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 2a. R_{SENSE} is chosen based on the required output current. Using the maximum inductor current $I_{L(MAX)}$ and ripple current ΔI_L from the Inductor Value Calculation section, the target sense resistor value is given by Equation 2.

$$R_{SENSE} \leq \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (2)$$

To ensure that the application will deliver full-load current over the full operating temperature range, choose the minimum value for the selected $V_{SENSE(MAX)}$ range in the in the Electrical Characteristics table and account for tolerances in switching frequency, inductance, and R_{SENSE} resistance. The power rating of the sense resistor should be calculated based on the maximum value for the selected $V_{SENSE(MAX)}$ range.

To avoid potential jitter or instability due to PCB noise coupling into the current sense signal, the AC current sensing ripple of $\Delta V_{SENSE} = \Delta I_L \bullet R_{SENSE}$ should also be checked to ensure a good signal-to-noise ratio. In general, for a reasonably good PCB layout, a target ΔV_{SENSE} AC ripple range of 20% to 40% of $V_{SENSE(MAX)}$ at 50% duty cycle is recommended for both R_{SENSE} and DCR sensing applications.

The parasitic inductance (ESL) of the sense resistor introduces significant error in the current sense signal, particularly for lower inductor value (<3µH) or higher current (>5A) applications. This error may be compensated for

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with an RC filter into the sense pins as shown in Figure 2a. Set the RC filter time constant $R_F \bullet C_F = ESL/R_{SENSE}$ for optimal cancellation of the ESL. Surface mount sense resistors in low ESL wide footprint geometries are recommended to minimize this error. If not specified on the manufacturer's data sheet, the ESL can be approximated as 0.4nH for a resistor with a 1206 footprint and 0.2nH for a 1225 footprint.

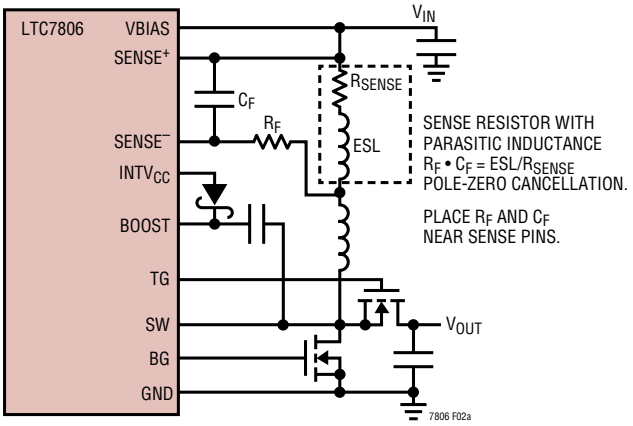
Inductor DCR Current Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC7806 can sense the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor would cost several points of efficiency compared to inductor DCR sensing.

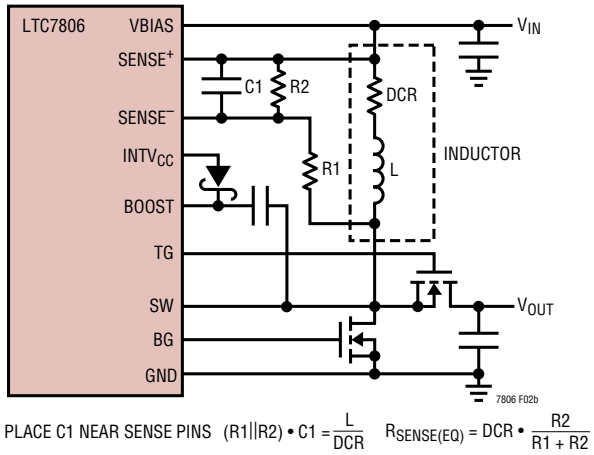
If the external (R1||R2) • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the capacitor C1 is equal to the drop across the inductor DCR multiplied by R2/(R1+R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information. While referred to as DCR, note that the AC resistance of the winding based on the frequency content of the current waveforms is what determines the sense voltage and the resulting current limit behavior. The AC winding resistance is particularly likely to differ from the specified DCR in high frequency (MHz range) designs.

Using the maximum inductor current $I_{L(MAX)}$ and ripple current ΔI_L from the Inductor Value Calculation section, the target sense resistor value is given by Equation 3.

$$R_{SENSE(EQUIV)} \leq \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (3)$$



(a) Using a Resistor to Sense Current



(b) Using the Inductor DCR to Sense Current

Figure 2. Current Sensing Methods

To ensure that the application will deliver full-load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in the Electrical Characteristics table and account for tolerances in switching frequency and inductance.

Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C. To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio given by Equation 4.

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX\ at\ T_{L(MAX)}}} \quad (4)$$

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C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1||R2 to around 2k, reducing error that might have been caused by the SENSE+ pin's ≈1µA current.

The target equivalent resistance R1||R2 is calculated from the nominal inductance, C1 value, and DCR (Equation 5).

$$R1||R2 = \frac{L}{(DCR\ at\ 20°C) \bullet C1} \quad (5)$$

The sense resistor values are given by Equation 6.

$$R1 = \frac{R1||R2}{R_D};\quad R2 = \frac{R1 \bullet R_D}{1 - R_D} \quad (6)$$

The maximum power loss in R1 is related to duty cycle and occurs in continuous mode at $V_{IN} = V_{OUT}/2$ (Equation 7).

$$P_{LOSS}\ R1 = \frac{(V_{OUT(MAX)} - V_{IN}) \bullet V_{IN}}{R1} \quad (7)$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Setting the Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing gate charge and transition losses but requires larger inductance values and/or more output capacitance to maintain low output ripple voltage.

In high output voltage and high frequency applications, transition losses contribute more significantly to power loss, and a good balance between size and efficiency is generally achieved with a switching frequency between 300kHz and 900kHz. Lower output voltage applications benefit from lower switching losses and can therefore more readily operate at higher switching frequencies up to 3MHz if desired.

A further constraint on the operating frequency is the maximum duty cycle. The maximum duty cycle, which can be approximated as $DC_{MAX} \approx (1 - V_{IN(MIN)}/V_{OUT}) \bullet 100\%$, is limited as shown in Figure 3a. At low frequencies, the output will dropout if the required duty cycle is higher than 93%. At high frequencies, the maximum duty cycle available to maintain constant-frequency operation is reduced further. In this region, if a higher duty cycle is required to keep the output voltage in regulation, the controller will skip the top MOSFET turn-on and keep the bottom MOSFET on for more than one clock cycle to achieve the higher duty cycle at an effectively lower frequency. Choose a frequency that limits the maximum duty cycle to a value lower than the curve shown in Figure 3a.

The switching frequency is set using the FREQ and PLLIN/SPREAD pins as shown in Table 1.

Table 1.

FREQ PIN	PLLIN/SPREAD PIN	FREQUENCY
0V	0V	370kHz
$INTV_{CC}$	0V	2.25MHz
Resistor to GND	0V	100kHz to 3MHz
Any of the Above	External Clock 100kHz to 3MHz	Phase-Locked to External Clock
Any of the Above	$INTV_{CC}$	Spread Spectrum Modulated

Tying the FREQ pin to ground selects 370kHz while tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and ground allows the frequency to be programmed anywhere between 100kHz and 3MHz. Choose a FREQ pin resistor from Figure 3b or Equation 8.

$$R_{FREQ}\ (in\ k\Omega) = \frac{37MHz}{f_{OSC}} \quad (8)$$

To improve electromagnetic interference (EMI) performance, spread spectrum mode can optionally be selected by tying the PLLIN/SPREAD pin to $INTV_{CC}$. When spread spectrum is enabled, the switching frequency modulates within 0% to +20% of the frequency selected by the FREQ pin. Spread spectrum may be used in any operating mode selected by the MODE pin (Burst Mode, pulse-skipping, or forced continuous mode).

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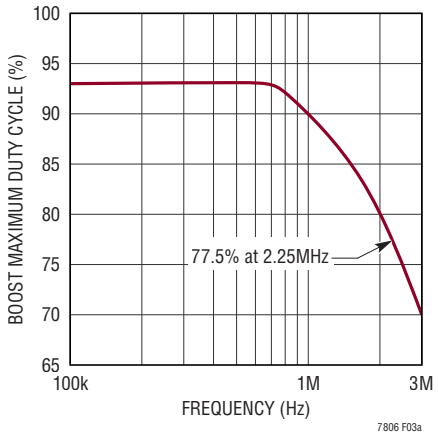
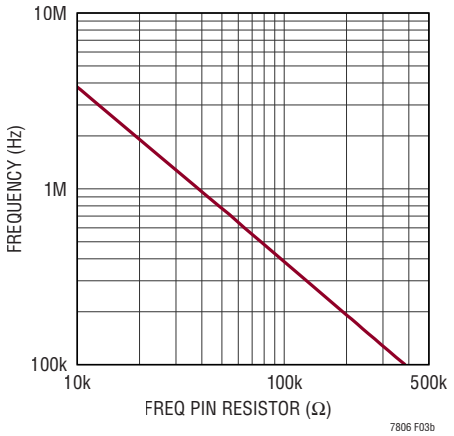


(a) Relationship Between Oscillator Frequency and Maximum Duty Cycle



(b) Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

Figure 3. Setting the Operating Frequency

A phase-locked loop (PLL) is also available on the LTC7806 to synchronize the internal oscillator to an external clock source connected to the PLLIN/SPREAD pin. After the PLL locks, BG1 is synchronized to the rising edge of the external clock signal, and BG2 is 180° out-of-phase from BG1. See the Phase-Locked Loop and Frequency Synchronization section for details.

Selecting the Light Load Operating Mode

The LTC7806 can be set to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode or forced continuous conduction mode at light load currents. To select Burst Mode operation, tie the MODE pin to ground. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to $INTV_{CC}$ through a 100k resistor. An internal 100k resistor from the MODE pin to ground selects Burst Mode operation if the pin is floating. When synchronized to an external clock through the PLLIN/SPREAD pin, the LTC7806 operates in pulse-skipping or forced continuous mode if selected. If Burst Mode operation is selected, the operating mode when synchronized depends on the state of the OVMODE pin. Table 2 summarizes the use of the MODE pin to select the light load operating mode.

Table 2.

MODE PIN	LIGHT LOAD OPERATING MODE	OVMODE PIN	MODE WHEN SYNCHRONIZED
0V	Burst Mode	0V	Forced Continuous
0V	Burst Mode	$INTV_{CC}$	Pulse-Skipping
100k to $INTV_{CC}$	Pulse-Skipping	0V or $INTV_{CC}$	Pulse-Skipping
$INTV_{CC}$	Forced Continuous	0V or $INTV_{CC}$	Forced Continuous

In general, the requirements of each application will dictate the appropriate choice for light load operating mode. In Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator turns off the top MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the regulator operates in discontinuous conduction. In addition, when the load current is very light, the inductor current will begin bursting at frequencies lower than the switching frequency and enter a low current sleep mode when not switching. As a result, Burst Mode operation has the highest possible efficiency at light load.

In forced continuous mode, the inductor current is allowed to reverse at light loads and switches at the same frequency regardless of load. In this mode, the efficiency at light loads is considerably lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the inductor current ripple is independent of load current.

In pulse-skipping mode, constant-frequency operation is maintained down to approximately 5% of the designed maximum output current. At very light loads, the PWM comparator may remain tripped for several cycles and

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force the top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher light load efficiency than forced continuous mode, but not nearly as high as Burst Mode operation. Consequently, pulse-skipping mode represents a compromise between light load efficiency, output ripple and EMI.

In some applications, it may be desirable to change light load operating mode based on the conditions present in the system. For example, if a system is inactive, one might select high efficiency Burst Mode operation by keeping the MODE pin set to 0V. When the system wakes, one might tie MODE to $INTV_{CC}$ to switch to low noise forced continuous mode or send an external clock to PLLIN/SPREAD. Such on-the-fly mode changes can allow an individual application to benefit from the advantages of each light load operating mode.

Power MOSFET Selection

Two external power MOSFETs must be selected for each channel of the LTC7806: one N-channel MOSFET for the bottom (main) switch, and one N-channel MOSFET for the top (synchronous) switch.

The peak-to-peak gate drive levels are set by the $INTV_{CC}$ regulation point of 5.4V. Consequently, logic-level threshold MOSFETs must be used in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode, the duty cycles for the top and bottom MOSFETs are given by Equation 9.

$$\text{MAIN SWITCH DUTY CYCLE} = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$
$$\text{SYNCHRONOUS SWITCH DUTY CYCLE} = \frac{V_{IN}}{V_{OUT}} \quad (9)$$

The MOSFET power dissipations at maximum output current are approximated given by Equation 10.

$$P_{MAIN} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V_{IN}^2}\left(I_{OUT(MAX)}\right)^2(1+\delta) \bullet R_{DS(ON)} + \left(\frac{V_{OUT}^3}{V_{IN}}\right)\left(\frac{I_{OUT(MAX)}}{2}\right) \bullet (R_{DR}+R_G)(C_{MILLER}) \bullet \left(\frac{1}{V_{INTVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right) \bullet f_{OSC}$$
$$P_{SYNC} = \frac{V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)} \quad (10)$$

where δ is the temperature dependency of $R_{DS(ON)}$ ($\delta \approx 0.005/°C$), R_G is the internal gate resistance of the MOSFET, and R_{DR} is the effective driver resistance at the MOSFET's Miller threshold voltage ($R_{DR} \approx 1\Omega$). V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the main N-channel equation includes an additional term for transition losses, which are highest at high output voltages. For $V_{OUT} < 20V$ and moderate switching frequencies, the high current efficiency generally improves with larger MOSFETs, while for $V_{OUT} > 20V$ the transition losses rapidly increase to the $(R_{DR} + R_G)$ point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the synchronous switch is on for up to 100% of the period.

C_{IN} and C_{OUT} Selection

The C_{IN} and C_{OUT} requirements for the LTC7806 are reduced by the two-phase architecture and its impact on the worst-case input and output ripple voltages and currents.

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The input ripple current in a boost converter is relatively low (compared to the output ripple current) because this current is continuous. The boost input capacitor C_{IN} voltage rating should comfortably exceed the maximum input voltage. Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of C_{IN} is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

The output current in a boost converter is discontinuous, so C_{OUT} should be selected to meet output voltage ripple requirements. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady-state peak-to-peak ripple due to charging and discharging the bulk capacitance of C_{OUT} in a single-phase boost converter is given by Equation 11.

$$\Delta V_C = \frac{V_{IN} \bullet (I_{L(MAX)} - I_{OUT(MAX)})}{V_{OUT} \bullet C_{OUT} \bullet f_{OSC}} \quad (11)$$

The peak-to-peak ripple due to the voltage drop across the ESR is given by Equation 12.

$$\Delta V_{ESR} = \left(I_{L(MAX)} + \frac{1}{2}\Delta I_L \right) \bullet ESR \quad (12)$$

The LTC7806 is configured as a 2-phase single output converter where the outputs of the two channels are connected together and both channels have the same duty cycle. With 2-phase operation, the two channels are operated 180 degrees out-of-phase. This effectively interleaves the output capacitor current pulses, greatly reducing the output capacitor ripple current. As a result, the capacitance and/or ESR requirement of the high frequency output capacitor can be relaxed for a given output ripple voltage requirement.

The previous Equation 11 and Equation 12 for ripple voltage also apply for more than one phase if $I_{OUT(MAX)}$ is taken as the total output current for the system, and the duty cycle is high enough to avoid overlapping output current pulses, or $D > (1–1/N_{PH})$ where N_{PH} is the phase count, which is true at $V_{IN(MIN)}$ for most applications.

Because the ripple current in the output capacitor is a square wave, the ripple current requirements for the output capacitor depends on the duty cycle, the number of phases and the maximum output current. Figure 4 illustrates the normalized output capacitor ripple current as a function of duty cycle in a 2-phase configuration. To choose a ripple current rating for the output capacitor, first establish the duty cycle range based on the output voltage and range of input voltage. Referring to Figure 4, choose the worst-case high normalized ripple current as a percentage of the maximum load current.

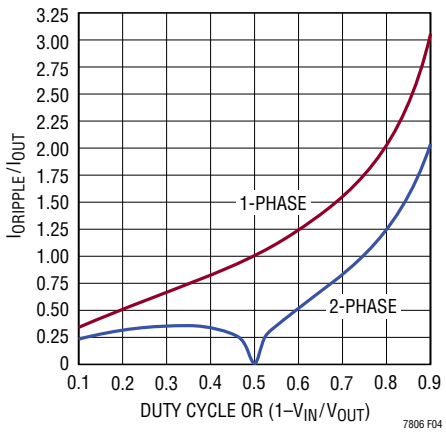

Figure 4. Normalized Output Capacitor Ripple Current (RMS) for a Boost Converter

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings such as OS-CON and POSCAP.

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PolyPhase Operation

For output loads that demand very high current, multiple LTC7806s can be cascaded to run out-of-phase to provide more output current and at the same time to reduce input and output voltage ripple. The PLLIN/SPREAD pin allows the LTC7806 to synchronize to the frequency and phase of the CLKOUT signal of another LTC7806 or to some other external clock signal. As shown in Figure 5, for a 4-phase system, the CLKOUT signal, which is 90 degrees out of phase from the BG1 rising edge, can be connected to the PLLIN/SPREAD pin of the following LTC7806 stage to set both the frequency and the phase of each channel of the entire system to further improve on the ripple reduction shown in Figure 4. For higher phase counts, external clock signals can be generated with the requisite phase differences and fed into the PLLIN/SPREAD pins of multiple LTC7806s.

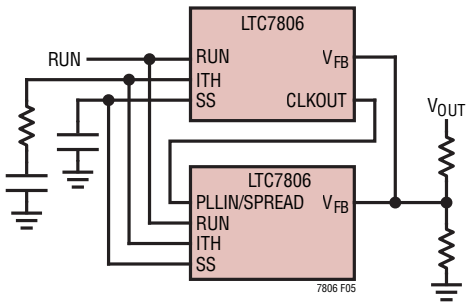


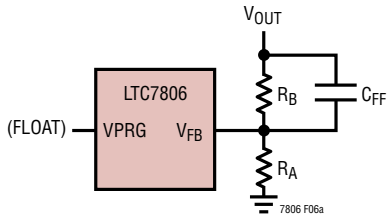
Figure 5. Configuration for a 4-Phase System

Setting the Output Voltage

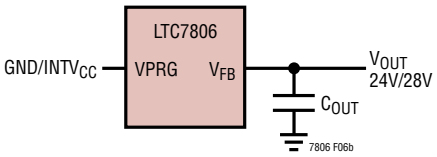
The VPRG pin selects whether the controller output voltage is set by an external feedback resistor divider or programmed to a fixed 24V or 28V output. Floating VPRG allows the boost output voltage to be set by an external feedback resistor divider as shown in Figure 6a. The regulated output voltage is then determined by Equation 13.

$$V_{OUT(BOOST)} = 1.2V\left(1+\frac{R_B}{R_A}\right) \quad (13)$$

Tying the VPRG to GND or $INTV_{CC}$ configures the boost controller for a fixed output voltage of 24V or 28V, respectively. As shown in Figure 6b, directly connect the V_{FB} pin to the output when configured for a fixed output voltage.



(a) Setting Boost Output Using External Resistors



(b) Setting Boost to Fixed 24V/28V Output

Figure 6. Setting Boost Output Voltage

Place resistors R_A and R_B very close to the V_{FB} pin to minimize PCB trace length and noise on the sensitive V_{FB} node. Great care should be taken to route the V_{FB} trace away from noise sources, such as the inductor or the SW trace. To improve frequency response, a feedforward capacitor (C_{FF}) may be used.

RUN Pin and Undervoltage Lockout

The LTC7806 is enabled using the RUN pin, which has a rising threshold of 1.2V with 100mV of hysteresis. Pulling the RUN pin below 1.1V shuts down the main control loop. Pulling it below 0.7V disables the controller and most internal circuits, including the $INTV_{CC}$ LDOs. In this state, the LTC7806 draws only ≈1.5µA of quiescent current.

The RUN pin is high impedance and must be externally pulled up/down or driven directly by logic. The RUN pin can tolerate up to 40V (abs max), so it can be conveniently tied to V_{IN} or V_{BIAS} in always-on applications where the controller is enabled continuously and never shut down. Do not float the RUN pin.

The RUN pin can be configured as a precise UVLO by connecting it to the output of an external resistor divider network off V_{IN}, as shown in Figure 7.

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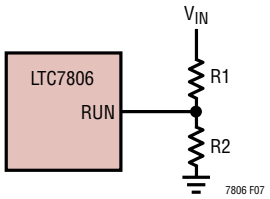

Figure 7. Using the RUN Pin as a UVLO

The rising and falling UVLO thresholds are calculated using the RUN pin thresholds given by Equation 14.

$$V_{UVLO(RISING)} = 1.2V\left(1+\frac{R_1}{R_2}\right)$$
$$V_{UVLO(FALLING)} = 1.1V\left(1+\frac{R_1}{R_2}\right) \quad (14)$$

For applications that do not require a precise UVLO the RUN pin can be tied to V_{IN} or V_{BIAS}. In this configuration, the UVLO threshold is limited to the internal $INTV_{CC}$ UVLO threshold as shown in the Electrical Characteristics table.

The current that flows through the R1–R2 divider directly adds to the shutdown, sleep, and active current of the LTC7806, and care should be taken to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the megohm range may be required to keep the impact on quiescent shutdown and sleep currents low.

Soft-Start

The start-up of V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is lower than the internal 1.2V reference, the LTC7806 regulates the feedback voltage to the voltage on the SS pin instead of 1.2V. Soft-start is configured by simply connecting a capacitor from the SS pin to ground. An internal 12.5µA current source charges the capacitor, providing a linear ramping voltage at the SS pin. The LTC7806 will regulate the feedback voltage (and hence V_{OUT}) according to the voltage on the SS pin, allowing V_{OUT} to rise smoothly to its final regulated value. For a desired soft-start time, t_{SS}, select a soft-start capacitor $C_{SS} = t_{SS} \bullet 10\mu F/sec$.

$INTV_{CC}$ Regulators

The LTC7806 features two separate internal P-channel low dropout linear regulators (LDOs) that supply power at the $INTV_{CC}$ pin from either the V_{BIAS} pin or the $EXTV_{CC}$ pin depending on the $EXTV_{CC}$ pin voltage. $INTV_{CC}$ powers the MOSFET gate drivers and much of the LTC7806's internal circuitry. The V_{BIAS} LDO and the $EXTV_{CC}$ LDO each regulate $INTV_{CC}$ to 5.4V and can provide a peak current of at least 100mA.

The $INTV_{CC}$ pin must be bypassed to ground with a minimum of 4.7µF ceramic capacitor, placed as close as possible to the pin. An additional 1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and GND pins is also highly recommended to supply the high frequency transient currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC7806 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the V_{BIAS} LDO or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than 4.8V, the V_{BIAS} LDO is enabled. Power dissipation for the IC in this case is equal to $V_{BIAS} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the LTC7806 $INTV_{CC}$ current is limited to less than 35.5mA from a 36V supply when not using the $EXTV_{CC}$ supply at a 70°C ambient temperature given by Equation 15.

$$T_J = 70°C + (35.5mA)(36V)(43°C/W) = 125°C \quad (15)$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in forced continuous mode (MODE = $INTV_{CC}$) at maximum V_{BIAS}.

When the voltage applied to $EXTV_{CC}$ rises above 4.8V, the V_{BIAS} LDO is turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above approximately 4.5V. The $EXTV_{CC}$ LDO attempts to regulate the $INTV_{CC}$ voltage

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to 5.4V, so while $EXTV_{CC}$ is less than 5.4V, the LDO is in dropout and the $INTV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than 5.4V (up to an absolute maximum of 30V), $INTV_{CC}$ is regulated to 5.4V.

Significant thermal gains can be realized by powering $INTV_{CC}$ from an external supply, and efficiency is also improved if the external supply is derived from another switching regulator. This is accomplished by tying the $EXTV_{CC}$ pin directly to an external supply that is greater than the $INTV_{CC}$ regulation point. Tying the $EXTV_{CC}$ pin to an 8.5V supply reduces the junction temperature in Equation 15 from 125°C to 83°C given by Equation 16.

$$T_J = 70°C + (35.5mA)(36V)(43°C/W) = 83°C \quad (16)$$

The following list summarizes the three possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This will cause $INTV_{CC}$ to be powered from the internal V_{BIAS} LDO resulting in an efficiency penalty of up to 10% or more at high V_{BIAS} voltages.
2. $EXTV_{CC}$ connected directly to V_{IN}. This can be used if V_{BIAS} is tied to V_{OUT} and the maximum V_{IN} voltage is 30V or less. This approach allows the regulator to ride through very low input voltage conditions (V_{IN} < 4.5V) and provides significant thermal benefit when V_{IN} > 4.8V.
3. $EXTV_{CC}$ connected to an external supply. This can be used if an external supply compatible with the MOSFET gate drive requirements is available in the 5V to 30V range. This supply may be higher or lower than V_{BIAS}; however, a lower $EXTV_{CC}$ voltage results in higher efficiency.

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors C_B connected to the BOOST pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Block Diagram is charged through external diode D_B from $INTV_{CC}$ when the SW pin is low. Individual Kelvin connections from each of the external diodes to the $INTV_{CC}$ bypass capacitor are recommended to prevent the high currents required to charge the Boost capacitors from injecting noise into other analog signals.

When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{OUT} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the output voltage: $V_{BOOST} = V_{OUT} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). For typical applications, a suitable value of C_B is in the 0.1µF to 0.47µF range.

The external diode D_B can be a Schottky diode or silicon diode, but in either case it should have low leakage and fast recovery. The reverse breakdown of the diode must be greater than $V_{OUT(MAX)}$. Pay close attention to the reverse leakage at high temperatures where it generally increases substantially.

A leaky diode not only increases the quiescent current of the boost converter, but it can create a current path from the BOOST pin to $INTV_{CC}$. This will cause $INTV_{CC}$ to rise if the diode leakage exceeds the current consumption on $INTV_{CC}$, which is primarily a concern in Burst Mode operation where the load on $INTV_{CC}$ can be very small. There is an internal voltage clamp on $INTV_{CC}$ that prevents the $INTV_{CC}$ voltage from running away, but this clamp should be regarded as a failsafe only.

Each topside MOSFET driver includes an internal charge pump that delivers current to the bootstrap capacitor from the BOOST pin. This current maintains the bias voltage required to keep the top MOSFET on continuously during dropout/overvoltage conditions. In applications supporting dropout or overvoltage conditions, the Schottky or PN-junction diode selected for the topside driver should have a reverse leakage less than the available output current the charge pump can supply. Curves displaying the available charge pump current under different operating conditions can be found in the Typical Performance Characteristics section.

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest duration that the LTC7806 is capable of turning on the bottom MOSFET. It is determined by internal timing delays and the gate charge required to turn on the bottom MOSFET. Low duty

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cycle applications may approach this minimum on-time limit and care should be taken to ensure Equation 17.

$$t_{ON(MIN)} < \frac{V_{OUT} - V_{IN}}{V_{OUT} \bullet f_{OSC}} \quad (17)$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase. The minimum on-time for the LTC7806 is approximately 105ns. However, as the peak sense voltage decreases the minimum on-time gradually increases up to about 150ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Current Monitor (IMON)

The channel 2 inductor current can be monitored at the IMON pin. This pin generates a voltage that represents a scaled and filtered version of the inductor current sensed through the SENSE2$^+$ and SENSE2$^-$ pins. The DC voltage on IMON normally varies between 0.4V and 1.4V, corresponding to a sensed inductor current I_L between 0% and 100% of the maximum designed inductor current as given by Equation 18.

$$V_{IMON} = 1V \bullet \frac{I_L \bullet R_{SENSE}}{V_{SENSE(MAX)}} + 0.4V \quad (18)$$

The IMON voltage may momentarily be less than 0.4V or greater than 1.4V, but eventually is limited to these levels by the current loop. When the controller is in sleep, this pin is held at 0.4V. An internal 30k resistor is in series with the IMON buffer to facilitate filtering of the sensed inductor current ripple. Place a capacitor from IMON to ground to filter the ripple and achieve an average current measurement over multiple switching cycles.

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self-heating (such as a heavy load from $INTV_{CC}$ to ground) internal overtemperature shutdown circuitry will shut down the LTC7806. When the internal die temperature exceeds 180°C, the $INTV_{CC}$ LDO and gate drivers are disabled. When the die cools to 160°C, the LTC7806 enables the $INTV_{CC}$ LDO and resumes operation beginning with a soft-start start-up. Long-term overstress (T_J > 125°C) should be avoided as it can degrade the performance or shorten the life of the part.

Phase-Locked Loop and Frequency Synchronization

The LTC7806 has an internal phase-locked loop (PLL) which allows the turn-on of the bottom MOSFET of controller 1 to be synchronized to the rising edge of an external clock signal applied to the PLLIN/SPREAD pin. The turn on of controller 2's bottom MOSFET is thus 180° out-of-phase with the external clock.

Rapid phase-locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. Before synchronization, the PLL is prebiased to the frequency set by the FREQ pin. Consequently, the PLL only needs to make minor adjustments to achieve phase-lock and synchronization. Although it is not required that the free-running frequency be near the external clock frequency, doing so will prevent the oscillator from passing through a large range of frequencies as the PLL locks.

Unlike forced continuous mode and pulse-skipping mode, Burst Mode operation cannot be synchronized to an external clock. Therefore, if Burst Mode operation is selected, the LTC7806 switches from Burst Mode operation to either pulse-skipping (if OVMODE is tied to $INTV_{CC}$) or forced continuous mode (if OVMODE is grounded) when the PLL is used. The LTC7806 is guaranteed to synchronize to an external clock applied to the PLLIN/SPREAD pin that swings up to at least 2.2V and down to 0.5V or less. Note that the LTC7806 can only be synchronized to an external clock frequency within the range of 100kHz to 3MHz.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine

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what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed by using Equation 19.

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...) \quad (19)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC7806 circuits: 1) IC V_{BIAS} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) bottom MOSFET transition losses.

1. The V_{BIAS} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. Other than at very light loads in Burst Mode operation, V_{BIAS} current typically results in a small (<0.1%) loss.
2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f_{SW} (Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the top and bottom MOSFETs.
3. I^2R losses are predicted from the DC resistances of the input fuse (if used), MOSFET, inductor, current sense resistor, and input and output capacitor ESR. These losses cause the efficiency to drop at high output currents.
4. Transition losses apply only to the bottom MOSFET and become significant only when operating at higher output voltages (typically 20V or greater). Transition losses can be estimated from the equation for the main switch power dissipation in the Power MOSFET Selection section.

Other hidden losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. The LTC7806 2-phase architecture typically halves this input capacitance requirement over competing solutions. Other losses including inductor core losses generally account for less than 2% total additional loss but can be significant when operating at high switching frequencies.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} • (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem.

OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC coupled and AC filtered closed loop response test point. The DC step rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the Typical Application circuits provide an adequate starting point for most applications.

The ITH series R_C–C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their initial values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been

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determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately C_{LOAD} • 25µs/µF. Thus, a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume V_{IN} = 12V (nominal), V_{IN} = 8V (min) to 20V (max), V_{OUT} = 24V, I_{MAX} = 8A ($I_{OUT(MAX)}$ = 4A per phase), $V_{SENSE(MAX)}$ = 50mV and f = 1MHz.

The frequency is not one of the internal preset values, so a resistor from the FREQ pin to GND is required, with a value given by Equation 20.

$$R_{FREQ} = \frac{37MHz}{1MHz} = 37k\Omega \quad (20)$$

Most of the design analysis is based on operation of a single-phase carrying half of the current. The inductance value is chosen based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. The minimum inductance for 30% ripple current is given by Equation 21.

$$L = \frac{V_{IN}}{(f)(\Delta I_L)}\left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (21)$$

The largest ripple occurs when V_{IN} = V_{OUT}/2 = 12V, where the average maximum inductor current is $I_{L(MAX)}$ = $I_{OUT(MAX)}$ • (V_{OUT}/V_{IN}) = 8A.

A 2.4µH inductor will produce 31% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 9.25A.

The minimum on-time occurs at maximum V_{IN} given by Equation 22.

$$t_{ON(MIN)} = \frac{V_{OUT} - V_{IN(MAX)}}{V_{OUT}(f)} = \frac{4V}{24V(1MHz)} = 167ns \quad (22)$$

The equivalent R_{SENSE} resistor value can be calculated by using the minimum value for the selected maximum current sense threshold (50mV) given by Equation 23.

$$R_{SENSE} \le \frac{44mV}{9.25A} \approx 0.004\Omega \quad (23)$$

To allow for additional margin, a lower value R_{SENSE} may be used; however, be sure that the inductor saturation current has sufficient margin above $V_{SENSE(MAX)}$/R_{SENSE}, where the maximum value of 55mV is used for $V_{SENSE(MAX)}$.

For an adjustable output setting (VPRG floating), choose 1% feedback resistors R_A = 11.3k and R_B = 215k for an output voltage of 24.032V; however, since 24V is one of the fixed output settings, VPRG can alternatively be

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grounded with V_{FB} connected directly to V_{OUT}. This not only saves component cost, but also reduces the quiescent current due to the V_{FB} feedback divider.

The best way to evaluate MOSFET performance in a particular application is to build and test the circuit on the bench, facilitated by an LTC7806 demo board. However, an educated guess about the application is helpful to initially select MOSFETs. Transition losses will likely dominate over I^2R losses for the bottom MOSFET. Therefore, choose a MOSFET with higher $R_{DS(ON)}$ and lower gate charge to minimize the combined loss terms. The top MOSFET does not experience transition losses, and its power loss is generally dominated by I^2R losses. For this reason, the top MOSFET is typically chosen to be of lower $R_{DS(ON)}$ and subsequently higher gate charge than the bottom MOSFET. Be sure to select logic-level threshold MOSFETs, since the gate drive voltage is limited to 5.4V ($INTV_{CC}$).

C_{OUT} is chosen to filter the square current in the output and must be rated to support the resulting high RMS current. The maximum peak and RMS output capacitor current occurs at the minimum input voltage. Use the curve in Figure 4 with a duty cycle of $D = (1 – V_{IN(MIN)}/V_{OUT})$ to estimate the RMS current that the output capacitors need to absorb. In this example, D = 0.66 and the output ripple current from Figure 4 is approximately 0.75 • 8A = 6A. Two pieces (1 per phase) of 10µF 1210 50V X5R or similar capacitors would be rated to handle this RMS current, and would have a net ESR of 0.0025Ω. The capacitance of these parts decreases by about 50% due to DC bias, giving a net capacitance of 10µF.

In calculating the output ripple voltage, use Equation 11 and Equation 12 given in the C_{IN} and C_{OUT} Selection section to calculate 133mV of capacitive ripple and 18mV of ripple from the ESR. The peaks of the two ripple components are not quite aligned, but a conservative approach would be to add them together. An additional capacitor might be added to meet transient requirements. A tantalum, polymer or aluminum polymer hybrid capacitor would usually be a good choice for the bulk capacitor to provide high capacitance with reasonably low ESR.

The input capacitor needs to absorb the inductor ripple current, which has a maximum RMS value of 0.72A at V_{IN} = 12V. A small ceramic capacitor such as a 4.7uF X5R 0805 or similar capacitor could absorb this. Alternatively, a higher-grade electrolytic capacitor might carry a sufficient ripple current rating and would be more likely to meet any damping needs arising from inductive wiring or interconnect supplying power to the boost regulator.

For a 10ms soft-start, select a 0.1µF capacitor for the SS pin. As a first pass estimate for the bias components, select C_{INTVCC} = 4.7µF, boost supply capacitor C_B = 0.1µF. The TG gate drive voltage (relative to SW) should be around 4.5V ~ 5V. If it is too low, increase C_B or use a boost diode with a lower forward voltage drop, keeping in mind the reverse leakage current trade-off typical of Schottky diodes.

Determine and set application-specific parameters. Set the MODE pin based on the trade-off of light load efficiency and constant-frequency operation. Set the PLLIN/SPREAD pin based on whether a fixed, spread spectrum, or phase-locked frequency is desired. The RUN pin can be used to control the minimum input voltage for regulator operation or can be tied to V_{IN} for always-on operation. Use ITH compensation components from the typical applications as a first guess, check the transient response for stability, and modify as necessary.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. Figure 8 illustrates the current waveforms present in the various branches of the 2-phase synchronous boost regulator operating in the continuous mode. Check the following in your layout:

1. Put the bottom N-channel MOSFETs and the top N-channel MOSFETs in one compact area with C_{OUT}.
2. Are the signal and power grounds kept separate? The combined IC ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The area of the loop formed by the top N-channel

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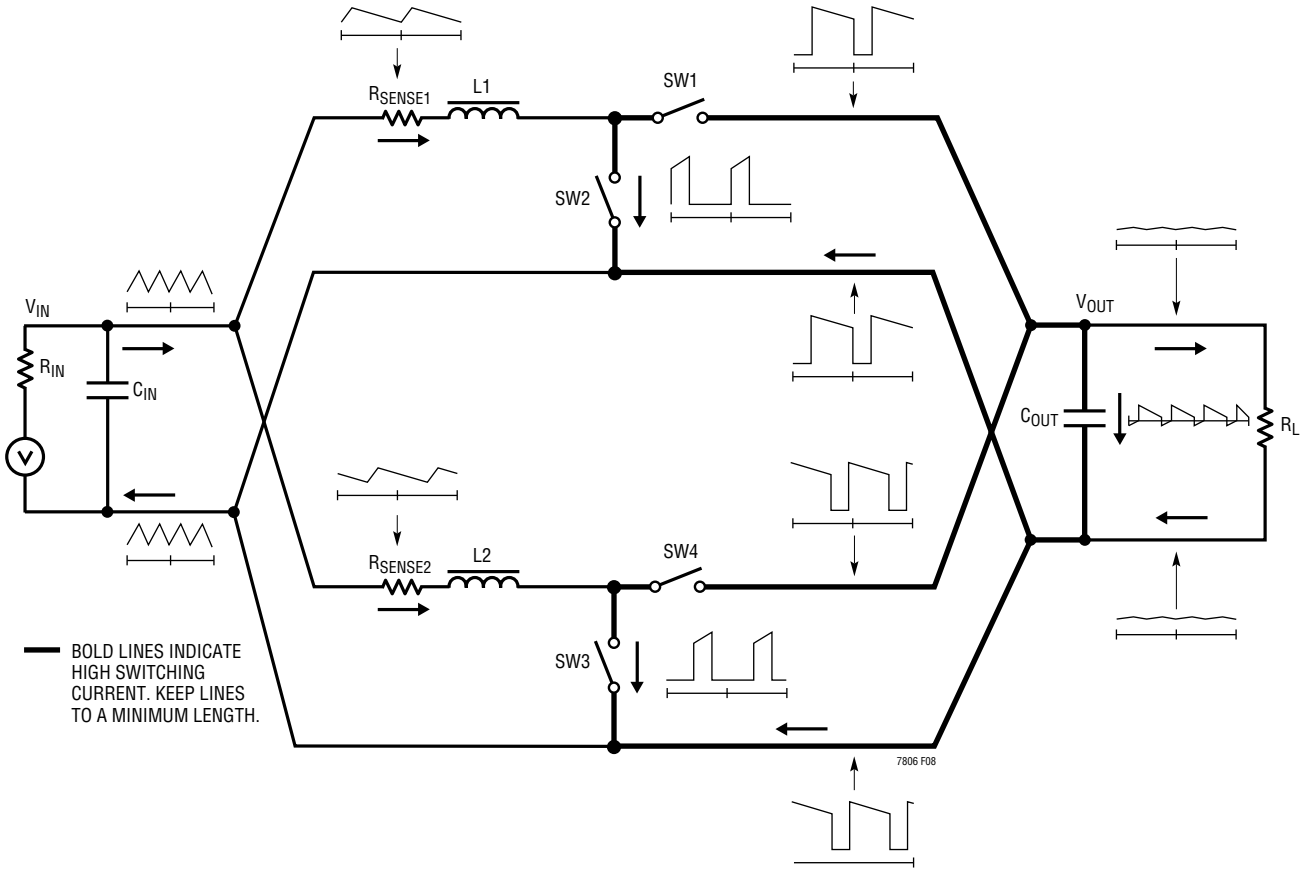

Figure 8. Branch Current Waveforms

MOSFET, bottom N-channel MOSFET and the high frequency (ceramic) C_{OUT} capacitor(s) should be minimized with short leads, planar connections and multiple paralleled vias.

3. Do the LTC7806 V_{FB} pins' resistive dividers connect to the (+) terminals of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground. Place the divider close to the V_{FB} pin to minimize noise coupling into the sensitive V_{FB} node. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).

4. Are the $SENSE^+$ and $SENSE^-$ leads routed together with minimum PC trace spacing? Route these traces away from the high frequency switching nodes, on an inner layer if possible. The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.

5. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ pin and power ground? This capacitor carries the MOSFET drivers' current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and GND pins can help improve noise performance substantially. Use individual Kelvin connections from the $INTV_{CC}$ bypass capacitor to each of the external Boost supply diodes to prevent the high currents that charge the Boost capacitors from injecting noise into other analog signals.

6. Keep the switching nodes (SW1, SW2), top gate nodes (TG1, TG2), boost nodes (BOOST1, BOOST2), and bottom gate nodes (BG1, BG2) away from sensitive small-signal nodes, especially from the voltage feedback and current sensing pins. All of these nodes have very large and fast-moving signals and therefore should be kept on the output side of the LTC7806 and occupy minimum external-layer PC trace area. Minimize the loop inductance of the TG and BG gate

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drive traces and their respective return paths to the controller IC (SW and GND) by using wide traces and multiple parallel vias.

7. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the GND pin of the IC.

PC Board Layout Debugging

It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 25% of the maximum designed current level in Burst Mode operation.

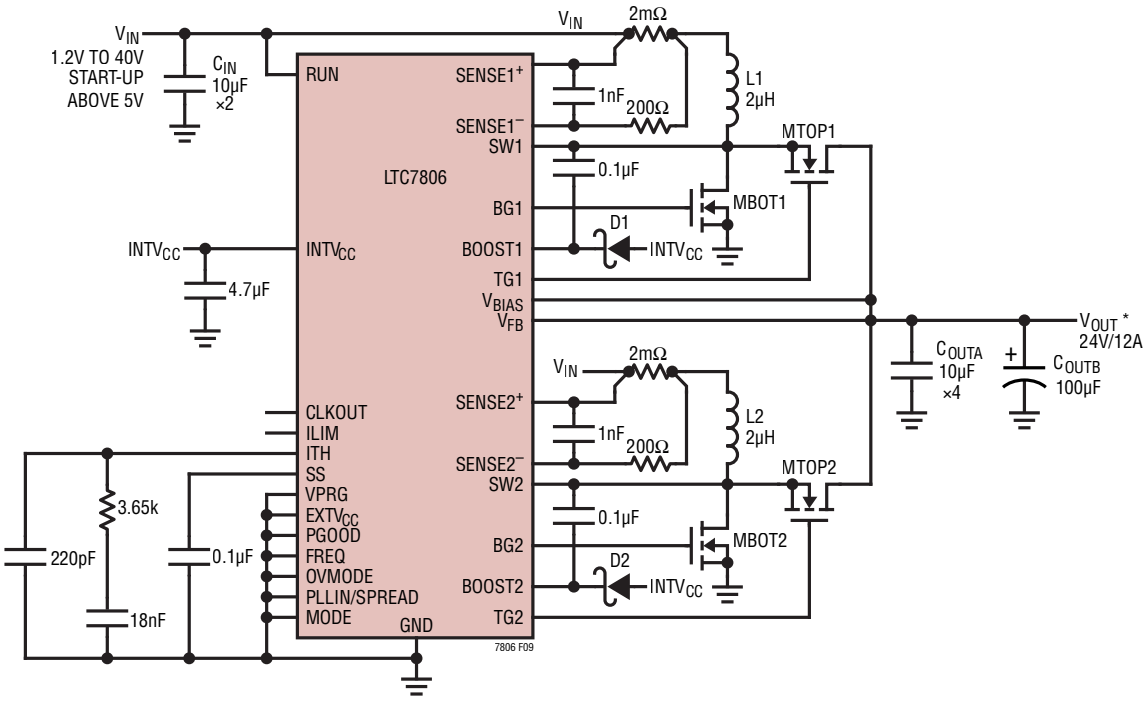
The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point when the other channel is turning on its bottom MOSFET. This occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation. Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins.

The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{OUT}, the top MOSFET, and the bottom MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

TYPICAL APPLICATIONS

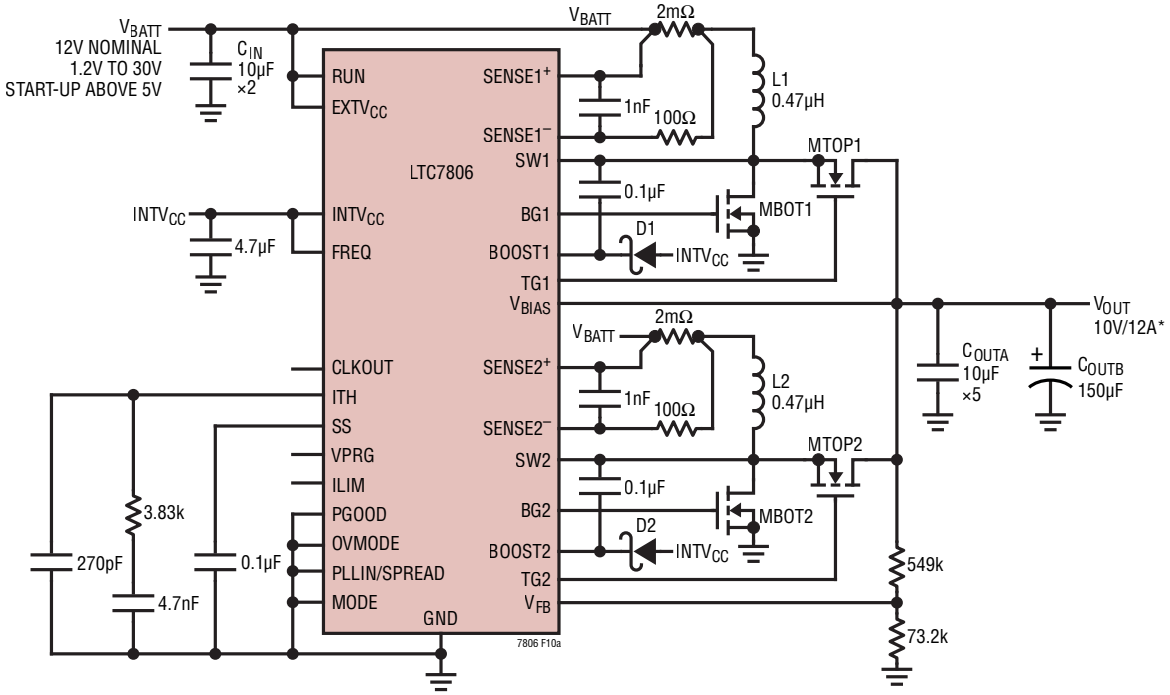


C_{IN}, C_{OUTA}: MURATA GCM32EC71H106KA03
C_{OUTB}: SUNCON 63HVPF100M
D1,2: INFINEON BAS140W
L1,2: COILCRAFT SER2011-202MLD
MBOT1,2, MTOP1,2: INFINEON BSC059N04LS6

f_{SW} = 370kHz
*WHEN V_{IN} > 24V, V_{OUT} FOLLOWS V_{IN}
*WHEN V_{IN} < 9V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED

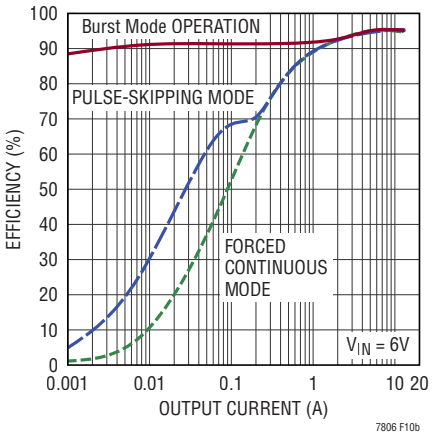
Figure 9. High Efficiency 24V, 12A Boost Regulator

TYPICAL APPLICATIONS

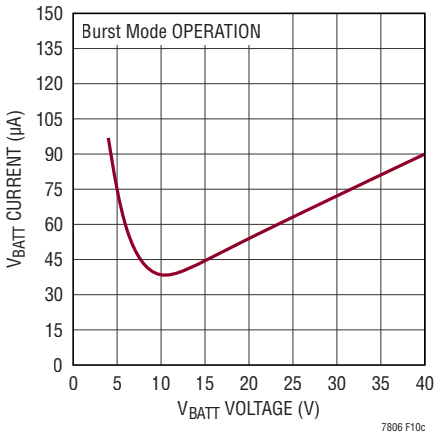


C_{IN}, C_{OUTA}: MURATA GCM32EC71H106KA03
C_{OUTB}: SUNCON 50HVPF150M
D1,2: INFINEON BAS140W
L1,2: WURTH 744355047
MBOT1,2, MTOP1,2: INFINEON BSC059N04LS6

f_{SW} = 2.25MHz
*WHEN V_{BATT} > 10V, V_{OUT} FOLLOWS V_{BATT}
WHEN V_{BATT} < 4.5V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED



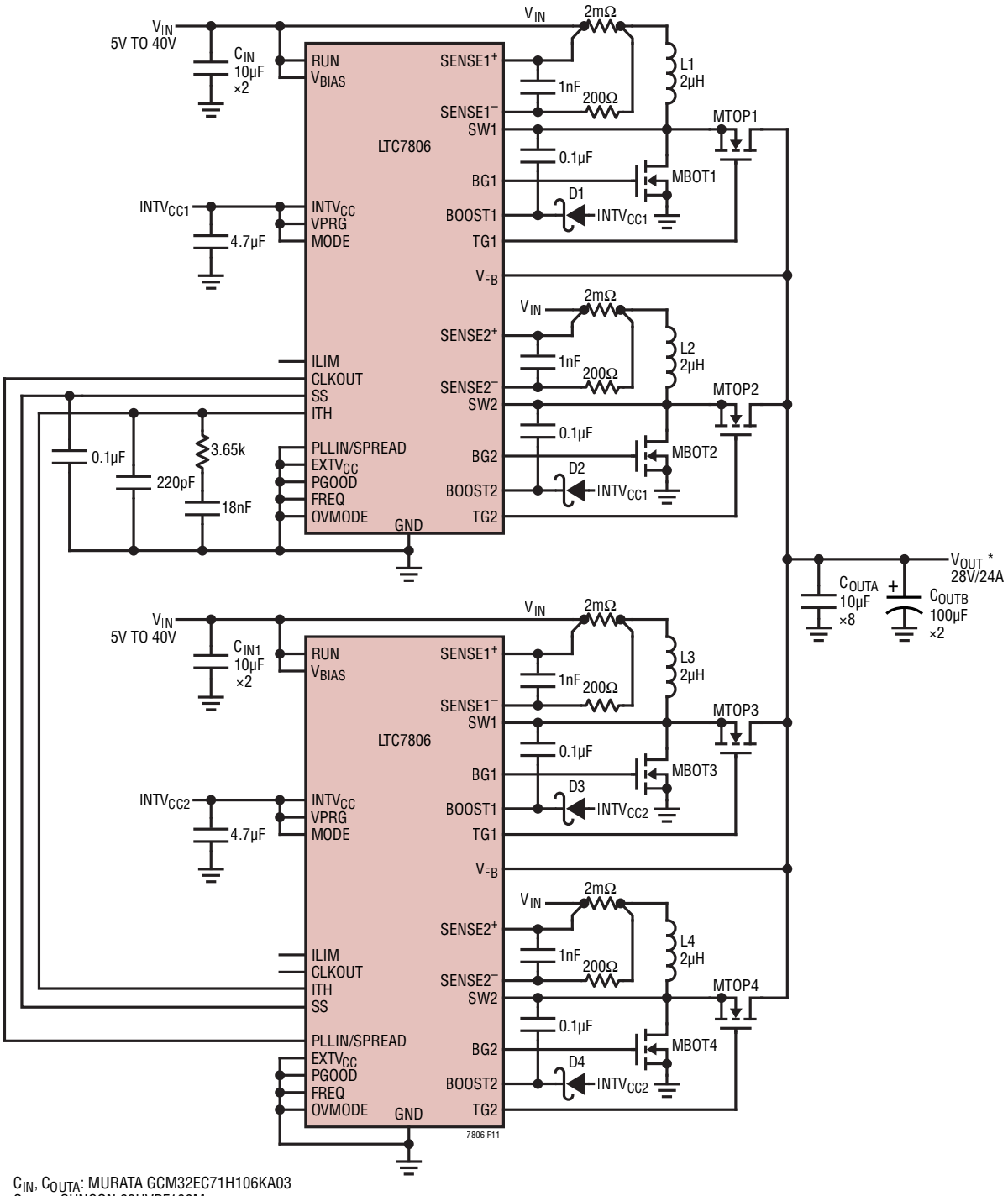
(b) Efficiency vs Load Current



(c) No-Load Burst Mode Input Current vs Input Voltage

Figure 10. High Efficiency 2.25MHz, Automotive PassThru Pre-Boost Regulator

TYPICAL APPLICATIONS

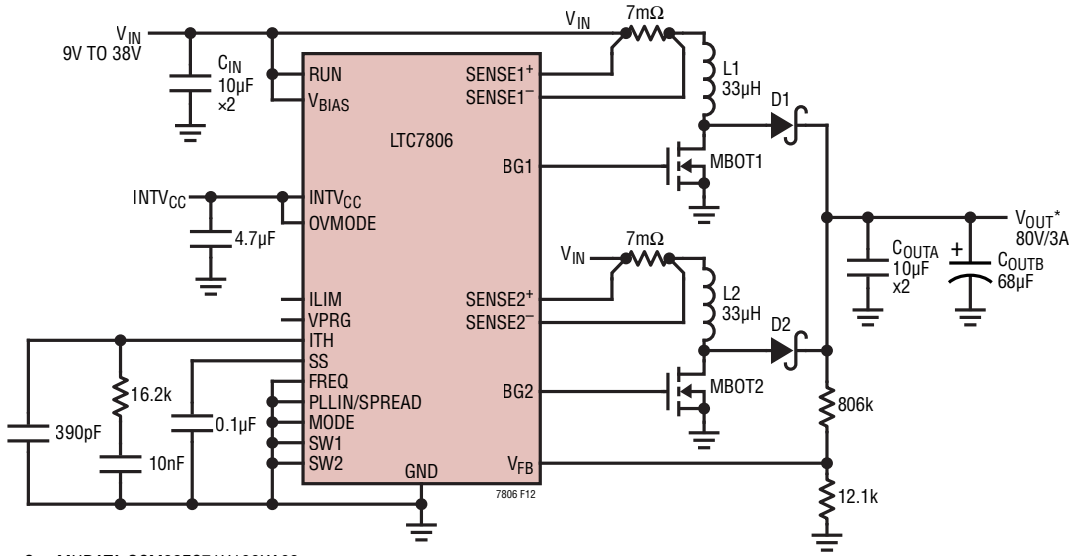


C_{IN}, C_{OUTA}: MURATA GCM32EC71H106KA03
C_{OUTB}: SUNCON 63HVPF100M
D1,2,3,4: INFINEON BAS140W
L1,2,3,4: COILCRAFT SER2011-202MLD
MBOT1,2,3,4, MTOP1,2,3,4: INFINEON BSC059N04LS6

f_{SW} = 370kHz
*WHEN V_{IN} > 24V, V_{OUT} FOLLOWS V_{IN}
*WHEN V_{IN} < 9V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED

Figure 11. 4-Phase 28V/672W Boost Regulator

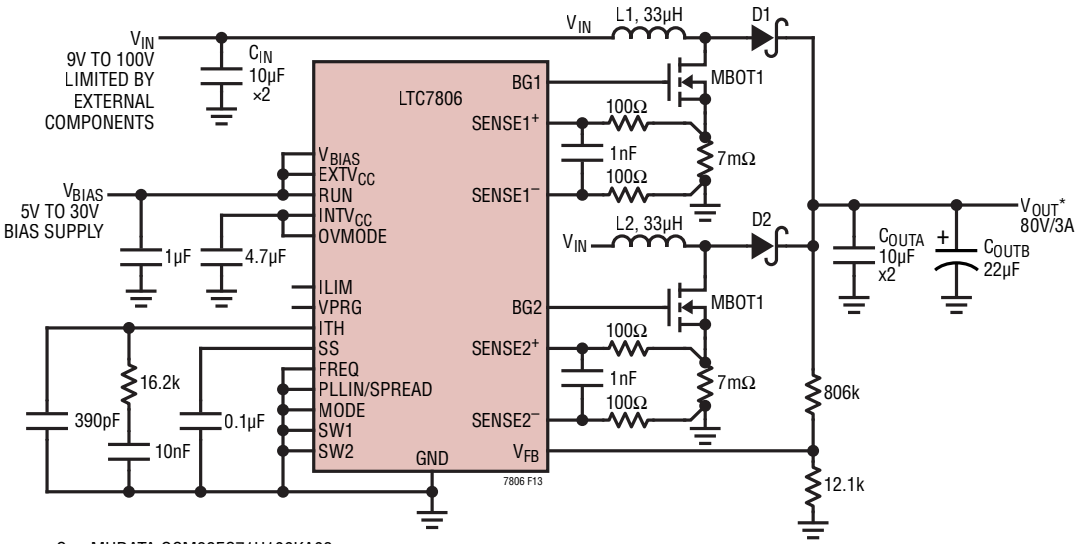
TYPICAL APPLICATIONS



C_{IN}: MURATA GCM32EC71H106KA03
C_{OUTA}: TDK C5750X7S2A106K230KE
C_{OUTB}: SUNCON100CE68LX
D1,2: VISHAY VS-12CWQ10FN-M3
L1,2: COILCRAFT XAL1510-333MEB
MBOT1,2: INFINEON BSC159N10LSF-G

f_{SW} = 370kHz
PINS NOT USED IN THIS CIRCUIT: $EXTV_{CC}$, BOOST1, BOOST2, TG1, TG2, PGOOD, CLKOUT
*WHEN V_{IN} < 24V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED

Figure 12. Low I_Q Nonsynchronous 80V/240W Boost Regulator



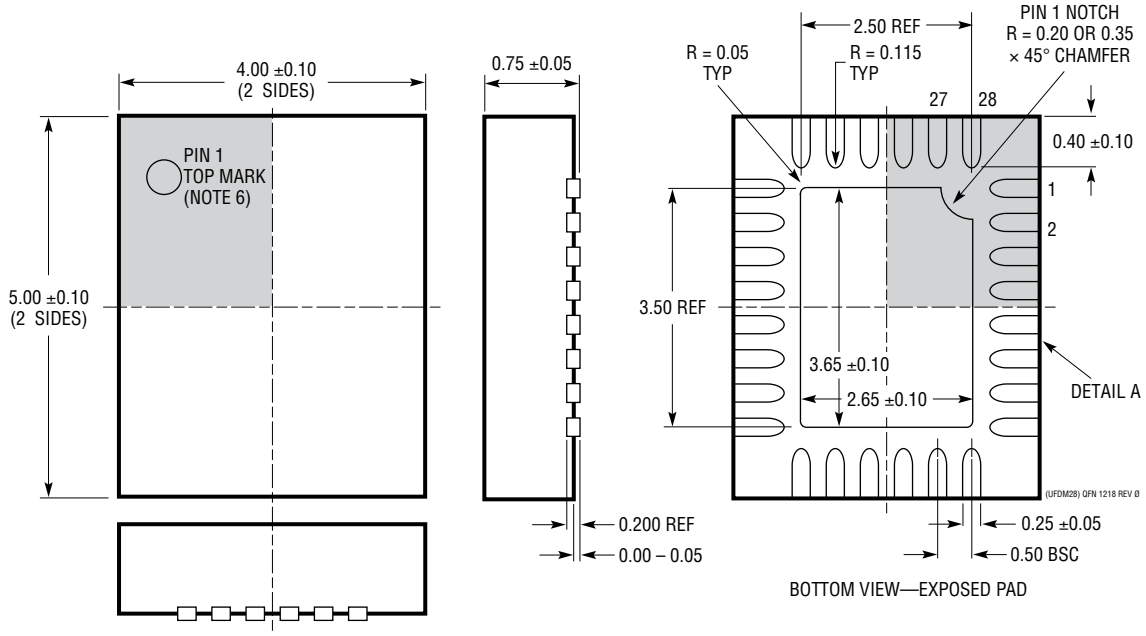
C_{IN}: MURATA GCM32EC71H106KA03
C_{OUTA}: TDK C5750X7S2A106K230KE
C_{OUTB}: SUNCON100CE68LX
D1,2: VISHAY VS-12CWQ10FN-M3
L1,2: COILCRAFT XAL1510-333MEB
MBOT1,2: INFINEON BSC159N10LSF-G

f_{SW} = 370kHz
PINS NOT USED IN THIS CIRCUIT: BOOST1, BOOST2, TG1, TG2, PGOOD, CLKOUT
*WHEN V_{IN} < 24V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED
*WHEN V_{IN} > 80V, V_{OUT} FOLLOWS V_{IN}

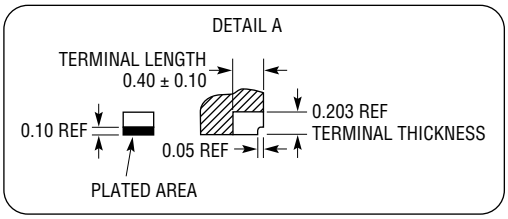
Figure 13. Low I_Q Nonsynchronous 80V/240W Boost Regulator with Extended V_{IN} Range

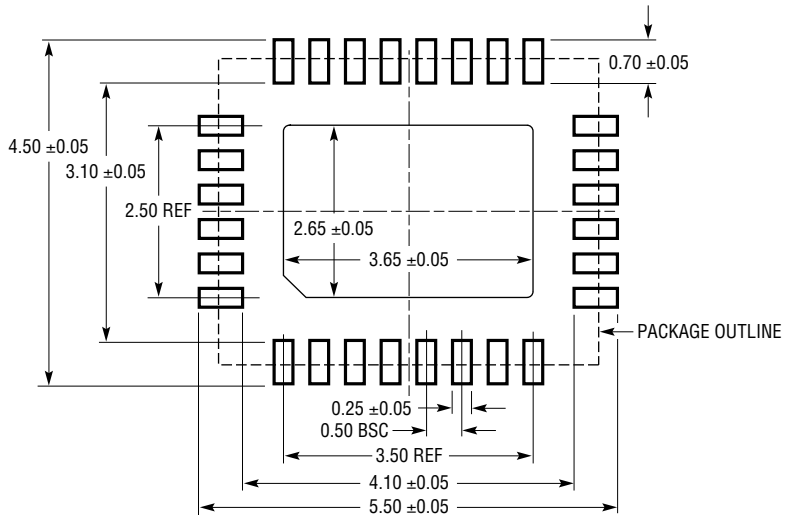
PACKAGE DESCRIPTION

UFDM Package
28-Lead Plastic Side Wettable QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1682 Rev Ø)



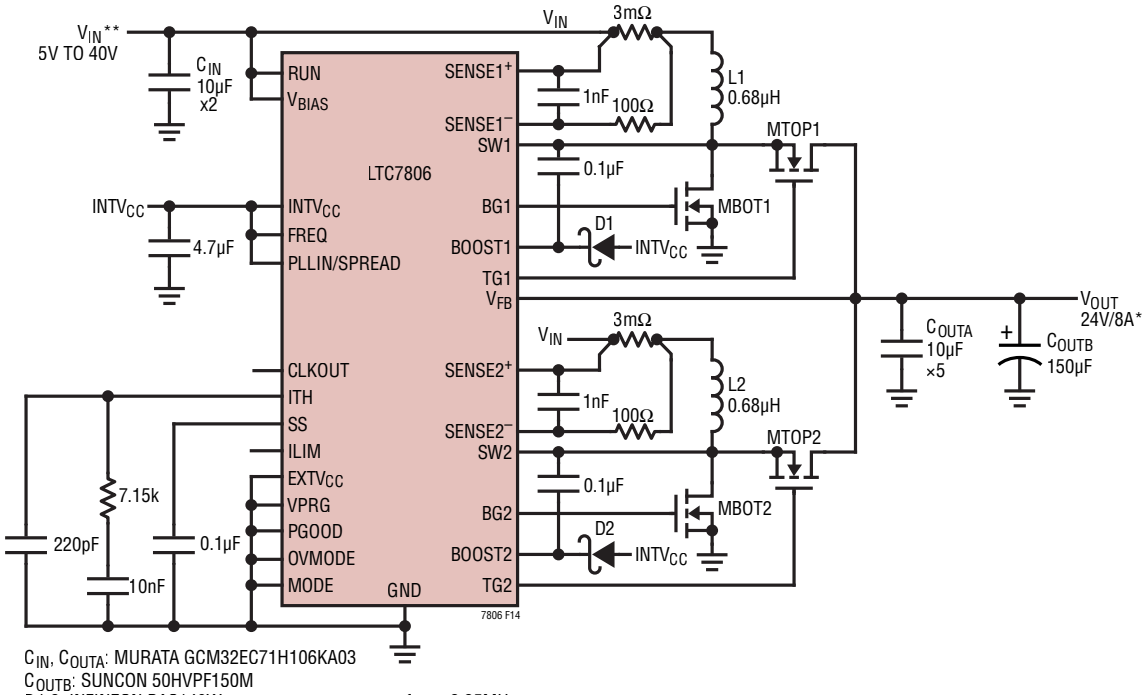
NOTE:
1. DRAWING NOT TO SCALE
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE





RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

TYPICAL APPLICATION



CIN, COUTA: MURATA GCM32EC71H106KA03
COUTB: SUNCON 50HVPF150M
D1,2: INFINEON BAS140W
L1,2: WURTH 7443330068
MBOT1,2, MTOP1,2: INFINEON BSC059N04LS6

f_{SW} = 2.25MHz
*WHEN V_{IN} < 8V, MAXIMUM LOAD CURRENT AVAILABLE IS DERATED BY INPUT CURRENT LIMIT
**CONSTANT FREQUENCY OPERATION WHEN V_{IN} > 6V

Figure 14. High Efficiency 2.25MHz, 24V Boost Regulator with Spread Spectrum

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7804	38V Low I_Q, 3MHz Multiphase Synchronous Boost Controller with PassThru	4.5V ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 100kHz to 3MHz Fixed Operating Frequency, 3mm × 3mm QFN-16
LTC7818	40V, Low I_Q, 3MHz, Triple Output Buck/Buck/Boost Synchronous Controller with Spread Spectrum	4.5V ≤ V_{IN} ≤ 40V, I_Q = 14µA, 100% Duty Cycle Capable Boost, Buck and Boost V_{OUT} Up to 40V, PLL Fixed Frequency 100kHz to 3MHz
LTC3787	38V Single Output, Low I_Q Multiphase Synchronous Boost Controller with PassThru	4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHZ to 900kHz Fixed Operating Frequency, 4mm × 5mm QFN-28, SSOP-28
LTC3788/ LTC3788-1	38V Dual Output, Low I_Q Multiphase Synchronous Boost Controller with PassThru	4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHZ to 900kHz Fixed Operating Frequency, 5mm × 5mm QFN-32, SSOP-28
LTC3786	38V Low I_Q Synchronous Step-Up Controller with PassThru	4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHZ to 900kHz Fixed Operating Frequency, 3mm × 3mm QFN-16, MSOP-16E
LTC3769	60V Low I_Q Synchronous Boost Controller with PassThru	4.5V (Down to 2.3V After Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, 50kHZ to 900kHz Fixed Operating Frequency, 4mm × 4mm QFN-24, TSSOP-20
LTC3784	60V Single Output, Low I_Q Multiphase Synchronous Boost Controller with PassThru	4.5V (Down to 2.3V After Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, 50kHZ to 900kHz Fixed Operating Frequency, 4mm × 5mm QFN-28, SSOP-28
LTC3897	PolyPhase Synchronous Boost Controller with Input/ Output Protection	4.5V ≤ V_{IN} ≤ 65V, 5V to 10V Gate Drive, 100kHz to 750kHz Fixed Operating Frequency, TSSOP-38, 5mm × 7mm QFN-38
LTC3862/ LTC3862-1	Single Output, Multiphase Current Mode Step-Up DC/DC Controller	4V ≤ V_{IN} ≤ 36V, 5V or 10V Gate Drive, 75kHz to 500kHz Fixed Operating Frequency, SSOP-24, TSSOP-24, 5mm × 5mm QFN-24