## DEMO MANUAL DC2249B

## LTM4622 <br> Ultrathin Dual 2.5A Step-Down $\mu$ Module Regulator

## DESCRIPTION

Demonstration circuit 2249B features the LTM ${ }^{\circledR} 4622$ $\mu$ Module ${ }^{\circledR}$ regulator, a tiny low profile high performance high efficiency dual step-down regulator. The LTM4622 has an operating input voltage range of 3.6 V to 20 V and is able to provide an output current of up to 2.5 A for each channel. Each output's voltage is programmable from 0.6 V to 5.5 V . The LTM4622 is a complete DC-DC point of load regulator in a low profile thermally enhanced $6.25 \mathrm{~mm} \times$ $6.25 \mathrm{~mm} \times 1.82 \mathrm{~mm}$ LGA package requiring only a few input and output capacitors. Output voltage tracking is available
through the TRACK/SS pin for supply rail sequencing. External clock synchronization is available through the SYNC/MODE pin. For high efficiency at low load currents the MODE pin jumper (JP3) selects the Burst Mode ${ }^{\circledR}$ option for operation in less noise sensitive applications. The LTM4622 data sheet must be read in conjunction with this demo manual for working on or modifying demo circuit 2249B.

Design files for this circuit board are available.
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## PERFORMARCE SUMmARY

Specifications are at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| PARAMETER | CONDITIONS | VALUE |
| :---: | :---: | :---: |
| Input Voltage Range |  | 4 V to 20V |
| Output Voltage $\mathrm{V}_{\text {OUT1 }}, \mathrm{V}_{\text {OUT2 }}$ | Programmable with FB Pin Resistors | $3.3 \mathrm{~V}_{D C}, 1.2 \mathrm{~V}_{D C}$ |
| Maximum Continuous Output Current Each Phase | Derating is Necessary for Certain Operating Conditions. See Data Sheet for Details | $2.5 \mathrm{~A}_{\text {DC }}$ |
| Default Operating Frequency |  | 1MHz |
| Efficiency | $\begin{aligned} & V_{\text {IN }}=12 \mathrm{~V}, V_{\text {OUT1 }}=3.3 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=2.5 \mathrm{~A}, \mathrm{f}_{\text {SW }}=2 \mathrm{MHz} \\ & \mathrm{~V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{~V}_{\text {OUT2 }}=1.2 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=2.5 \mathrm{~A}, \mathrm{f}_{\text {SW }}=1 \mathrm{MHz} \end{aligned}$ | 87.5\%. See Figure 2 <br> $76.7 \%$. See Figure 2 |

## BOARD PHOTO



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## QUICK START PROCEDURE

Demonstration circuit 2249B is an easy way to evaluate the performance of the LTM4622. Please refer to Figure 1 for test setup connections and follow the procedure below.

1. With power off, place the jumpers in the following positions for a typical application for $3.3 \mathrm{~V}_{\text {OUT }}$ and $1.2 \mathrm{~V}_{\text {OUT }}$ rails:

| JP1 | JP2 | JP3 |
| :---: | :---: | :---: |
| RUN1 | RUN2 | MODE |
| ON | ON | CCM |

2. Before powering up the input supply and loads, preset the input voltage supply to be between 4 V to 20V. Preset the load current for each output rail to OA.
3. With power off, connect the loads, input voltage supply and meters as shown in Figure 1.
4. Turn on the input power supply. The output voltage meters for each output rail should display the programmed output voltage $\pm 2 \%$.
5. Once the proper output voltages are established, adjust the load current on each rail within the 0 A to 2.5 A range and observe each output rail's load regulation, efficiency, and other parameters.
6. To observe increased light load efficiency place the mode pin jumper (JP3) in the BURST position.
Note: Demonstration circuit 2249B is designed to exhibit the wide output voltage range of the LTM4622. In order to keep inductor current ripple within reasonable limits it is recommended to increase programmed switching frequency for higher output voltages. The programmed switching frequency for data provided in this manual is consistent with switching frequency recommendations corresponding to the programmed output voltage. Please refer to the LTM4622 data sheet for more details regarding recommended switching frequency for your particular application.

## PUICK START PROCEDURE



Figure 1. Test Setup

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## PUICK START PROCEDURE



Figure 2. Measured Supply Efficiency at $12 \mathrm{~V}_{\text {IN }}$ and $5 \mathrm{~V}_{\text {IN }}$

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## PUICK START PROCEDURE



| $\mathrm{V}_{\text {IN }}(\mathrm{V})$ | $\mathrm{V}_{\text {OUT }}(\mathrm{V})$ | $\mathrm{C}_{\text {OUT }}$ |
| :---: | :---: | :---: |
| 12 | 1.2 | $1 \times 22 \mu \mathrm{~F}+1 \times 47 \mu \mathrm{~F}$ |



Figure 3. Measured Load Transient Response (1A to 2A Load Step)
Figure 4. Measured Load Transient Response (1A to 2A Load Step)


| $\mathrm{V}_{\text {IN }}(\mathrm{V})$ | $\mathrm{V}_{\text {OUT1 }}(\mathrm{V}), \mathrm{I}_{\text {OUT1 }}(\mathrm{A})$ | $\mathrm{V}_{\text {OUT2 }}(\mathrm{V}), \mathrm{I}_{\text {OUT2 }}(\mathrm{A})$ | $\mathrm{f}_{\text {SW }}(\mathrm{MHz})$ | $\mathrm{T}_{\text {AMBIENT }}\left({ }^{\circ} \mathrm{C}\right)$ |
| :---: | :---: | :---: | :---: | :---: |
| 12 | $3.3,2.5$ | $1.2,2.5$ | 2 | 22 |

Figure 5. Thermal Capture at Full Load Natural Convection

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## PARTS UST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
| :---: | :---: | :--- | :--- | :--- |
| Required Circuit Components |  |  |  |  |
| 1 | 1 | C1 | CAP, X5R, $2.2 \mu \mathrm{~F}, 10 \mathrm{~V}, 10 \%, 0603$ | MURATA, GRM188R61A225KE34D |
| 2 | 2 | C3, C13 | CAP, X5R, $22 \mu \mathrm{~F}, 25 \mathrm{~V}, 20 \%, 0805$ | MURATA, GRM21BR61E226ME-44L |
| 3 | 2 | C16, C29 | CAP, X5R, $22 \mu \mathrm{~F}, 6.3 \mathrm{~V}, 20 \%, 0805$ | MURATA, GRM21BR60J226ME39L |
| 4 | 2 | C20, C23 | CAP, X5R, 47 $\mu \mathrm{F}, 6.3 \mathrm{~V}, 20 \%, 1206$ | MURATA, GRM31CR60J476ME19L |
| 5 | 2 | C21, C24 | CAP, X5R, $0.1 \mu \mathrm{~F}, 25 \mathrm{~V}, 10 \%, 0603$ | MURATA, GRM188R61E104KA01D |
| 6 | 1 | R11 | RES, CHIP, $60.4 \mathrm{k}, 1 / 16 \mathrm{~W}, 1 \%, 0603$ | VISHAY, CRCW060360K4FKEA |
| 7 | 1 | R20 | RES, CHIP, $13.3 \mathrm{k}, 1 / 16 \mathrm{~W}, 1 \%, 0603$ | VISHAY, CRCW060313K3FKEA |
| 8 | 1 | U1 | IC, LTM4622EV, LGA $25-6.25 \mathrm{X} 6.25$ | ANALOG DEVICES, LTM4622EV\#PBF |

Additional Demo Board Circuit Components

| 2 | 1 | C2 | CAP, X5R, $10 \mu \mathrm{~F}, 25 \mathrm{~V}, 10 \%, 0805$ | TAIYO YUDEN, TMK212BBJ106KGHT |
| :---: | :--- | :--- | :--- | :--- |
| 4 | 3 | C4, C6, C18 | CAP, X5R, $1 \mu \mathrm{~F}, 10 \mathrm{~V}, 10 \%, 0603$ | MURATA, GRM188R61A105KA61D |
| 5 | 0 | C8, C15, C22, C28 | CAP, 0603 | OPTION |
| 6 | 1 | C10 | CAP, X5R, $22 \mu \mathrm{~F}, 25 \mathrm{~V}, 10 \%, 7343$ | SANYO, 25TQC22MV |
| 10 | 0 | C17, C25 | CAP, 7343 | OPTION |
| 18 | 1 | Q1 | XSTR, SUD50N04-8M8P-4GE3 MOSFET T0-252 | VISHAY, SUD50N04-8M8P-4GE3 |
| 19 | 1 | RS1 | RES, CHIP, $0.05 \Omega, 1 / 4 \mathrm{~W}, 1 \%, 1206$ | VISHAY, WSL1206R0500FEA |
| 20 | 0 | R2, R10, R12, R14, R16 T0 <br> R19, R21, R22, R23, R26 T0 <br> R29 | CAP, 0603 | OPTION |
| 21 | 1 | R3 | RES, CHIP, 10k, $1 / 16 \mathrm{~W}, 1 \%, 0603$ |  |
| 22 | 4 | R9, R15, R24, R25 | RES, CHIP, $100 \mathrm{k}, 1 / 16 \mathrm{~W}, 1 \%, 0603$ | VISHAY, CRCW060310K0FKEA |
| 24 | 1 | R13 | RES, CHIP, $0,1 / 16 \mathrm{~W}, 1 \%, 0603$ | VISHAY, CRCW0603100KFKEA |

Hardware: For Demo Board Only

| 13 | 14 | E1 T0 E14 | TESTPOINT, TURRET, 0.095" | MILL-MAX, 2501-2-00-80-00-00-07-0 |
| ---: | :---: | :--- | :--- | :--- |
| 14 | 2 | JP1, JP2 | HEADER, 1 X3 0.079 | SULLINS, NRPN031PAEN-RC |
| 15 | 1 | JP3 | HEADER, 2X3 0.079 | SULLINS, NRPN032PAEN-RC |
| 16 | 3 | XJP1, XJP2, XJP3 | SHUNT | SAMTEC 2SN-BK-G |
| 17 | 2 | J1, J2 | CONN, BNC, 5PINS | CONNEX, 112404 |
| 28 | 4 | STAND 0FF | STAND OFF, SNAP 0N, 0.375" TALL | KEYSTONE_8832 |

## SCHEMATIC DIAGRAM



## ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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