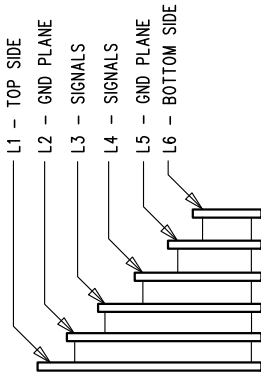


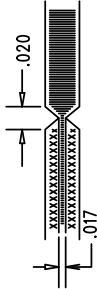
REVISION HISTORY			
ECO	REV	DESCRIPTION	APP. ENG.
-	3	PRODUCTION	YL
			09-16-16

## LAYER STRUCTURE



## NOTES: UNLESS OTHERWISE SPECIFIED

1. FAB PER IPC-A-600.
2. MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR-370HR OR EQUIVALENT.  
-FINISHED THICKNESS TO BE 0.062 +/- .005  
-TOTAL OF 6 LAYERS WITH 2 OZ. CU ON ALL LAYERS  
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
3. SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.  
0/0 ARE PRIMARY DATUMS.
4. DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001 THICK MIN.  
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.  
-HOLE LOCATION TOLERANCES ARE +/-0.003 IN RELATION TO CENTER
5. FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.  
-GOLD IMMERSION BOTH SIDES.  
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
6. DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.
7. DESIGN HAS SOLDER MASK DEFINED PADS ON U1.  
U1 SOLDER MASK SIZE IS 25 MIL AND PAD SIZE IS 29 MIL.  
DON'T CHANGE PAD SIZE OR SOLDER MASK SIZE.
8. PCBs ARE TO BE RoHS COMPLIANT.
9. SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):



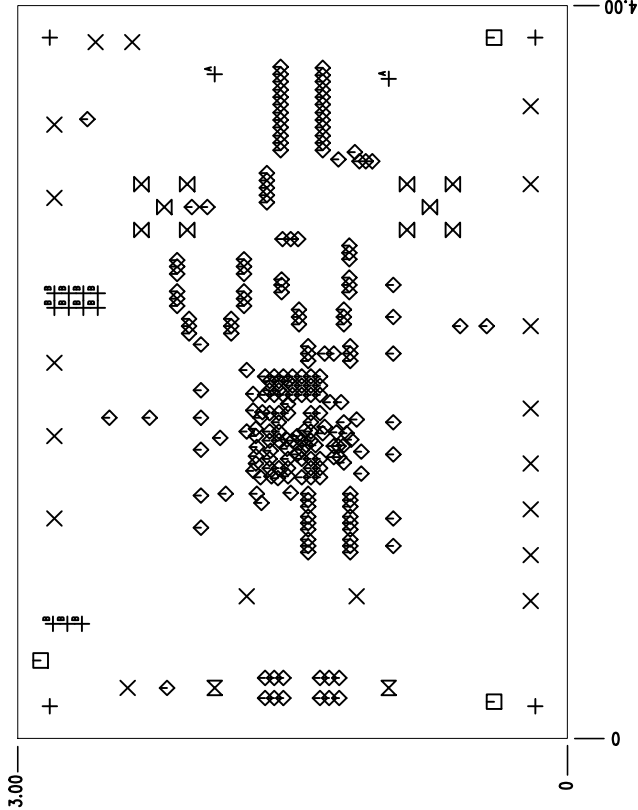
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		APPROVALS		LINEAR TECHNOLOGY				9510 MCCARTHY BLVD MILPITAS, CA 95035 PH: (408)432-9000 WWW.LINEARTECH.COM LTC CONFIDENTIAL - FOR CUSTOMER USE ONLY			
TOLERANCES:		PCB DES.		LT		TITLE: FABRICATION DRAWING  SINGLE-OUTPUT, HIGH EFFICIENCY STEP-DOWN µMODULE REGULATOR					
XX = ±0.01		APP ENG.		YL							
XXX = ±0.005											
INTERPRET DIM AND TOL PER ASME Y14.5M-1994						SIZE		IC NO.		REV	
THIRD ANGLE PROJECTION						N/A		LTM4647EY		3	
								DEMO CIRCUIT 2141A			
		SCALE = NONE						FILENAME:		DC2141A-3.PCB	
										SHT 1 OF 1	

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SIZE	QTY	SYM	PLATED	TOL
0.01	228	◇	YES	+/-0.003
0.035	11	⊥	YES	+/-0.003
0.055	10	⊗	YES	+/-0.003
0.064	18	⊗	YES	+/-0.003
0.07	3	□	NO	+/-0.003
0.187	4	+	NO	+/-0.005
0.189	2	⊥	YES	+/-0.005
0.205	2	⊗	YES	+/-0.005