LTP5900, LTP5901 and LTP5902 Highly Accelerated Life Test (HALT) Recommendations

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1 About This Document

This document summarizes the results of the Highly Accelerated Life Test (HALT) performed on the LTP5900, LTP5901 and LTP5902 modules ("Modules") between 2/04/2013 and 2/12/2013. Results of post-test evaluations and recommendations are also provided.

For details on the Modules, please refer to the respective product pages (references [1], [2] and [3].

The complete HALT report is provided in reference [6] (HALT Report). For other test reports, please refer to the appropriate documents provided in reference.

1.1 Audience

This document is intended for system developers and hardware designers.

1.2 Related Documents

The following related references are available:

[1] LTP5900 Product Page

[2] LTP5901 Product Page

[3] LTP5902 Product Page

[4] Humidity Test Report (internal document: 071-0015)

[5] Vibration Test Report (internal document: 071-0016)

[6] HALT Report (internal document: 071-0017)

1.3 Conventions and Terminology

This guide uses the following text conventions:

- `Computer type` indicates information that you enter, such as a URL.
- **Bold type** indicates buttons, fields, and menu commands.
- *Italic type* is used to introduce a new term.
- **Note:** Notes provide more detailed information about concepts.
- **Caution:** Cautions advise about actions that might result in loss of data.
- **Warning:** Warnings advise about actions that might cause physical harm to the hardware or your person.

1.4 Revision History

Document / Revision	Date	Description
071-00018 rev 1	11/14/2013	Initial release

Executive Summary

1.5 Introduction

The tested devices ("UUT") consist of the LTP5900, LTP5901 and LTP5902 products based on the LTC5800 mote-on-chip or manager-on-chip. The LTP5900 (ETERNA1) is a of a 22-pin through hole printed circuit board module and the LTP5901/2 (ETERNA2) are castellated surface mount modules.

It is important to note that HALT subjects the Modules to stresses that exceed product requirements and that **failures are expected**.

1.6 Overall Pass / Fail

All Tests Passed

1.7 Introduction

HALT was conducted on a statistically representative sample of each of the Modules (LTP5900, LTP5901 and LTP5902). A total of 36 Modules (12 of each type) were assembled or reflowed onto a test fixture in accordance with our customer usage guidelines. All tests were carried out concurrently on all the Modules.

The Modules were monitored as motes in a Smartmesh network. Two networks of 18 motes were established. A PC connected to the managers was used to assess the connectivity of all the Modules during testing. Regular logs with network statistics were recorded.

1.8 Failures/ Incompletes/ Concerns

No Failures of the LTP5900, LTP5901 or LTP5902 modules where noted within the specified operating conditions.

Failures where noted outside of operating conditions in Vibration Step Stress, Combined Environment (vibration and temperature). Soft failures occurred at cold in the Extended Temperature Test.

Those failures would need to be mitigated should the Modules be specified for extreme cold and extreme vibration environments.

A pre-test setup concern was addressed by adjusting the low voltage test parameter to compensate setup noise on the power supply rail.

1.9 Test Coverage

All HALT scheduled tests were performed. HALT includes: Cold Thermal Step Stress, Hot Thermal Step Stress, Voltage Margining Verification, Rapid Thermal Transitions, Vibration Step Stress, Combined Environment, and Extended Temperature Test.

The complete HALT report is available in reference [6]. Additional environmental and performance testing was carried out successfully in separate campaigns (see Related Documents [4] and [5].

2 Test Result Analysis

2.1 Pre-HALT Observations

2.1.1 Test Summary

The UUTs did not operate at low voltage 2.1vDC. The voltage was gradually increased and the UUTs remained operational at 2.2vDC.

2.1.2 Discussion

Prior to starting HALT, the ETERNA1 & ETERNA2 UUTs were successfully tested at the voltage specification of low 2.1vDC and 3.76vDC.

The text fixture supply rail was exhibiting cumulative noise from all the Modules preventing testing at the minimum spec voltage of 2.1V. The low voltage limit was then set at 2.2V for the remainder of the HALT campaign.

Note that the 2.1V supply voltage parameter has successfully applied in all DVT testing and in temperature on a statistically significant sample size across various build lots.

Modifying the minimum supply parameter (2.2V instead of 2.1V) for the purpose of HALT is not considered as a failure. All the tests were adequately carried out with the modified parameter, including voltage margining in temperature.

2.2 Cold Thermal Step Stress

All units successfully booted up and joined the network at 0°C, -20°C & -40°C.

2.3 Hot Thermal Step Stress

All units successfully booted up and joined the network at +45°C, +65°C & +85°C

2.4 Voltage Margining Verification

All units remained operational during the voltage margin test.

2.5 Rapid Thermal Transitions

All units remained operational throughout all 5 rapid temperature cycles.

2.6 Vibration Step Stress

2.6.1 Test Summary

The ETERNA1 & ETERNA2 UUTs were subjected to a vibration step stress to 30 Grms.

The UUTs remained operational to 20 Grms. At 25 Grms and higher vibration levels, most of the EMI shields on ETERNA1 Motes broke off the PCB and on ETERNA2 one shield broke. In addition, at 25 Grms and higher vibration levels, several UUTs became lost and disconnected from the network on both COM3 & COM7.

All the UUTs recovered at the end of the vibration test.

2.6.2 Discussion

At the 25 Grms setting, the accelerometers directly located on the Modules recorded significantly higher accelerations (Ch2=164.23 Grms and ch3=154.42 Grms). The fixture accelerometer also captured similar high acceleration readings (ch4 153.29 Grms). This is indicative of amplification created by fixture resonances, particularly visible on the vibration graphs in the 1kHz to 1.75 kHz range.

Taking into account the fixture effective transmissibility gain (resonance), the Modules were successfully subjected to accelerations actually greater than 100 Grms (109.86 ch4) while the vibration table setting was set to 20 Grms.

In conclusion, the shield damage observed during HALT is not considered failure since the Modules did not exhibit damages at accelerations levels (100 Grms) well in excess of the specification.

Should operation be required in extreme vibration environments, it is recommended that the shield design be modified accordingly; for example a different shield geometry, thickness or the addition of damping material under or around the shield could be explored.

Some Modules also disconnected from the mesh networks during Vibration Step Stress test. All recovered after the test. The intermittent failures could have been the result of loose shield material making random electrical contact on the test board.

2.7 Combined Environment

2.7.1 Test Summary

The ETERNA1 & ETERNA2 UUTs were exposed to 5 rapid temperature cycles from -40°C to +85°C combined with vibration ranging from 5 Grms to 25 Grms. The dwell time at each extreme was 15 minutes and the thermal transition rate was set to 30°C per minute.

All the UUTs intermittently failed and became disconnected throughout the combined environment. At the end of the combined environment, all the UUTs recovered except for Mote MAC_F7-77 which did not recover and was not displayed on the list of UUTs.

2.7.2 Discussion

Although all units intermittently failed and became disconnected throughout the Combined Environment test, it is not considered a failure for the same reasons as discussed in the Vibration Step Stress test: a 25 Grms setting actually exposes the units to accelerations in excess of 150 Grms.

A failure analysis was performed on Unit MAC_F7-77 which did not recover immediately after the test. The root cause was associated to the 32kHz crystal, found to be out of spec by 515ppm. However the crystal was later found to be back in compliance after being sent to the vendor for analysis. The crystal was then re-installed, and unit MAC_F7-77 was found to be operating.

2.8 Extended Temperature Test

2.8.1 Test Summary

ETERNA1 & ETERNA2 UUTs were subjected to extended cold and hot temperature step stress. The cold temperature began at -40°C and the hot temperature began at +85°C. The dwell time at each thermal step was 15 minutes. The results are as follows:

Extended Cold Temperature Test: The UUTs remained operational to -60°C. A power cycle test was performed at the end of -60°C and on COM3 15/18 motes were live and on COM7 16/19 were live. The UUTs were power cycled at +30°C and recovered.

Extended Hot Temperature test: The UUTs remained operational to +105°C. A power cycle test was performed at the end of the +105°C and all the UUTs passed.

2.8.2 Discussion

UUTs are not considered failing the Extended Temperature Test. The behavior described in the previous section may be explained by the crystal temperature characteristics: at extreme temperatures, crystals exhibit a relatively steep frequency curve resulting in wide part-to-part variation for a given temperature. As temperature drops, the crystal frequency error eventually exceeds the operating limits of the temperature compensation mechanism of the units.