REVISIONS				
ECO	REV	DESCRIPTION	DATE	APPROVED
1079	1	INITIAL RELEASE	5-16-12	
1152	2	CHANGED STUB LENGTH	8-6-12	
1208	3	SYNC'ED ALL REV'S	2-26-13	
1270	4	COVER WITH SOLDER MASK 9 GROUND VIA UNDER U1	07-17-13	
1369	5	TENTED BACK SIDE VIA'S	03-12-14	

23. MANUFACTURER TO ADD COUNTRY OF ORIGIN IN SILKSCREEN (FARSIDE).

22. INTERPRET DIMENSIONS PER ANSI-Y14.5.

21. CERTIFICATE OF COMPLIANCE TO BE PROVIDED ON ALL SHIPMENTS.

20. EACH LOT MUST INCLUDE ONE SOLDER SAMPLE AND ONE CORE SAMPLE.

19. TEAR DROPPING OF TRACE TO PAD JUNCTION ON ANY LAYER IS PERMITTED PROVIDING MINIMUM METAL-TO-METAL SPACING IS NOT COMPROMISED.

18. THIEVING NOT PERMITTED ON THIS DESIGN.

17. REMOVAL OF INNER SIGNAL LAYER NON-FUNCTIONAL PADS IS PERMITTED.

16. HOLE SIZE: HOLE SIZES GIVEN ARE "FINISHED" HOLE SIZE.

15. ELECTRICAL TEST: FINISHED PCB SHALL BE SUBJECT TO 100% CONTINUITY AND ELECTRICAL ISOLATION (SHORTS AND OPENS) TESTING. TEST FIXTURES TO BE GENERATED FROM PROVIDED IPC-D-356A FORMATTED NET LIST, CROSS-REFERENCED TO GERBER-EXTRACTED NET LIST DATA. THE BOARD MUST BE MARKED WITH A PERMANENT INK STAMP TO INDICATE PASSING THE ELECTRICAL TEST.

14. TRACE IMPEDANCE:
OUTER LAYERS: SINGLE ENDED: 0.020" TRACES TO BE 50 OHMS +/- 5 OHMS.

13. PCB STACKUP: PER DRAWING AND DIELECTRIC CONSTANT 4.5+/-0.15, FOR ALL THREE LAYERS.

12. PCB TRACES: NOMINAL CONDUCTOR WIDTHS ON FINISHED PCB TO BE WITHIN +/-15% OR 0.001 WHICHEVER IS LESS OF ARTWORK AS DEFINED ON GERBER DATA AND SUPPLIED APERTURE WIDTH.

11. SILKSCREEN: SILKSCREEN LEGEND OVER SOLDER MASK, BOTH SIDES. MATERIAL TO BE WHITE ELECTRICALLY NONCONDUCTIVE INK, NO INK TO APPEAR ON COMPONENT PADS, FIDUCIALS, ELECTRICALLY EXPOSED VIAS OR MOUNTING HOLES. MINIMUM TEXT HEIGHT TO BE 0.040 WITH 0.004 STROKE WIDTH. OVERLAP ONTO TENTED HOLES IS ALLOWED. USE ROHS-COMPLIANT MATERIAL.

10. MARKINGS: MARKING REQUIREMENTS ON SECONDARY SIDE OF PCB-SILKSCREEN DATE CODE AND UL RECOGNIZED VENDOR MARK. DATE CODE FORMAT- "DOM: WW-YY" (ACTUAL WEEK (WW) AND (YY) THAT THE FAB WAS MANUFACTURED). MARKING REQUIREMENTS ON TOPSIDE OF PCB- SILKSCREEN DATE CODE "DOM: WW-YY" (ACTUAL WEEK (WW) AND (YY) THAT THE FAB WAS MANUFACTURED). KEEP MARKINGS OUT OF HATCHED AREA SHOWN.

9. WARP AND TWIST: NOT TO EXCEED 0.010" / INCH.

8. TOLERANCES: ALL TOLERANCES ARE NONCUMULATIVE. HOLE TO EDGE TOLERANCE SHALL NOT VARY MORE THAN +/-0.010 INCHES. TRACE LINE WIDTH TO BE +/-0.001".

7. SOLDER MASK: ROHS COMPLIANT, LPI SOLDER MASK PER IPC-SM-840C, OVER BARE COPPER (SMOBC) BOTH SIDES. REGISTRATION TO BE WITHIN +/-0.002 OF THE ASSOCIATED CIRCUIT LAYER, WITH NO MASK APPEARING ON PADS. PRESENCE OF SOLDER MASK RESIDUE SCRATCHES, AND/OR CONTAMINATION WHICH IMPAIR CONTACT PERFORMANCE ARE CONSIDERED MAJOR DEFECTS, AND CAUSE FOR LOT REJECTION. COLOR: GREEN.

6. ANNULAR RING: 0.002 DIA MIN FOR EXTERNAL LAYERS, 0.001 DIA MIN FOR INTERNAL LAYERS.

5. FINISH: GOLD IMMERSION, 2-5 MICRO INCHES (ROHS COMPLIANT).

4. PLATING: 0.50 OZ COPPER ON 2 OUTER LAYERS, 0.50 OZ COPPER ON 2 INNER LAYERS. SEE STACKUP DRAWING.

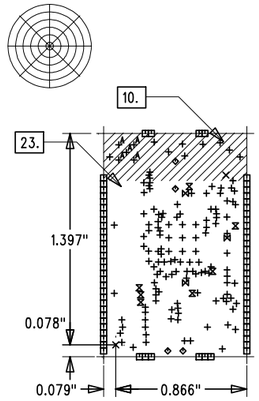
3. THICKNESS: 0.039 +/- .004 (FINISHED).

2. MATERIAL: FR-4 HYG 180 ROHS COMPLIANT MATERIAL. GLASS TRANSITION TEMPERATURE MUST MEET OR EXCEED THAT REQUIRED FOR LEAD-FREE PROCESSING. MATERIAL SHALL BE UL94V-D FLAMMABILITY RATED.

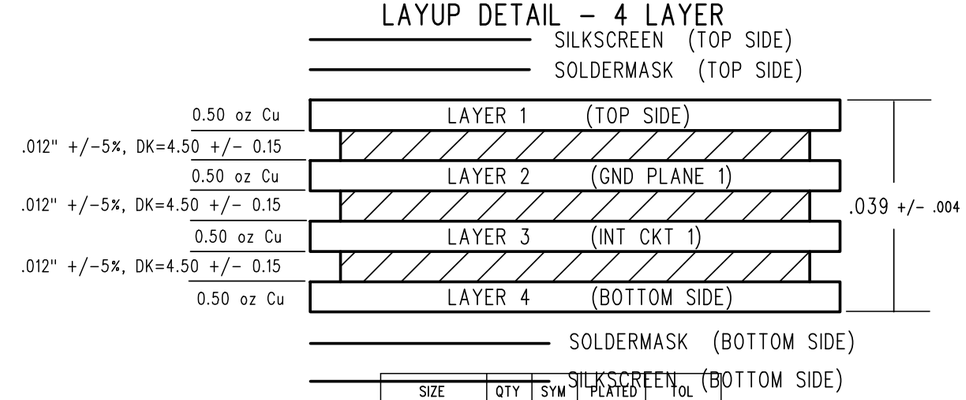
1. FABRICATION: FABRICATION AND ACCEPTANCE TO MEET THE REQUIREMENTS OF IPC-A-600 AND IPC/ANSI-MLL950-C CLASS 2, AOL .25 GENERAL INSPECTION LEVEL II. ACCEPTANCE STAMP NO LARGER THAN 0.25 INCH IS TO BE LOCATED ON THE SOLDER SIDE USING CONTRASTING (WHITE PREFERRED) NONCONDUCTIVE PERMANENT INK.

THE FAB SHALL BE ROHS-COMPLIANT.

NOTE: THE FAB SHALL BE BUILT TO THE SPECIFICATIONS LISTED HERE



LAYUP DETAIL - 4 LAYER



SIZE	QTY	SYM	PLATED	TOL
0.01	132	+	YES	+/-0.003
0.012	7	⧖	YES	+/-0.003
0.02	3	⋈	NO	+/-0.003
0.02	70	⊡	YES	+/-0.003
0.031	5	+A	YES	+/-0.003
0.035	4	◇	YES	+/-0.003
0.039	2	×	NO	+/-0.003

RPD ENGINEERING, GRASS VALLEY, CA 95945 530-271-0804
COMPANY: DUST NETWORKS DATE: 3/12/14 P/N: 600-0176
TITLE:CASTELLATED MOTE, CANADIAN REV:5
LAYER: A/W: 612-0176

SEE ARENA		UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES:	APPROVALS / DATE
NEXT ASSY	USED ON	TOLERANCES ARE: FRACTIONS: DECIMALS: .XX ± .01 ANGLES: 0° 30" .XXX ± .005	DRAWN BY: R.P.D. 9-16-10
APPLICATION		MATERIAL - SEE NOTES	CHECKED
		FINISH - SEE NOTES	ENGRG
		DO NOT SCALE DRAWING	ISSUED
			CONTRACT NO.

DUST NETWORKS

TITLE: PCB FAB, MODULE, CANADIAN

SIZE	FSCM NO.	DWG NO.	REV.
B		615-0176	5

SCALE: NONE SHEET 1 OF 1