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23. MANUFACTURER TO ADD COUNTRY OF ORIGIN IN SILKSCREEN (FAR SIDE).
22. INTERPRET DIMENSIONS PER ANSI-Y14.5.
21. CERTIFICATE OF COMPLIANCE TO BE PROVIDED ON ALL SHIPMENTS.
20. EACH LOT MUST INCLUDE ONE SOLDER SAMPLE AND ONE CORE SAMPLE.
19. TEAR DROPPING OF TRACE TO PAD JUNCTION ON ANY LAYER IS PERMITTED PROVIDING MINIMUM METAL-TO-METAL SPACING IS NOT COMPROMISED.
18. THIEVING NOT PERMITTED ON THIS DESIGN.
17. REMOVAL OF INNER SIGNAL LAYER NON-FUNCTIONAL PADS IS PERMITTED.
16. HOLE SIZE: HOLE SIZES GIVEN ARE "FINISHED" HOLE SIZE.
15. ELECTRICAL TEST: FINISHED PCB SHALL BE SUBJECT TO 100% CONTINUITY AND ELECTRICAL ISOLATION (SHORTS AND OPENS) TESTING. TEST FIXTURES TO BE GENERATED FROM PROVIDED IPC-D-356A FORMATTED NET LIST, CROSS-REFERENCED TO GERBER-EXTRACTED NET LIST DATA. THE BOARD MUST BE MARKED WITH A PERMANENT INK STAMP TO INDICATE PASSING THE ELECTRICAL TEST.
14. TRACE IMPEDANCE:
BOARD DOES NOT HAVE CONTROLLED IMPEDANCE TRACE
13. PCB STACKUP: PER DRAWING AND DIELECTRIC CONSTANT 4.3+/-0.15, FOR ALL THREE LAYERS.

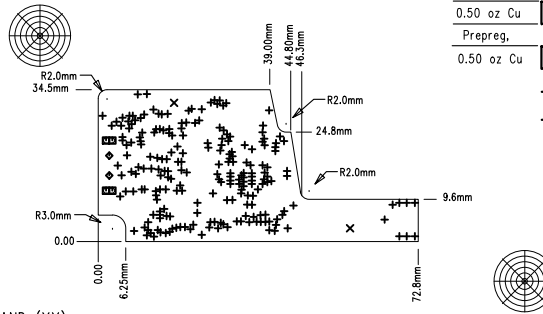
12. PCB TRACES: NOMINAL CONDUCTOR WIDTHS ON FINISHED PCB TO BE WITHIN +/-15% OR 0.001 WHICHEVER IS LESS OF ARTWORK AS DEFINED ON GERBER DATA AND SUPPLIED APERTURE WIDTH.
11. SILKSCREEN: SILKSCREEN LEGEND OVER SOLDER MASK, BOTH SIDES. MATERIAL TO BE WHITE ELECTRICALLY NONCONDUCTIVE INK, NO INK TO APPEAR ON COMPONENT PADS, FIDUCIALS, ELECTRICALLY EXPOSED VIAS OR MOUNTING HOLES. MINIMUM TEXT HEIGHT TO BE 0.040 WITH 0.004 STROKE WIDTH. OVERLAP ONTO TENTED HOLES IS ALLOWED. USE ROHS-COMPLIANT MATERIAL.
10. MARKINGS: MARKING REQUIREMENTS ON SECONDARY SIDE OF PCB-SILKSCREEN DATE CODE AND UL RECOGNIZED VENDOR MARK. DATE CODE FORMAT- "DOM: WW-YY" (ACTUAL WEEK (WW) AND (YY) THAT THE FAB WAS MANUFACTURED). MARKING REQUIREMENTS ON TOPSIDE OF PCB- SILKSCREEN DATE CODE "DOM: WW-YY" (ACTUAL WEEK (WW) AND (YY) THAT THE FAB WAS MANUFACTURED). KEEP MARKINGS OUT OF HATCHED AREA SHOWN.

9. WARP AND TWIST: NOT TO EXCEED 0.010" / INCH.
8. TOLERANCES: ALL TOLERANCES ARE NONCUMULATIVE. HOLE TO EDGE TOLERANCE SHALL NOT VARY MORE THAN +/-0.010 INCHES. TRACE LINE WIDTH TO BE +/-0.001".
7. SOLDER MASK: ROHS COMPLIANT, LPI SOLDER MASK PER IPC-SM-840C, OVER BARE COPPER (SMOBC) BOTH SIDES. REGISTRATION TO BE WITHIN +/-0.002 OF THE ASSOCIATED CIRCUIT LAYER, WITH NO MASK APPEARING ON PADS. PRESENCE OF SOLDER MASK RESIDUE SCRATCHES, AND/OR CONTAMINATION WHICH IMPAIR CONTACT PERFORMANCE ARE CONSIDERED MAJOR DEFECTS, AND CAUSE FOR LOT REJECTION. COLOR: GREEN.
6. ANNULAR RING: 0.002" DIA MIN FOR EXTERNAL LAYERS, 0.001" DIA MIN FOR INTERNAL LAYERS.
5. FINISH: GOLD IMMERSION, 2-5 MICRO INCHES (ROHS COMPLIANT).
4. PLATING: 0.5 OZ COPPER ON 2 OUTER LAYERS, 0.5 OZ COPPER ON 2 INNER LAYERS. SEE STACKUP DRAWING.
3. THICKNESS: 1.57mm +/- .005mm (FINISHED).
2. MATERIAL: FR-4 HYG 180 ROHS COMPLIANT MATERIAL. GLASS TRANSITION TEMPERATURE MUST MEET OR EXCEED THAT REQUIRED FOR LEAD-FREE PROCESSING. MATERIAL SHALL BE UL94V-D FLAMMABILITY RATED.

1. FABRICATION: FABRICATION AND ACCEPTANCE TO MEET THE REQUIREMENTS OF IPC-A-600 AND IPC/ANSI-MLL950-C CLASS 2, AOL .25 GENERAL INSPECTION LEVEL II. ACCEPTANCE STAMP NO LARGER THAN 0.25 INCH IS TO BE LOCATED ON THE SOLDER SIDE USING CONTRASTING (WHITE PREFERRED) NONCONDUCTIVE PERMANENT INK.

THE FAB SHALL BE ROHS-COMPLIANT.

NOTE: THE FAB SHALL BE BUILT TO THE SPECIFICATIONS LISTED HERE



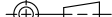

LINEAR TECHNOLOGY, MILPITAS CA 95035 408-432-1900			
COMPANY:	DUST NETWORKS	DATE: 11-05-14	P/N: 600-0235-0004
TITLE:	ETERNA USB MANAGER WITH CASTELLATED MODULE DRAGON		
LAYER:	FABRICATION DRAWING	A/W: 610-0235-0004	REV: 1

LAYUP DETAIL - 4 LAYER

	SILKSCREEN (TOP SIDE)	
	SOLDERMASK (TOP SIDE)	
0.50 oz Cu	LAYER 1 (TOP SIDE)	
Prepreg,		
0.50 oz Cu	LAYER 2 (GND PLANE 1)	
Prepreg,		
0.50 oz Cu	LAYER 3 (GND PLANE 2)	
Prepreg,		
0.50 oz Cu	LAYER 4 (BOTTOM SIDE)	
	SOLDERMASK (BOTTOM SIDE)	
	SILKSCREEN (BOTTOM SIDE)	

1.57mm
4 LAYERS

SIZE	QTY	SYM	PLATED	TOL
0.2	218	+	YES	+/-0.008
2.5	2	X	YES	+/-0.008
1.1 x 2.5	2	□	YES	+/-0.008
1.4	2	◇	YES	+/-0.008

<div>UNLESS OTHERWISE SPECIFIED</div> <div>DIMENSIONS ARE IN INCHES</div> <div>TOLERANCES:</div> <div>0.1XX" = ±0.01"</div> <div>0.0XX" = ±0.005"</div> <div>INTERPRET DIM AND TOL</div> <div>PER ASME Y14.5M-1994</div> <div>THIRD ANGLE PROJECTION</div> <div></div>	APPROVALS		<div>LINEAR TECHNOLOGY</div> <div>1630 MCCARTHY BLVD MILPITAS, CA 95035 PH: (408) 432-1900 WWW.LINEAR.COM ETC CONFIDENTIAL FOR CUSTOMER USE ONLY</div>
	PCB DES.	AK	
	APP ENG.	JON M.	
	TITLE: FABRICATION DRAWING		
	ETERNA USB MANAGER		
WITH CASTELLATED MODULE DRAGON			SIZE IC NO. REV 1 N/A 615-0235-0004 1
SCALE = NONE			
FILENAME: SHIT 1 OF 1			