

PCA SCH, MOTHERBOARD, CAMANCHE, MOTE VERSION

Content:

- 1. Title Page
- 2. Eterna
- 3. Memory
- 4. Connectors, LED & Power

Notes:

1. Associated Documents



BOM
700-0216-0401 REV2



ASY DWG
705-0216-0001 REV1



PCB FAB
600-0216-0001 REV1

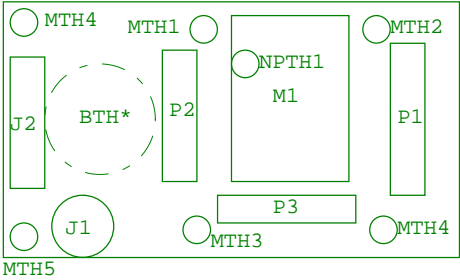
2. Assembly Options

- 1. External Memory or not
- 2. Russian or Canadian or uModule Oski based
- 3. PA_EXT_SET R value

Revision History:

Rev	Description	ECO	Author
01	Initial release, from 700-0216-0101 Rev 2	1263	Ric Peregrino
02	Load RADIO_INHIBIT and SLEEPn pulls	1365	Christophe Niglio

Parts placement, not to scale




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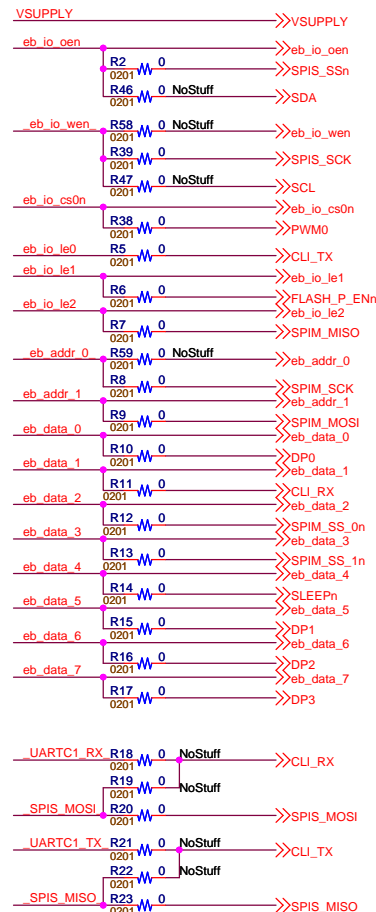
CUSTOMER NOTICE

LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.

THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND IS SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.

CONTRACT NO.	 A Linear Technology Company 1630 McCarthy Blvd. Phone: (408)432-1900 Milpitas, CA 95035 Fax: (408)434-0507			
APPROVALS				
DRAWN:				
CHECKED:				
APPROVED:				
ENGINEER:	TITLE: DC9018B-B			
DESIGNER:	PCA SCH, MOTHERBOARD, CAMANCHE			
	SIZE B	DWG NO. 710-0216-0401		REV 02
	DATE: Tuesday, February 25, 2014		SHEET 1 OF 4	

Place all R's on this page
as close as possible to M1



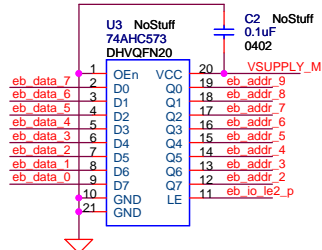
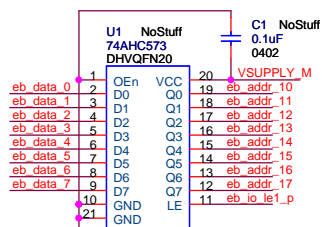
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SHEET 2 OF 4

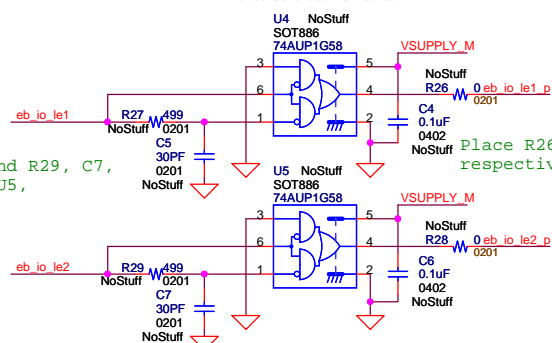
25 mil traces for VSUPPLY_M

VSUPPLY_M << VSUPPLY_M

eb_io_cs0n << eb_io_cs0n
 eb_io_le1 << eb_io_le1
 eb_io_le2 << eb_io_le2
 eb_addr_0 << eb_addr_0
 eb_addr_1 << eb_addr_1
 eb_data_0 << eb_data_0
 eb_data_1 << eb_data_1
 eb_data_2 << eb_data_2
 eb_data_3 << eb_data_3
 eb_data_4 << eb_data_4
 eb_data_5 << eb_data_5
 eb_data_6 << eb_data_6
 eb_data_7 << eb_data_7
 eb_io_oe1 << eb_io_oe1
 eb_io_oe2 << eb_io_oe2
 eb_io_wen << eb_io_wen



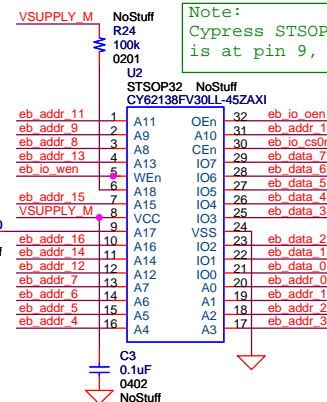
Pulse Generator Circuits



Place R27, C5, and R29, C7, close to U4 and U5, respectively

Place R26 and R28 close to U4 and U5, respectively

Stuff R25 for 256Kx8
 eb_addr_17 R25 0



Note:
 Cypress STSOP-32 pin 1
 is at pin 9, or A17



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CONTRACT NO.

APPROVALS

DRAWN:

CHECKED:

APPROVED:

ENGINEER:

DESIGNER:



A Linear Technology Company

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TITLE: **DC9018B-B**
 PCA SCH, MOTHERBOARD, CAMANCHE

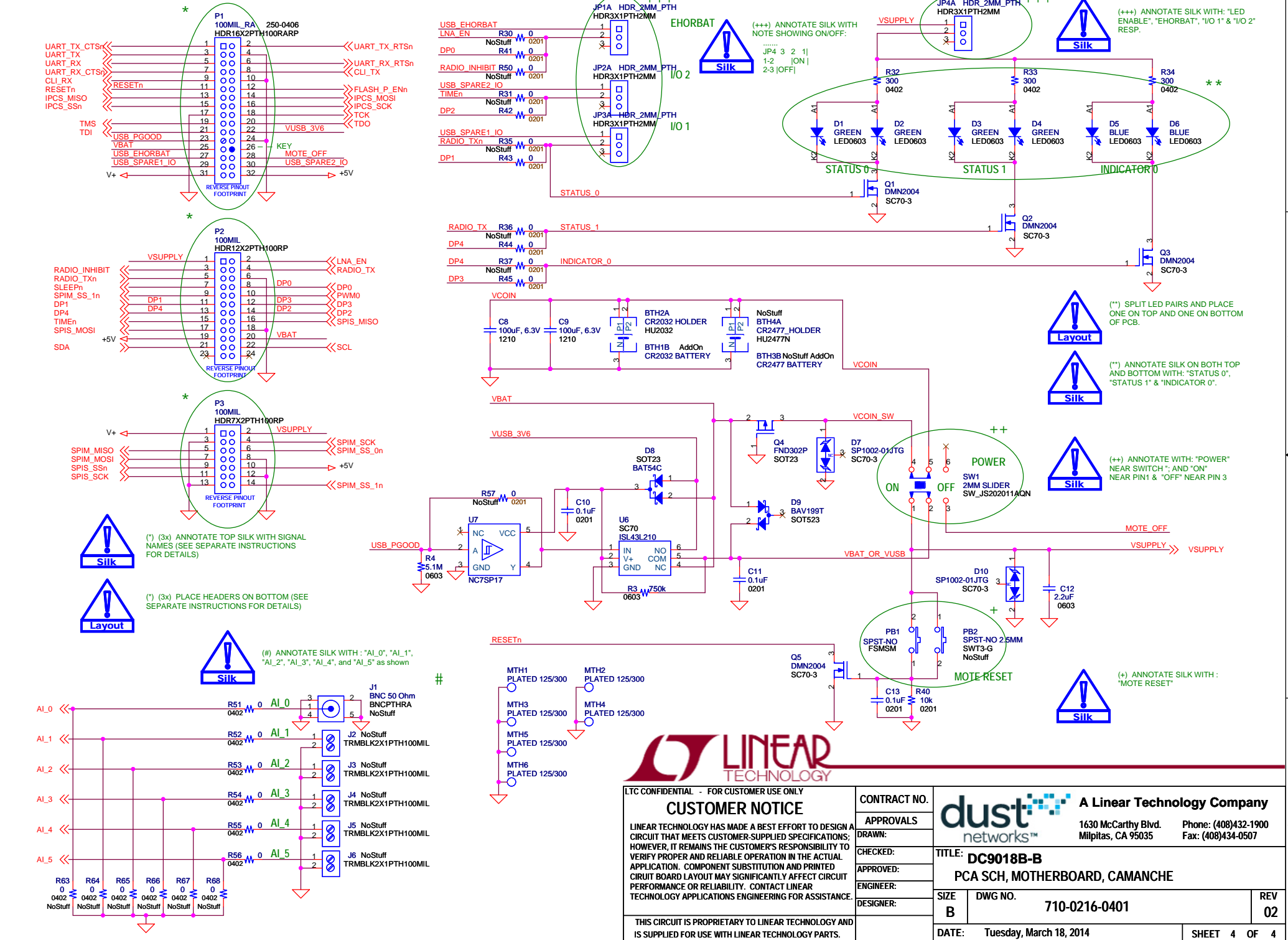
SIZE B DWG NO. 710-0216-0401


REV 02

DATE: Tuesday, March 18, 2014

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CONNECTORS, VISUAL INDICATORS, POWER



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		DATE: Tuesday, March 18, 2014			SHEET 4 OF 4