

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. <http://www.analog.com/aerospace>

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/MAT03

2.0 Part Number. The complete part number(s) of this specification follow:

<u>Part Number</u>	<u>Description</u>
MAT03-903L	Low noise, matched, dual PNP transistor

2.1 Case Outline.

<u>Letter</u>	<u>Descriptive designator</u>	<u>Case Outline (Lead Finish per MIL-PRF-38535)</u>
L	GDFP1-F10	10-Lead ceramic flatpack (cerpak)

<u>Terminal Connections ^{1/}</u>	
<u>Terminal</u>	<u>10 lead flatpack</u>
1	C1
2	nc
3	B1
4	nc
5	E1
6	E2
7	nc
8	B2
9	nc
10	C2

Figure 1 - Terminal connections.

^{1/} Substrate is normally connected to the most negative circuit potential, but can be floated.

3.0 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Collector to base voltage (BV_{CBO})	36V
Collector to emitter voltage (BV_{CEO})	36V
Collector to collector voltage (BV_{CC})	36V
Emitter to emitter voltage (BV_{EE})	36V
Collector current (I_C)	20mA
Emitter current (I_E)	20mA
Total power dissipation ^{1/}	500mW
Operating ambient temperature range	-55 to +125°C
Operating junction temperature range	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 60 sec)	+300°C
Dice junction temperature	+150°C

^{1/} Rating applies to applications not using heat sinking, device is free air only.

3.1 Thermal Characteristics:

Thermal Resistance, cerpac (L) Package
 Junction-to-Case (Θ_{JC}) = 80°C/W Max
 Junction-to-Ambient (Θ_{JA}) = 180°C/W Max
 Derate linearly at 5.56 mW/°C for ambient temperatures above 70°C.

4.0 Electrical Table:

Table I							
Parameter See notes at end of table	Symbol	Conditions ^{1/}	Sub-group	Limit Min	Limit Max	Units	
Current gain	h_{FE}	$I_C = 1\text{mA}, V_{CB} = 0\text{V}, -36\text{V}$	1	100			
			2, 3	70			
		$I_C = 100\text{A}, V_{CB} = 0\text{V}, -36\text{V}$	1	90			
		$I_C = 100\text{A}, V_{CB} = -36\text{V}$	2, 3	60			
		$I_C = 10\text{A}, V_{CB} = 0\text{V}, -36\text{V}$	1	80			
		$I_C = 10\text{A}, V_{CB} = -36\text{V}$	2, 3	50			
Current gain match ^{2/}	Δh_{FE}	$I_C = 100\text{A}, V_{CB} = 0\text{V}$	1		3	%	
Offset voltage	V_{OS}	$V_{CB} = 0\text{V}$	1		100	μV	
			2,3		150		
Change in offset voltage vs temperature ^{3/}	TCV_{OS}	$V_{CB} = 0\text{V}$			0.5	$\mu\text{V}/^\circ\text{C}$	
Offset voltage change vs V_{CB}	$\Delta V_{OS} / \Delta V_{CB}$	$V_{CB} = 0\text{V}, -36\text{V}$	1		150	μV	
Offset voltage change vs collector current	$\Delta V_{OS} / \Delta I_C$	$I_{C1} = 10\text{A}, I_{C2} = 1\text{mA}, V_{CB} = 0\text{V}$	1		50		
Input offset current	I_{OS}	$V_{CB} = 0\text{V}, I_C = 100\mu\text{A}$	1		35	nA	
Bulk emitter resistance	r_{BE}		1		0.75	Ω	
Collector base leakage current	I_{CBO}	$V_{CB} = -36\text{V}$	1		200	pA	
Collector saturation voltage	$V_{CE\text{SAT}}$	$I_C = 1\text{mA}, I_B = 100\mu\text{A}$	1		0.1	V	
Breakdown voltage	BV_{CEO}		1	36		V	
Noise voltage density	e_n	$I_C = 1\text{mA}$ $V_{CB} = 0\text{V}$	$f_0 = 10\text{Hz}$	7		2	$\text{nV}/\sqrt{\text{Hz}}$
			$f_0 = 100\text{Hz}$			1	
			$f_0 = 1000\text{Hz}$			1	
			$f_0 = 10000\text{Hz}$			1	

Table I Notes:

^{1/} $V_{CB} = -15\text{V}, I_C = 10\mu\text{A}$, unless otherwise specified.

^{2/} Current gain match (Δh_{FE}) is defined as: $\Delta h_{FE} = \frac{100 (\Delta I_C) h_{FE\text{ min}}}{I_C}$

^{3/} Guaranteed by VOS test ($TCV_{OS} = V_{OS}/T$ for $V_{OS} \ll V_{BE}$) ($T = 298^\circ\text{K}$ for $T_A = +25^\circ\text{C}$).

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, <u>1/</u> <u>2/</u>
Group A Test Requirements	1, 2, 3, 7
Group C end-point electrical parameters	1 <u>2/</u>
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1. Delta's excluded from PDA.
2/ See Table III for delta parameters. See table I for conditions.

4.2 Table III. Burn-in test delta limits.

Table III				
TEST TITLE	BURN-IN ENDPOINT	LIFETEST ENDPOINT	DELTA LIMIT	UNITS
h_{FE} @ 1mA	100 min	60 min	±40	
h_{FE} @ 100µA	90 min	54 min	±36	
h_{FE} @ 10µA	80 min	48 min	±32	
IOS	35	55	±20	nA

5.0 Life Test/Burn-In Circuit:

- 5.1 HTRB is not applicable for this drawing.
- 5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
- 5.3 Steady state life test is per MIL-STD-883 Method 1005.

MAT03

Rev	Description of Change	Date
A	Initiate	7/24/2000
B	Page 1: Update web address; correct typo for dice junction temperature. Page 2: change RC package theta JC from 18 to 35 °C Page 3: delete text "note 1" under table I conditions; change delta hFE condition from mA to •A; delete subgroups for TC _{VOS} ; format note numbers for table I; change note 3 from " This is the maximum change in V _{OS} measured at I _C = 10mA with V _{CB} = 0V" TO "Guaranteed by VOS test (TC _{VOS} = V _{OS} /T for V _{OS} << V _{BE}) (T = 298°K for T _A = +25°C)" Page 4, Table II: delete subgroup 7 from final electricals Page 5: add resistor values to burn-in figure.	1/22/2002
C	Change R3 of BI circuit from 2.5K to 10K ohm.	4/17/2002
D	Update web address. Delete burn-in circuit.	6/20/2003
E	Update package offering	10/10/2007
F	Update header/footer & add to 1.0 scope description	2/25/2008
G	Remove min. range in Dice Junction Temp	3/28/2008
H	Remove obsolete part number and update ASD to ADI standard	11/10/11