Heavy-Ion Test Results of the Voltage Comparator RH1011M

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Executive Summary

This report details the heavy-ion test experiments performed on the RH1011M at the Lawrence Berkeley National Labs (LBNL). The RH1011M [1] is a general purpose comparator with significantly better input characteristics than the LM111. Heavy-ions induced SEE (Single Event Effect) experiments included Single Event Transient (SET), Single Event Upset (SEU) and Single Event Latchup (SEL) tests up to an LET of 114 MeV.cm^2/mg at elevated temperatures (to case temperatures of 100°C). Under heavy-ion irradiations, with various inverting input bias conditions (proportional to differential input voltage as the non-inverting input voltage is fixed), the RH1011M showed sensitivities only to SETs. Beam tests confirmed the SEL and SEU immunity of this part in all test conditions. With the appropriate filtering capacitance at the output, the RH1011M was fully-mitigated to SET. The measured SET sensitive cross-section is about 1.6% of the total die's area. Because of the small difference in the offset voltage (VOS) with temperature (2mV at room and 4mV at 125°C), the SEE test results were not dependent on the temperature. However, when the comparator differential input voltage was very close to the offset voltage (VOS) or the inverting input voltage to the hysteresis boundary voltages, the SET pulse-width (PW) was the widest, and the measured SET cross-sections were the highest. At higher LET near the limiting cross-section, the dependence on differential input bias becomes less significant, as most SETs become wide.

The SET cross-sections dependence on these biases could be simply due to the peripheral capacitances charge/discharge times, so what might seem as bias dependence is truly related to parasitic time constants. We believe that the initial SET-PW will depend on the circuit response and the flux but its propagation on its parasitic and the ion's diffusion [4]. Careful selection of the circuit parasitic is crucial when operating the circuit in radiation beams, as they can change the time constants for signal propagation and widen the radiation-induced transients. This circuit can be used as is, as the widest measured SET-PW is about the comparator's response time. However, for accurate selection of the SET filter or for the circuit peripheral parasitic, we would recommend that the designer simulates his design by injecting SETs at the circuit inputs/outputs, as wide as the DUT maximum response time, as well as varying the bias during these injections. This could be accomplished by the LTSpice tool offered by Linear Technology, as most of the Linear LT parts spice models are offered [5]. That should provide guidance to the designer but the result should be correlated with laser and beam tests as most of the RH and LT parts differ in their process and sometimes in their design as well. The wrong selection of these parasitic can make things worse and widen the SET from nanoseconds to microseconds, making it harder on the following circuit to not propagate them.

1. Overview

This report details the heavy-ion test experiments performed on the RH1011M at the Lawrence Berkeley National Labs (LBNL). The RH1011M is a general purpose comparator with significantly better input characteristics than the LM111. It offers four times lower bias current, six times lower offset voltage and five times higher voltage gain. The RH1011M retains all the versatile features of the LT1011, including single 3V to ±18V supply operation, and a floating transistor output with 50mA source/sink capability. It can drive loads referenced to ground, negative supply or positive supply, and is specified up to 36V between V– and the collector output. A differential input voltage up to the full supply voltage is allowed, even with ±18V supplies, enabling the inputs to be clamped to the supplies with simple diode clamps. The RH1011M voltage offset (VOS) does not exceed ±4mV across the full range of the spec'd die junction temperature (-55°C to 125°C).

The wafer lots are processed to Linear Technology's in house Class S flow to yield circuits usable in stringent military applications. The device is qualified and available in three different hermetically sealed packages (8-Lead CERDIP (J8), 10-Lead flatpack (W10) and 8-Lead TO-5 Metal Can (H8)). More details are given about this voltage comparator in [1, 2 and 6]. This is a 7um technology using exclusively bipolar transistors. The part's block diagram is shown in Fig. 1. The H and W package designations are given in Figs. 2 and 3.

Absolute Maximum Ratings

Supply Voltage	36V
Output to Negative Supply	35V
Ground to Negative Supply	30V
Differential Input Voltage	35V
Voltage at STROBE Pin	5V
Input Voltage	Equal to Supplies
Output Short-Circuit Duration	10 sec
Operating Temperature Range	-55ºC
Storage Temperature Range	-65ºC
Lead Temperature (Soldering, 10 sec)	300ºC

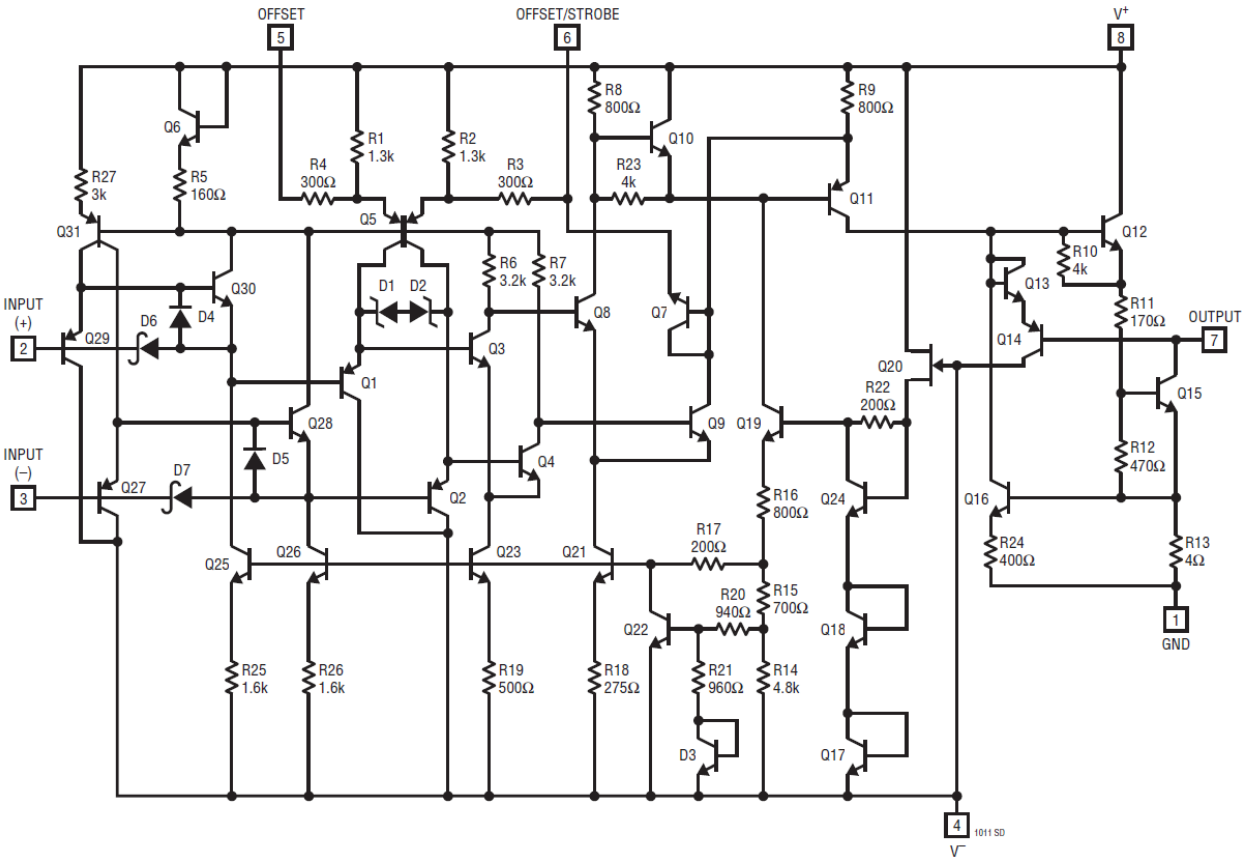

Fig. 1: Block Diagram of the RH1011M DIE

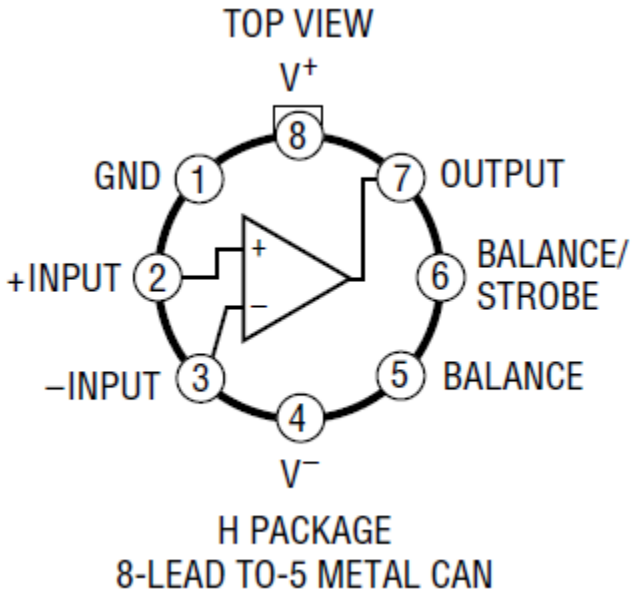

Fig. 2: RH1011M in H Package

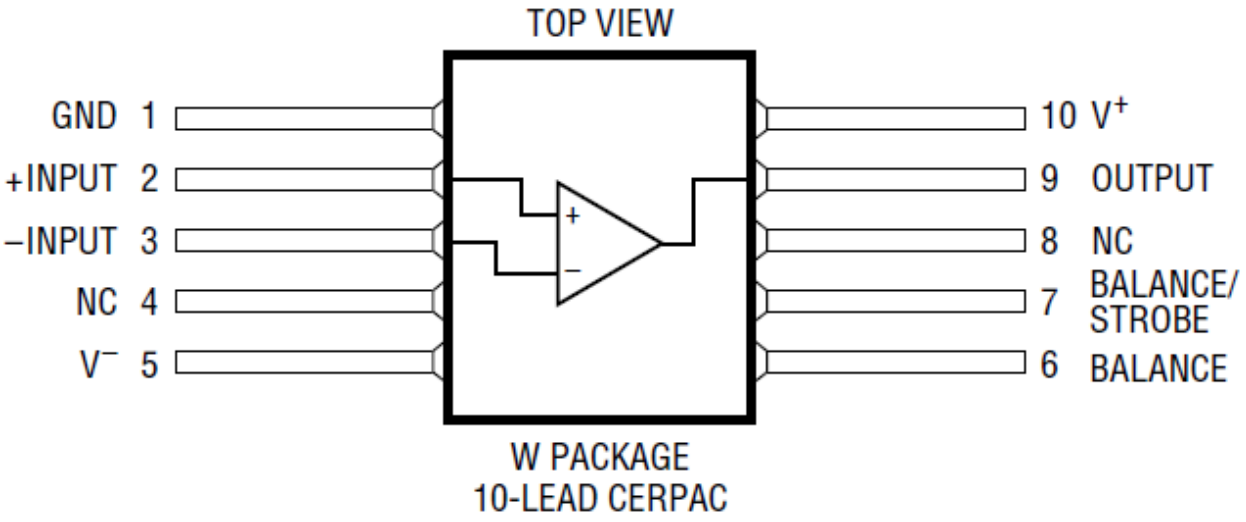

Fig. 3: RH1011M in W Package

Table 1 summarizes the parts' features and the electrical test equipment.

Table 1: Test and Part's Information

Generic Part Number	RH1011M
Package Marking	RH1011 Date Code
Manufacturer	Linear Technology
Fabrication Lot/Lot Date Code (LDC)	570900.1/1013A, 140392.2/9721B
Quantity tested	4
Dice Dimension	2.032 X 1.219 $mm^2 \approx 2.477\ mm^2 \approx 1/40\ cm^2$
Part Function	Voltage Comparator
Part Technology	BIPS700
Package Style	Hermetically sealed flat-10, Metal can-8
Test Equipment	Power supply, digital oscilloscope, multimeter, and computer
Temperature and Tests	SET, SEU and SEL @ Room Temp. and 100°C

2. Test Setup

Custom SEE boards were built for heavy-ion tests by the Linear Technology team, based on provided schematics from The Aerospace Corporation, Northrop Grumman and Ball Aerospace engineers. The RH1011MW and RH1011MH parts were tested at LBNL on Sept. 2012 at two different temperatures (at room temperature as well as at 100°C). During the beam runs, we were monitoring the temperature of the adjacent sense transistor (2N3904) to the DUT but not the die temperature (junction temperature). Hence the test engineer needs to account for additional temperature difference between the dice and the sense transistor, which was not measured in vacuum. In-air, both of the case and the sense transistor temperatures were measured to be the same. The temperature difference between the junction of the die and the case is a function of the DUT power dissipation multiplied by the thermal resistance $R_{theta\text{-}JC}(\Theta_{JC})$. With no heating, the temperature of the adjacent temperature sense transistor (2N3904) to the DUT (or the DUT case) was measured on average at about 35°C. The junction temperature was not measured in vacuum; its calculation is provided in Eq.1. This value was correlated in-air with a thermocouple.

$$T_J = T_C + P_D * \Theta_{JC} \qquad (1)$$

Where: T_J is the junction temperature, T_C the case temperature, P_D the power dissipated in the die and Θ_{JC} the thermal resistance between the die and the case. Note: A relatively small amount of power is dissipated in other components on the board. The sense transistor temperature (very similar to the case one) during each run is shown in Tables 2 and 3. That is not considered in this calculation.

The calculation of the dissipated power in the die is provided in Eq. 2:

$$P_D = Pin - Pout = |V_+ * I_+| + |V_- * I_-| - Pout \qquad (2)$$

Where:
1. V+ is the positive voltage supply
2. V- is the negative voltage supply
3. I+ is the positive current supply
4. I- is the negative current supply
5. Pin: Input Power Dissipation
6. Pout: Output Power Dissipation

Assuming that Pout =0 and in the case where:

$$T_c = 30°C;\ V_+ = 12V;\ V- = -12V;\ I_+ = 2.5mA;\ I_- = 5.2mA;\ \text{and}\ \Theta_{JC} = 40°C/W\ [6],$$

$$\underline{P_D = 92.4mW \text{ and } T_J \approx 34°C}$$

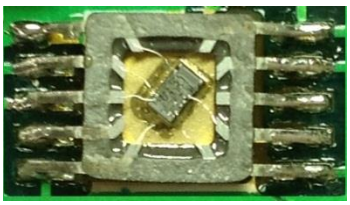

Fig. 4: Photography of the Decaped RH1011MW Dice

Two SEE test boards have been manufactured; the first one is called the hysteresis board and the second one VOS board. The naming of each board is a reflection of the part's most sensitive area in the beam, where SETs are the widest and their respective SET cross-sections are the highest. In the case of the hysteresis board, it is between 554 and 610mV, while for the VOS board at maximum junction temperature, it is between -4 and 4mV. For instance, the hysteresis board contains:

- The DUT with open-top (as shown in Fig. 4)
- The filtering caps for the voltage supplies (V- (-12V), V+ (+12V), VRef (+5V), VD (+5V))
- A filtering capacitance for the output (0.1uF used only for the filtering case)
- The hysteresis circuit (R1, R7 and R8 resistors)
- The 2N3904 bipolar transistor to sense the board temperature

For the Hysteresis board, the beam tests were run with and without the capacitance C6. This capacitance was added by the NGC engineers mainly for the mitigation of SETs that might occur on the 5VREF signal, originating from a peripheral circuit other than the RH1011M. It is not required for the RH1011M circuit and the data provided in the remaining of this report will demonstrate its non-impact on the obtained SET data. Figs. 5 and 6 show the SEE test board schematics. The pictures of these boards are given in Figs. 7 and 8.

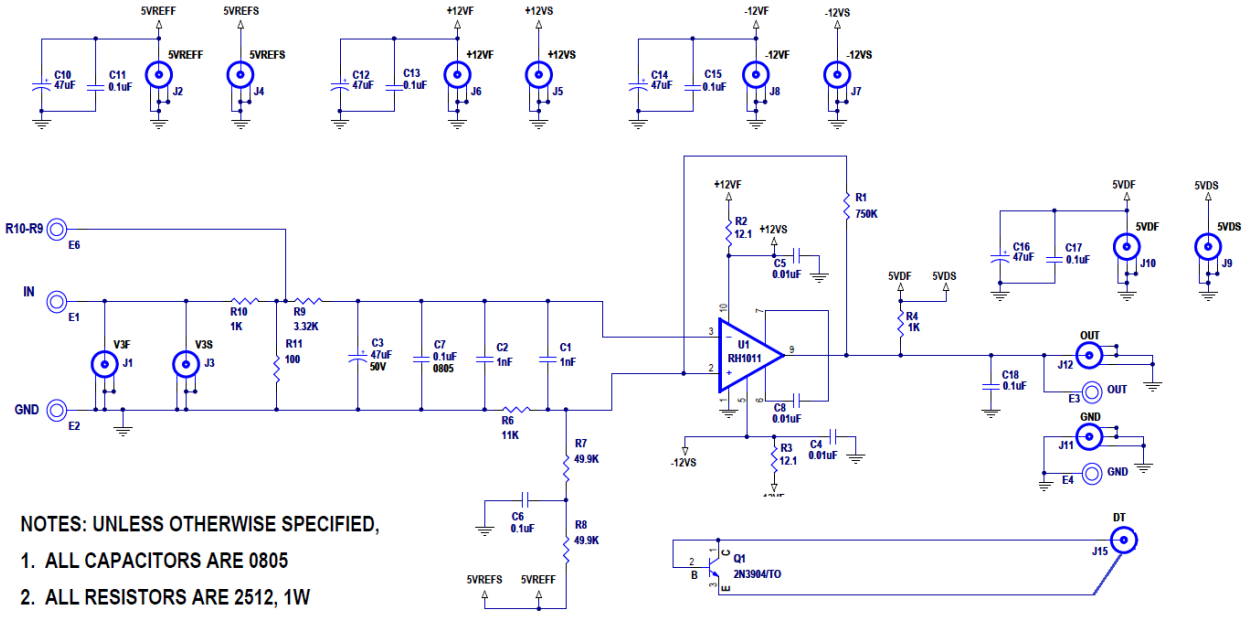

Fig. 5: Block Diagram of the RH1011MW SEE Hysteresis Board

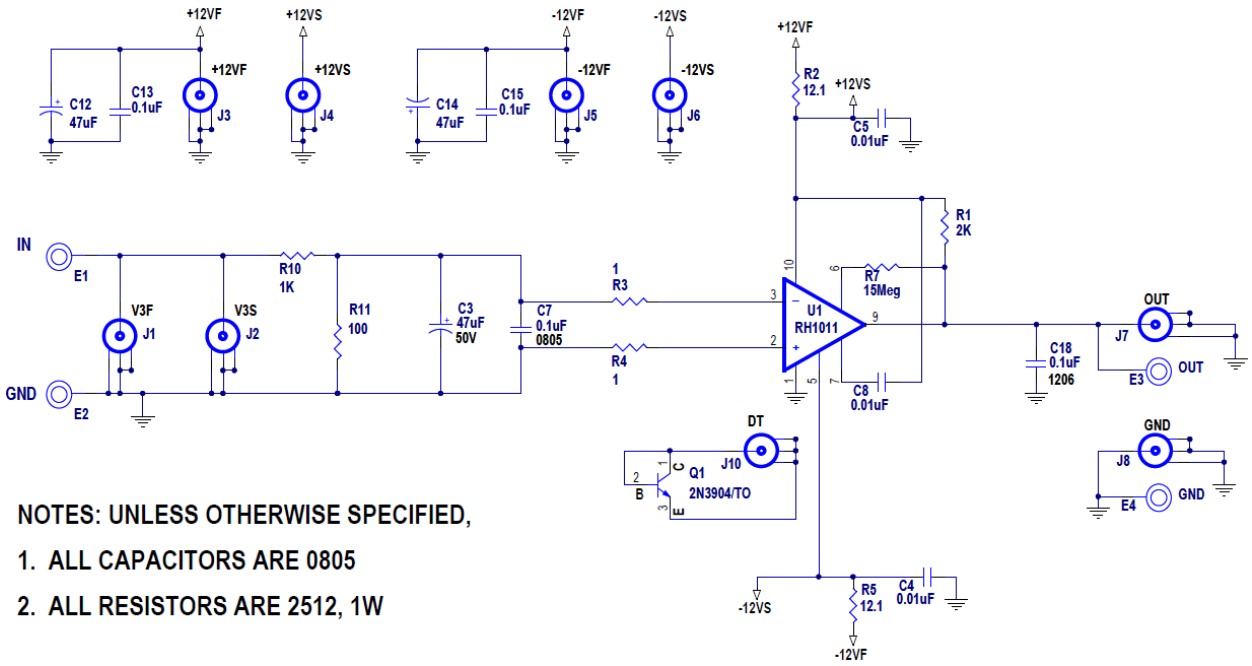

Fig. 6: Block Diagram of the RH1011MW SEE VOS Board

To minimize the distortion of the measured SET-PW, the test setup was placed as close as possible to the vacuum chamber. It is connected with two 3 ft long BNC cables to two Agilent Power Supplies (PS) (N6705B) and to a Tektronix oscilloscope (TDS6604B 1GHz, 2GS/s) to view the output signal (Vout). The first PS supplies the input voltages to the SEE test board and allows the automated logging and storage every 0.5 ms of the current input supplies (Iin), as well as the automation of power-cycles after the detection of a current spike on the input current that exceeds the current limit set by the user. The second PS is used for sensing the voltages of the input power supplies. This was done to avoid any interference from the power supplies that might cause widening of the transients upon the occurrence of an SET. The output pin (Vout) was also connected through two 3 ft BNC cables (vacuum chamber feed-through) to the scope. For better accuracy, the equivalent capacitive load of these cables should be calculated and accounted for, as it might affect the SET pulse width and shape. In this case, the cables capacitive load was about 250 pF. Note that during the laser tests, these BNC cables were replaced with a scope probe with an equivalent capacitive load about 10pF to minimize the distortion of the SET pulse. As the beam test results did not vary with the package (H and W), except for the SEU data, all SET data is extracted from the heavy-ions tests on the W packaged DUTs.

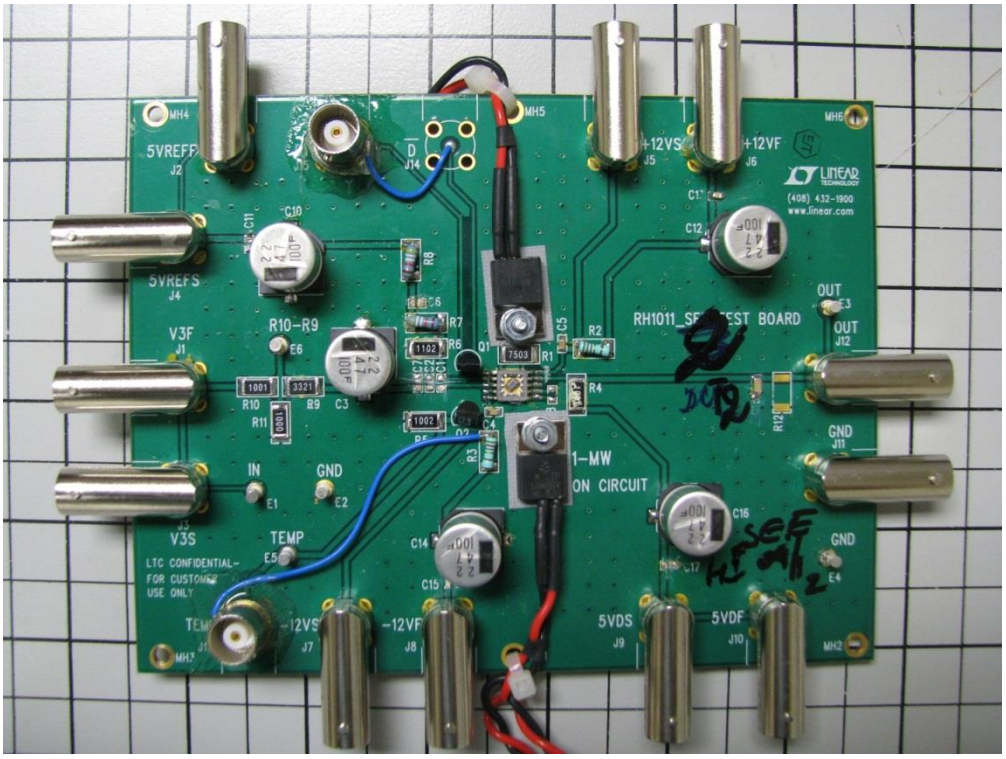

Fig. 6: Photograph of the first SEE Test Board (Hysteresis Board)

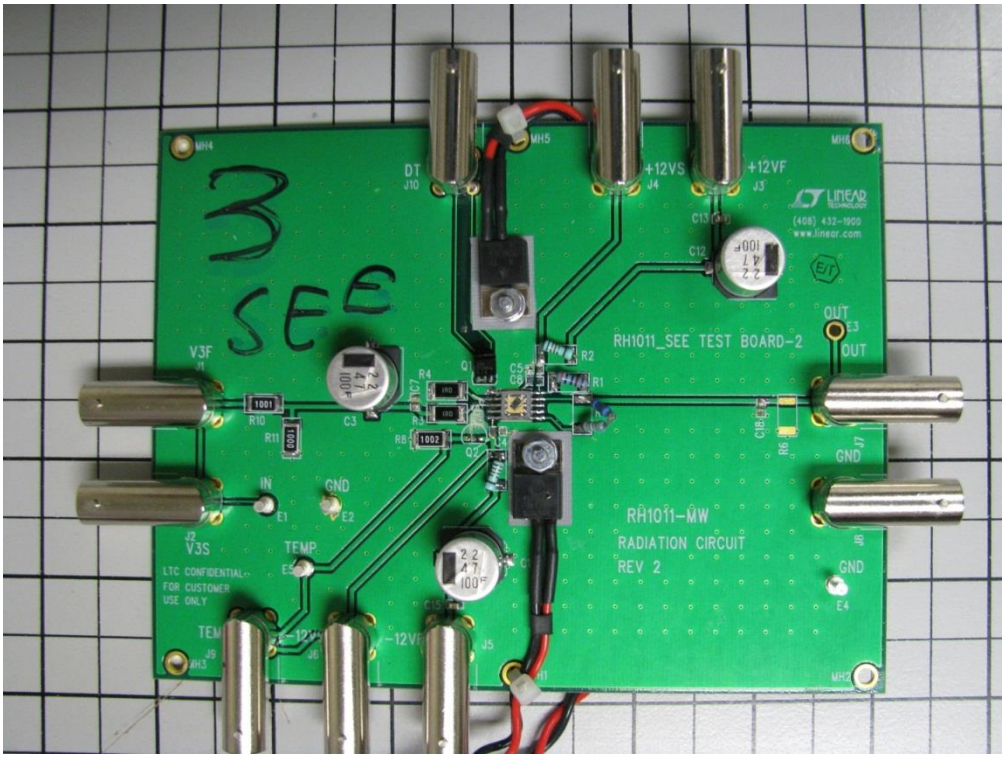

Fig. 7: Photograph of the Second SEE Test Board (VOS Board)

3. Heavy-Ion Beam Test Conditions

The RH1011M part was tested under various input bias conditions ranging from 50 to 1000mV in the case of the hysteresis board and from -200 to 200mV in the case of the VOS board. The selected beam energy is 10MeV/nucleon, which correlates with beam ions delivered at a rate of 7.7 MHz (eq. to a period of 130 ns). During these 130 ns, the ions are generated only within very short pulses that last for 10 ns, as shown in Fig. 8. At every pulse of 10 ns, N number of particles per square centimeter, depending on the flux, will be irradiating the DUT. The calculation of N is provided in Eq. 3:

$$N = \text{Flux} * 130\text{ns} \qquad (3)$$

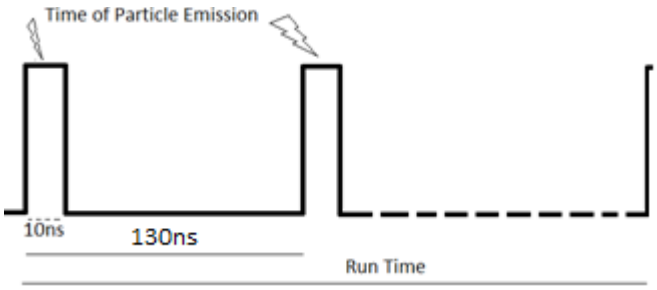

Fig. 8: Particle Emission during a Beam Run at Beam Energy of 10 MeV/nucleon; Emission Frequency = 7.7MHz

For instance if the flux equals 10^4 particles/cm^2/second, the probability (N) of having a particle emitted and striking within a defined square centimeter within a random 10ns active period and even during the entire period of 130 ns is $1.30\text{x}10^{-3}$. Multiply that value by the die area to determine the probability of a particle striking the die; $1.30\text{x}10^{-3}$ particles/cm^2 * 2.477 10^{-2} cm^2 = $3.22\text{x}10^{-5}$. We don't know exactly at what pulse this particle will be irradiating the DUT. The random nature of that emission will change the elapsed time between any two consecutive particles. The higher the beam's frequency or the flux; the higher is the likelihood to have more than one particle hitting the DUT in a very short time (within hundreds of nanoseconds). Indeed, the minimum time that is guaranteed by the facility to separate the occurrences of two particles can be as low as 130 ns but the probability of that happening is very low. To avoid overlapping of events, it is important then that the error-events last less than 130 ns or that the flux is much reduced.

Most importantly, in the case of these analog devices (power, signal conditioning, etc.), some of the DUT's transistors when hit by heavy-ions will cause wide SETs that might last for microseconds. To make sure that the error-rate calculation is accurate, the flux needs to be reduced until there is a consistency in the number of detected errors with the flux for a given ions' fluence. If that's not the case, the part is subject to multiple hits or SET widening from the peripheral parasitic. In these types of circuits, it is most likely to be the latter. The test engineer needs to account for the SET widening that the peripheral RC filters are causing. In other terms, if the original SET is widened at the DUT output, by the peripheral RC circuits or even the ones used to mitigate it, then the resulting event will dictate the maximum flux to be applied on the DUT. For instance, if the original SET is 600ns wide, while the mitigated SET is 200us (although with much lower amplitude) then the flux while testing the mitigated design should be less than 5E3 particles/cm²/sec.

Although the traditional obvious solution is to use RC filters, SET mitigation solutions such as the ones based on using guard-gate solutions for analog circuits might be more suitable in some cases as they will mitigate the SET without widening it [4]. As a result, comparators can keep their original fast response advantage but at the same time be SEE immune.

During the RH1011M SEU tests, we have noticed that there are usually three flux regions: 1) a threshold flux where for any flux below that value, the probability of multiple hits (double or higher) is extremely low and therefore negligible, 2) an instable region where the increase of the flux at a given LET and a given fluence will increase the SEE cross-sections almost linearly, and 3) a plateau or saturation region where the part is saturated meaning that the number of multiple hits won't make any difference anymore as the part has reached its saturation. Measured SEE cross-sections that will correlate best with orbital error-rates in space environment should use a flux that is lower than the threshold flux (region 1).

We have observed dependence of the SEE sensitivity on the flux in the case of the RH1011M. When operating the part in the hysteresis region (between 550 and 615mV), the error-signature of the comparator will change from an SET to an SEU at fluxes that are higher than 4E+3 particles/cm^2/sec, which is an artificial effect of the high beam fluxes, that won't be seen in space environments where ions fluxes are extremely low. In this case, this effect was expected as the PW of the detected SETs, with 10uF at the comparator output, were about 200us. Laser tests showed the same results when we increased the laser repetition rate (LRR). They also showed the effect of consecutive events even at low LRR. Indeed, in the hysteresis region, with low LRR, if we don't remove the laser injection, an SET will become an SEU after many injected laser pulses, showing the impact of the internal die and the circuit parasitic, in changing the shape of the propagated SET, if they did not fully recover from the previous laser injection. The laser test results showed 1) the effects of varying the laser repetition rate (equivalent to flux) and 2) the effects of consecutive injections even at low LRR (eq. to low fluxes). Single-shot SETs are then needed to avoid the overwhelming of the circuit's intrinsic and cross-coupling capacitances and mimic the real space environment fluxes. The run average and maximum fluxes during the heavy-ions tests are reported in Tables 2 and 3.

4. Radiation Test Results

Heavy-ions SEE experiments included SET, SEU and SEL tests up to an LET of 114 MeV.cm^2/mg at elevated temperatures (to case temperatures of 100°C). The RH1011M parts were irradiated under various bias conditions in 172 runs. Because of the cabling between the SEE test board and the scope, that adds a minimum capacitive load on the output signal of about 250pF, the 1nF input capacitances, the serial resistances on the comparator inputs and the feedback path (resistances and capacitances), the final measured SET-PW on the scope can be much wider than the initial SET-PW originating from the DUT output. Ideally, the SET-PW on the DUT output should be about the comparator response time, which is less than 400ns at a 1V maximum step-size [2]. Once the hit input transistor has trigged to the ion's deposited charge, the part will need approximately the sum of the circuit response time (about 400ns) to rising and falling edges (Figs. 9 and 10).

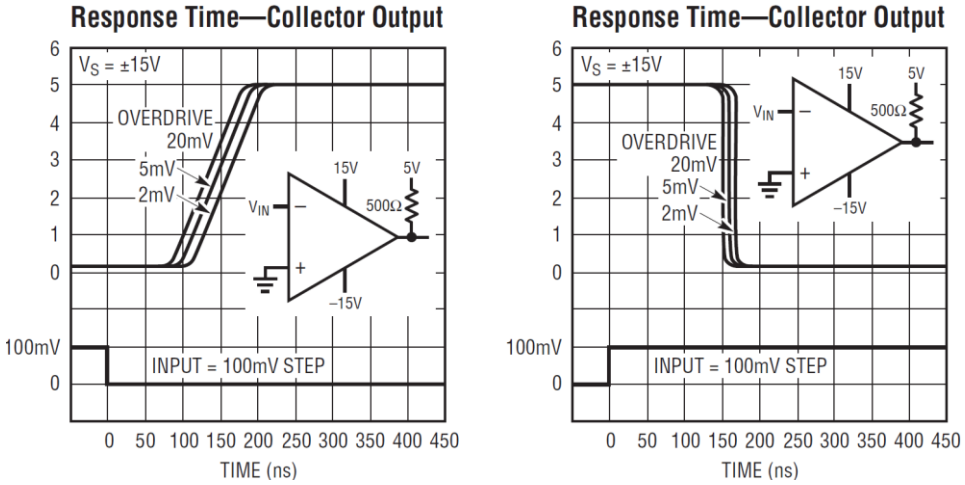

Fig. 9: DUT Responses Times to 100mV Rising and Falling Input Steps (Y-axis units are in Volts)

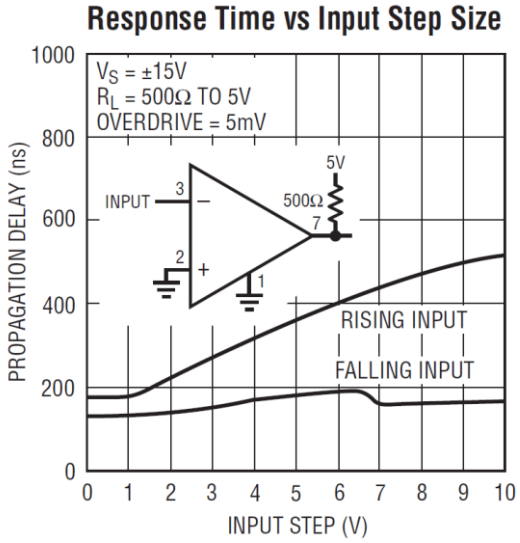

Fig. 10: Propagation Delay vs. Input Size

Furthermore, for SETs that have a voltage increase (negative edge) or voltage drop (positive edge) that is higher than 1V, for instance 5V, the comparator response time will increase to about 600ns, as shown in Fig. 10. The resulting SET will be widened by the BNC cables eq. capacitive load, hence the wide observed SETs (up to 2us) even when we don't use a filtering capacitance. The heavier is the ion, the larger are the deposited charge and its diffusion, the higher is the SET amplitude and hence the wider is the comparator response time to the SET.

In addition, in the hysteresis region between 550 and 615mV (Fig. 11), the comparator output signal depends on the input voltage levels as well as on the current output state. If the inverting input signal is lower than 550mV, the output state will remain high (5V), but if higher than 615mV, the output state will toggle low (0V), independently of the current output state. Between 550 and 615mV, if the current output state is high, the output remains high. Once it exceeds 610mV, the output voltage will flip from 5 to 0V. However, when decreasing the input voltage to a value that is higher than 550mV, the output will remain low and will flip high only when the input bias drops below 550mV. In-beam, this might seem as an SEU.

Indeed, if the initial input voltage is at 575mV and the output voltage is at 5V, an ion hit that will trigger an SET with negative 5V amplitude will toggle the output voltage from 5 to 0V and keep it at 0V even after the complete diffusion of the SET effect. The only way to toggle the output high is to power-cycle the comparator or to drop the input voltage below 550mV. It is then not recommended to operate or test it in this region, as it should be. This can also be reproduced on the bench without radiation, by varying the input supply voltage and monitoring the output. Note that the designer can change the voltage settings for this region by varying the resistance values of R7 and R8, shown in Fig. 5. For instance, decreasing these values from 50 to 5 Kohms, will shift this region from (550 to 615 mV) to (2.575 to 2.635V). In the following, SEU Data is shown for information only and are used to demonstrate the dependence of the SEU cross-sections on the flux.

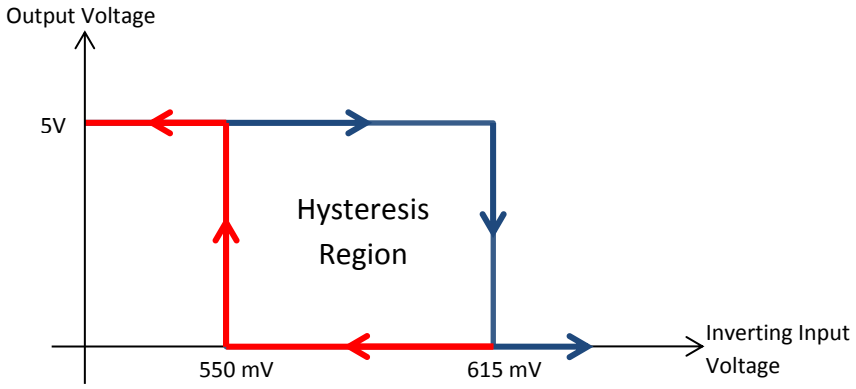

Fig. 11: A Comparator Output Voltage vs. Input Voltage in the Hysteresis Region, when the non-inverting input voltage is at 550mV

1) *False SEU Detection in the Hysteresis Region*

The SEU tests consisted of varying the input voltage levels from 550 to 615mV (hysteresis region) and observing the output state. Upsets have only been observed for non-inverting input voltage ranging between 575 and 615mV; this part can then be considered SEU immune. As shown in Fig. 12, increasing the flux from (1E4p/cm2) to (8E5p/cm2) increased the "SET-induced SEU" cross-section by an order of magnitude. This is simply the result of SET widening caused by the DUT and the circuit peripheral parasitic. In this case, it is the latter that causes the overlapping of the latent effects of consecutive SETs. As the next event occurs before the complete capacitor charge/discharge due to the previous transient, the part will accumulate the effects of consecutive events at high fluxes, similar to the effects of METs (Multiple Event Transients). If these parasitic are defeated by the SET and cannot filter it, they will reduce its amplitude but widen it [4].

The same principle applies to the internal die structures, these analog circuits have big capacitance values that are also widening internally these events and therefore need adequate time to completely propagate the event to the DUT output. Note that at a flux of 2E5p/cm^2, we have not seen any SEU up to a fluence of 1E8p/cm^2. At this moment, we don't know the reasons behind this. Once the maximum SET-PW has been measured (600ns if we don't consider the widening effects from the parasitic circuits), SET mitigation can be achieved by using the most adequate RC filter at the comparator output. During the beam tests, the run fluxes should be reduced to account for this. Since this part is only SET sensitive, only SET-data will be discussed in the remainder of this report.

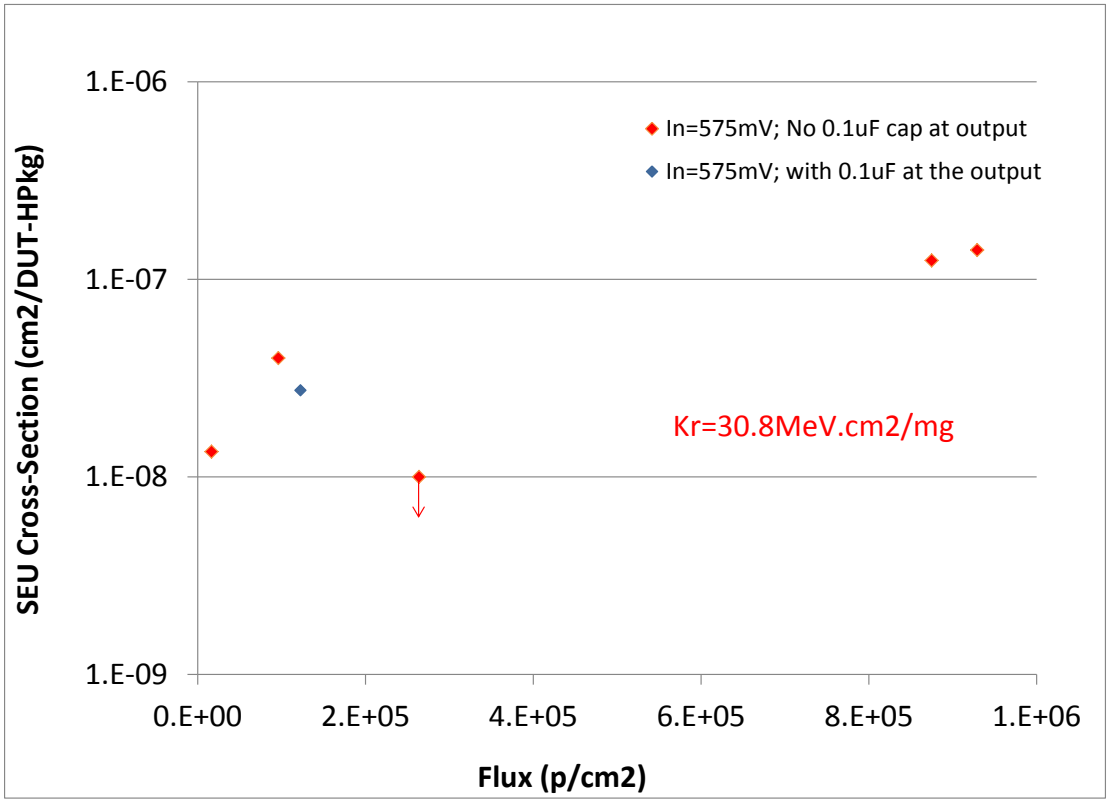

Fig. 12: SEU Cross-Section vs. Beam Flux when operating the RH1011MH in the Hysteresis Region, (Hysteresis board is shown in Fig. 5)

2) SET Detection Without Filtering (Without a capacitance at the Output Signal)

For SET detection, using the Hysteresis board, the beam tests consisted of varying the input voltage from 50 to 1000 mV and triggering the scope on positive and negative SETs occurring on the comparator output signal. For negative SET detection, the scope was set to trigger on switching negative pulse width from 5V to lower than 4.3V. For positive SET detection, the scope was set to trigger on an amplitude increase of about 1V from 200mV. The raw heavy-ion test results are summarized in Tables 2 and 3, showing SET sensitivities on the output. The data showed two SET-types. The first SET-type is short and of small amplitude, as shown in Fig. 13. The second SET-type was as wide as 2us, as shown in Fig. 14, while its cross-sections varied with the inverting input bias, which is proportional to the differential input voltage as the non-inverting input voltage is fixed.

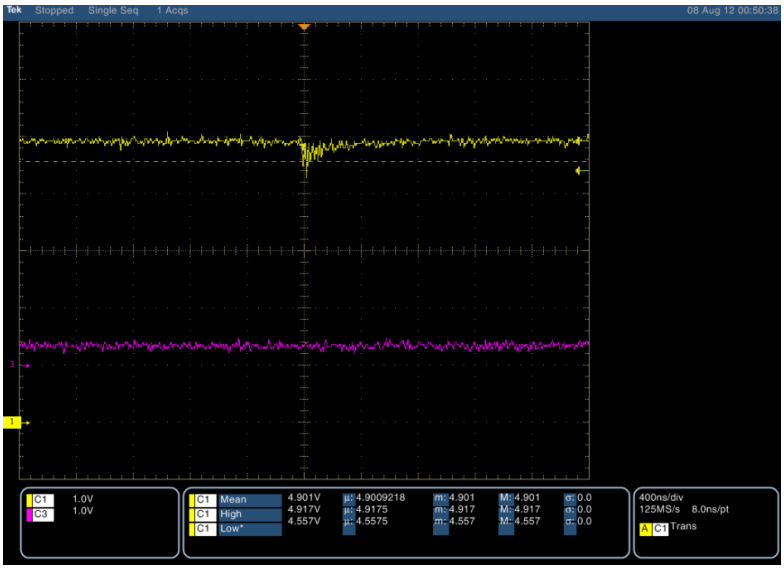

Fig. 13: Short SET on the DUT Output; Vin=450mV; Vout=5V - Run 27; Case Temperature = 34.5°C

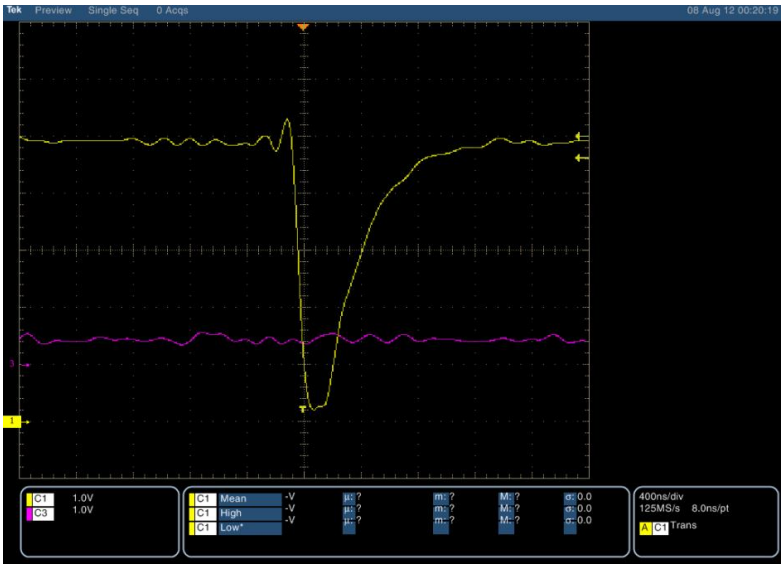

Fig. 14: Wide SET on the DUT Output; Vin=450mV; Vout=5V - Run 27; Case Temperature = 34.5°C

Under heavy-ion irradiations, with various differential input bias conditions, the RH1011M showed small sensitivities to SETs. Figs. 15 to 19 summarize the SET cross-sections at various biases. The measured SET sensitive cross-section is about 1.6% of the total die's area. Because of the small difference in the offset voltage (VOS) with temperature (2mV at room and 4mV at 125°C), the SEE test results were not dependent on the temperature. However, when the comparator differential input voltage is very close to the offset voltage (VOS) in the case of the VOS board or the inverting input bias close to the hysteresis boundary voltages in the case of the hysteresis board, the SET pulse-width (PW) is the widest, and the measured SET cross-sections are the highest. The inverting input bias (at test point E6, Fig. 5) is proportional to the differential input bias as the non-inverting input bias is fixed, in the case of the hysteresis board and grounded in the case of the VOS board. Hence, the lower the comparator input differential bias is, the higher the SET cross-section is. Generally, the smaller is the comparator differential input bias, or the closer we are to the hysteresis region, the higher are the part's susceptibility to trigger and the resulting SET cross-sections [3]. At higher LET near the limiting cross-section, the dependence on differential input bias becomes less significant, as most SETs become wide.

The SET cross-sections dependence on these biases could simply be due to the peripheral capacitances charge/discharge times, so what might seem as bias dependence is truly related to parasitic time constants. We believe that the initial SET-PW will depend on the circuit response and the flux but its propagation on its parasitic and the ion's diffusion [4]. Note that the addition of the C6 capacitance in the feedback path did not make a difference in the overall SET cross-sections.

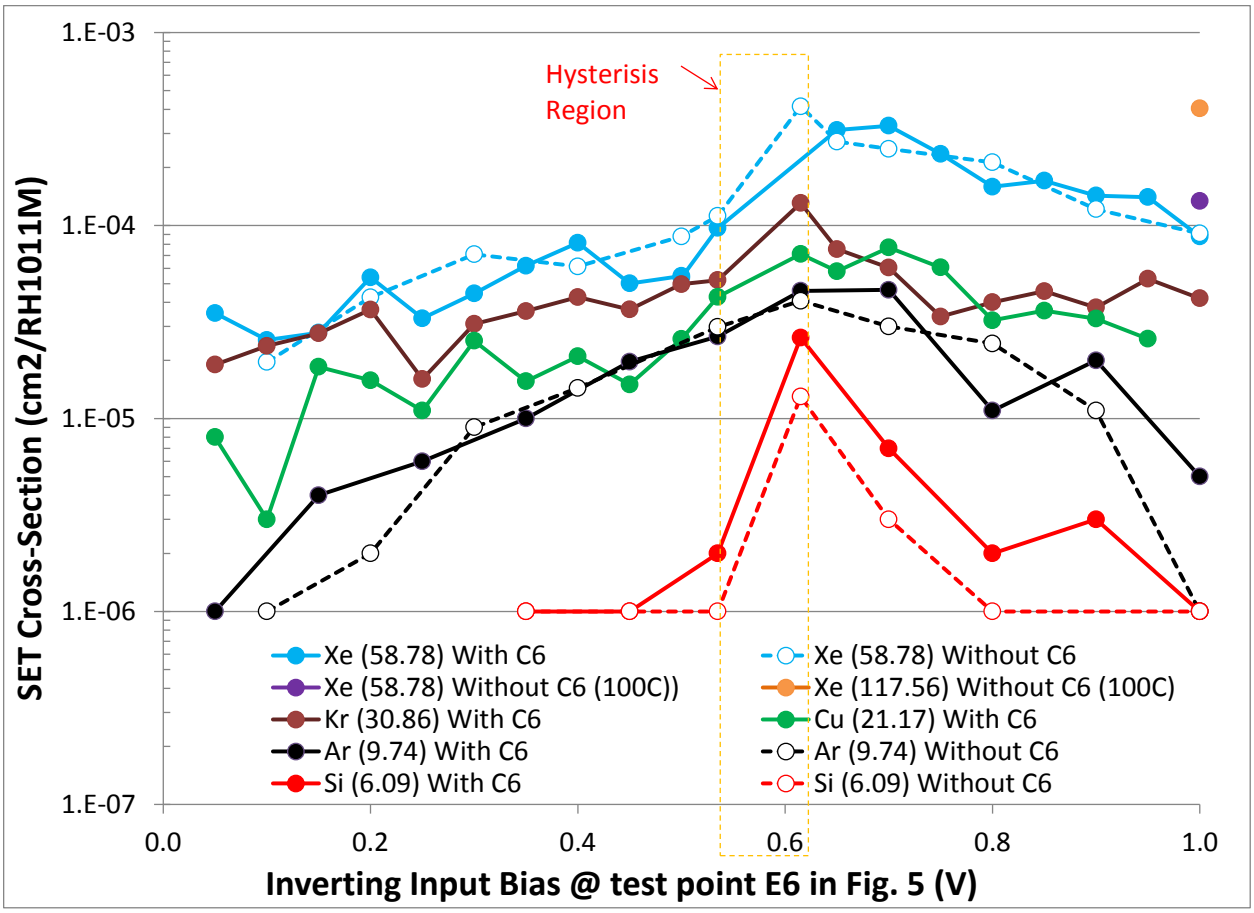

Fig. 15: Measured SET Cross-Sections, Using the Hysteresis Board, without Filtering vs. Inverting Input Bias (at test point E6, Fig. 5), LET, Temperature, With and Without C6 Capacitor

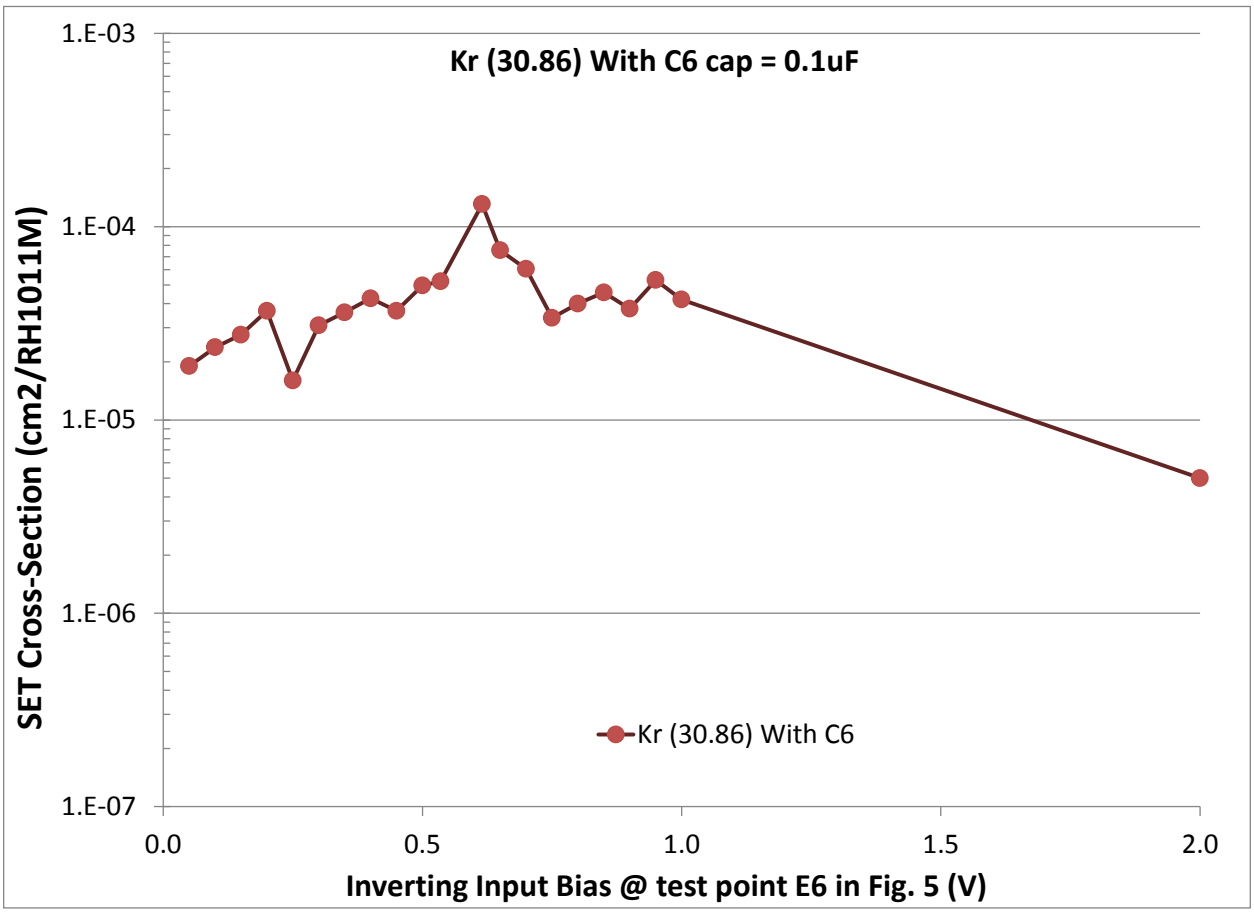

Fig. 16: Measured SET Cross-Sections, Using the Hysteresis Board vs. Inverting Input Bias. This graph shows clearly the SET cross-sections dependence on the inverting input bias when used in the hysteresis configuration. In this case, the inverting input bias (at test point E6, Fig. 5) is proportional to the differential input bias as the non-inverting input bias is fixed. Hence, the lower the comparator input differential bias is, the higher the SET cross-section is.

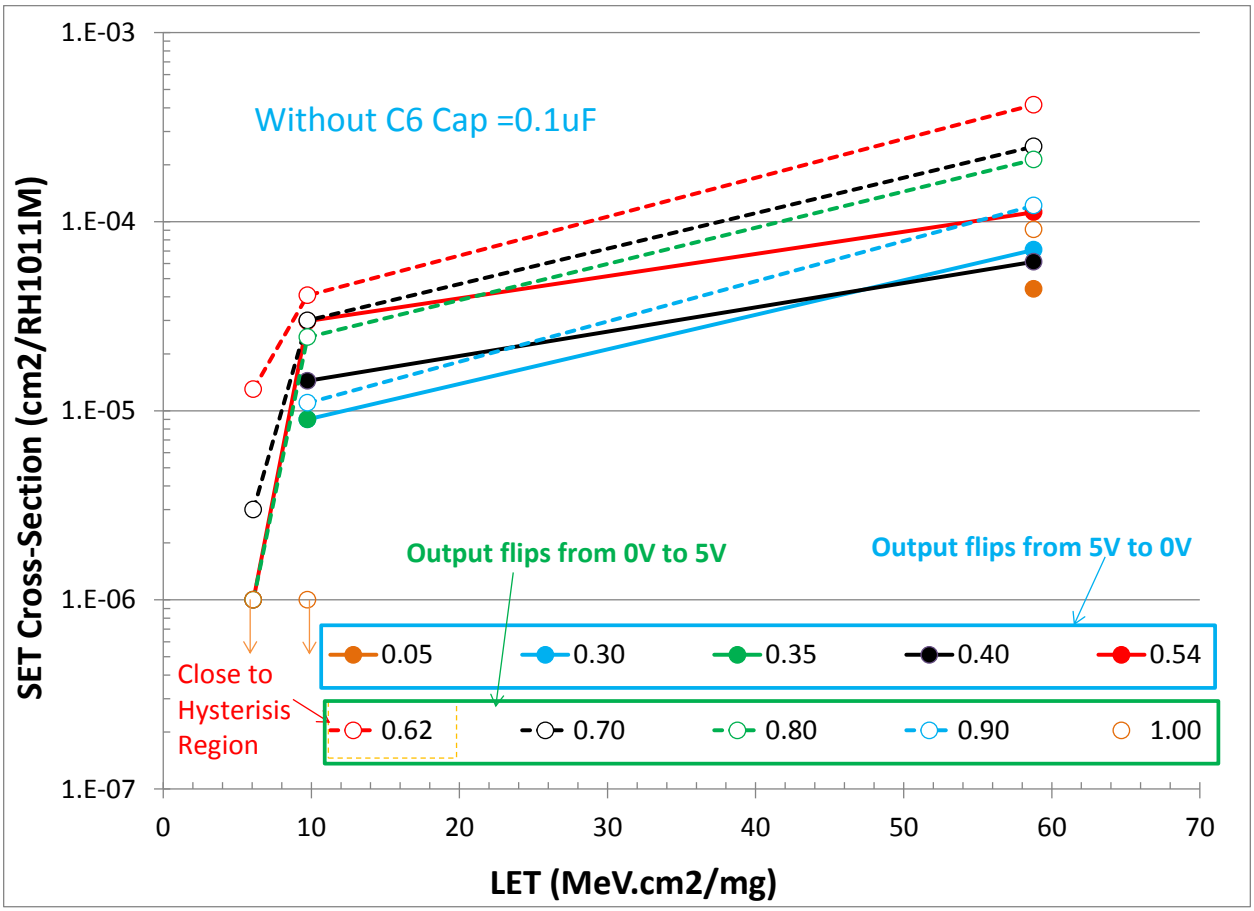

Fig. 17: Measured SET Cross-Sections, Using the Hysteresis Board vs. LET, and the Inverting Input Bias at Test Point E6 (Fig. 5), without the capacitance C6

Arrows pointing down are indication of no observed SETs up to that fluence at a given LET

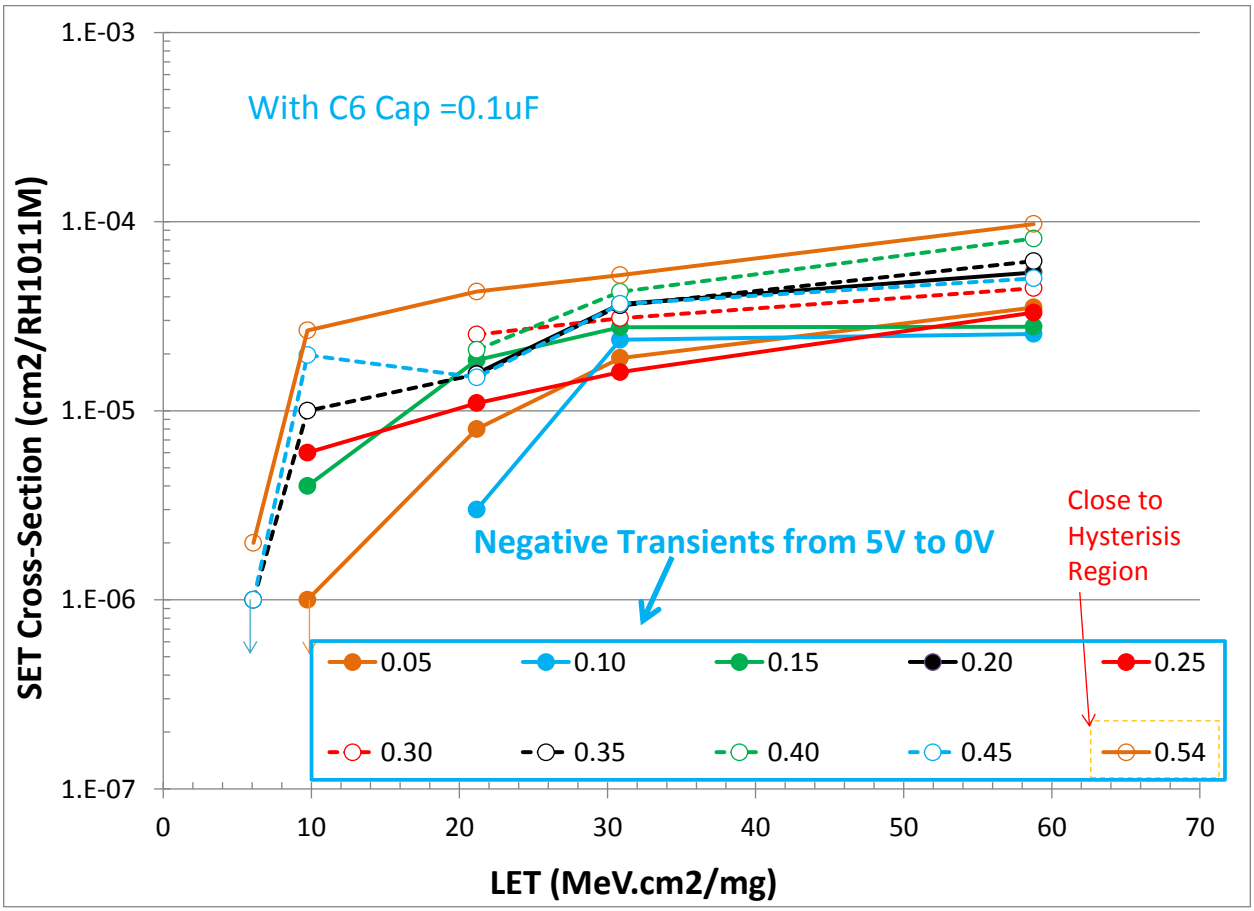

Fig. 18: Measured SET Cross-Sections, Using the Hysteresis Board vs. LET, and the Inverting Input Bias at Test Point E6 (Fig. 5), using the capacitance C6

Arrows pointing down are indication of no observed SETs up to that fluence at a given LET

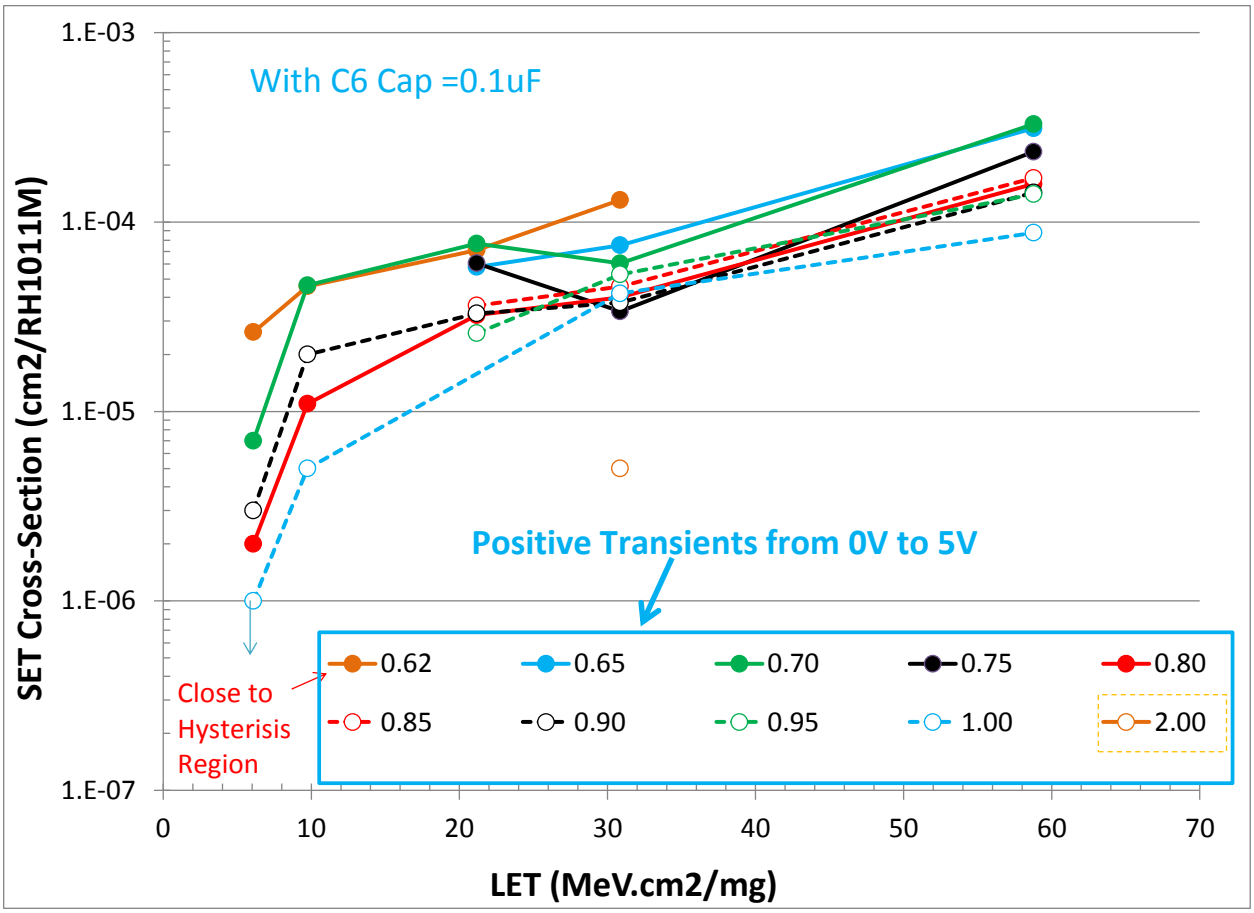

Fig. 19: Measured SET Cross-Sections, Using the Hysteresis Board vs. LET, and the Inverting Input Bias at the Test Point E6 (Fig. 5)

Arrows pointing down are indication of no observed SETs up to that fluence at the tested LET

This does not eliminate the possibility of noise for the second type of SETs as once the noise levels have caused the device in a circuit to trigger, its propagation will mostly depend on its layout and parasitic (capacitive load and resistances). In such a circuit, the capacitive load is high and will cause the resulting SET to become as wide as the maximum circuit response time. As mentioned above, the cabling capacitance, the feedback path and the two parallel input capacitances in serial with the resistances at the comparator inputs will make all the difference. A good printed circuit board designed to be minimally sensitive to noise, electromagnetic effects, with no ground loops, etc. is required for the SEE tests of such type of circuits.

3) SET Detection With Filtering (with a 0.1uF capacitance at the Output Signal)

For mitigation purposes, we've run the beam experiments with an equivalent capacitance at the output signal of 0.1uF on the hysteresis board and 22nF on the VOS board. Fig. 20 shows an example of SET on the output signal. In both cases, SETs were fully-mitigated with the added output capacitance up to an LET of 114 MeV/cm^2/mg and high temperature of 100°C on the sense transistor, as shown in Tables 2 and 3. Fig. 21 shows that a 22nF was sufficient to fully mitigate large amplitude and wide SETs. However, based on additional laser tests, we have demonstrated that a larger capacitance (0.1uF) was needed in the hysteresis board but not in the VOS board, showing that the feedback path was widening these SETs.

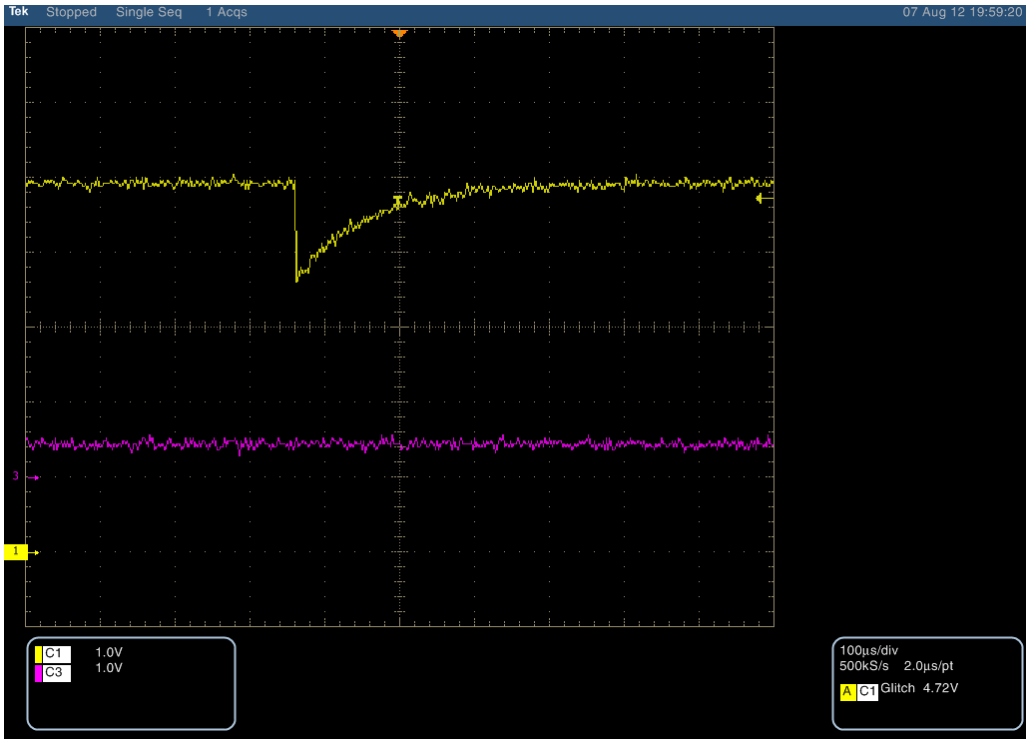

Fig. 20: SET Waveform with SET filtering (using 0.1uF) on the DUT Output; Vin=450mV; Vout=5V; Case Temperature = 34.5°C

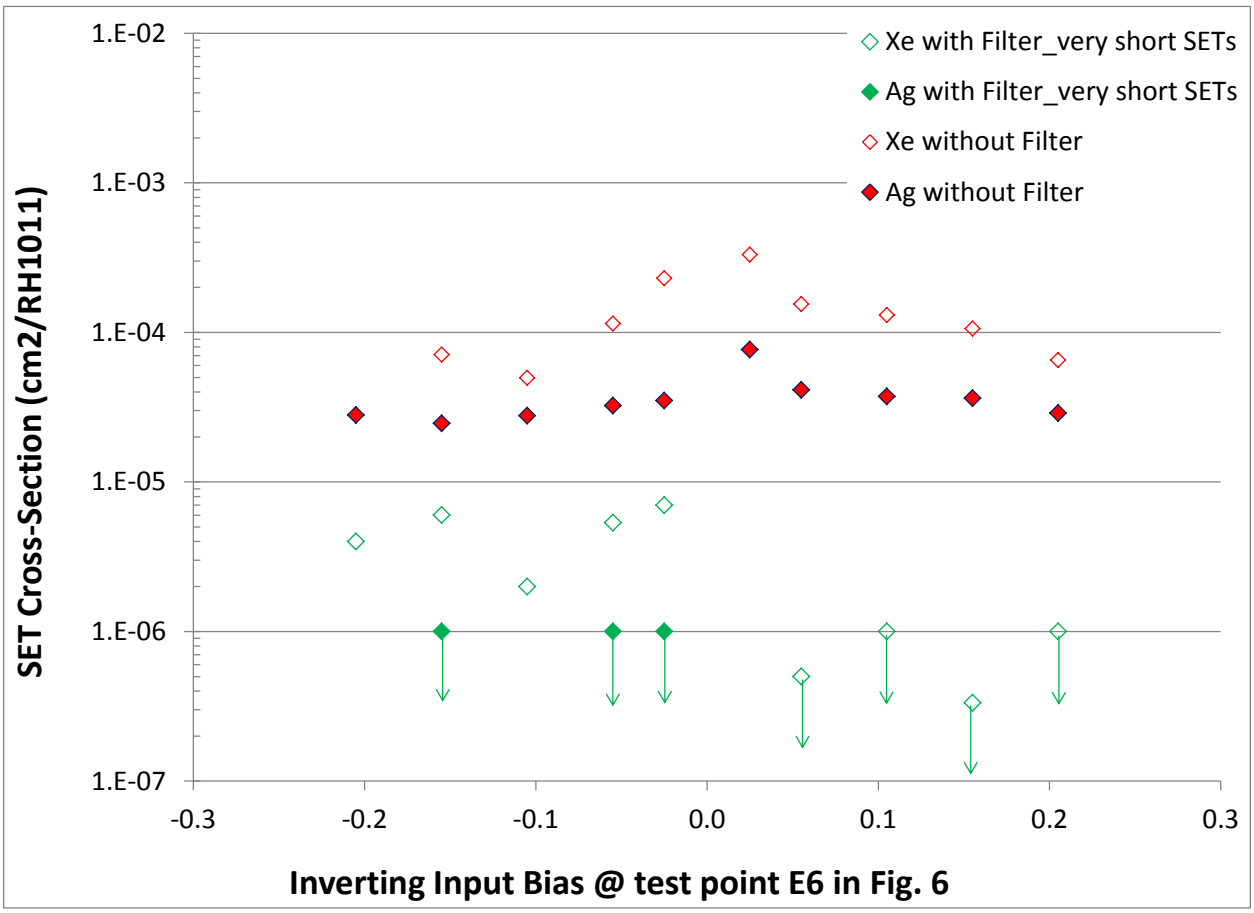

Fig. 21: Measured SET Cross-Sections, Using the VOS Board (Fig. 6, at test point E6), vs. Inverting Input Bias, LET, with and without 22nF capacitance at the comparator output. In this case, the negative voltage corresponds to the inversion of the bias polarity of the non-inverting input of the comparator

Arrows pointing down are indication of no observed SETs up to that fluence at tested LET

4) SET Cross-sections With/Without Filtering at hot (100°C)

With 0.1uF at the comparator's output and at high temperature (100°C) at the DUT case, the test results (green circles in Fig. 22) showed no SET sensitivities at the output voltage up to an LET of 114 MeV.cm^2/mg. Without this filtering capacitance, at an LET of 114 MeV.cm^2/mg, the measured limiting cross-section is 4x10^{-4} cm^2/die. This means that the sensitive cross-section on the part is about 4x10^{-2} mm^2, which is about 1.6% of the total die's area (2.477 mm^2).

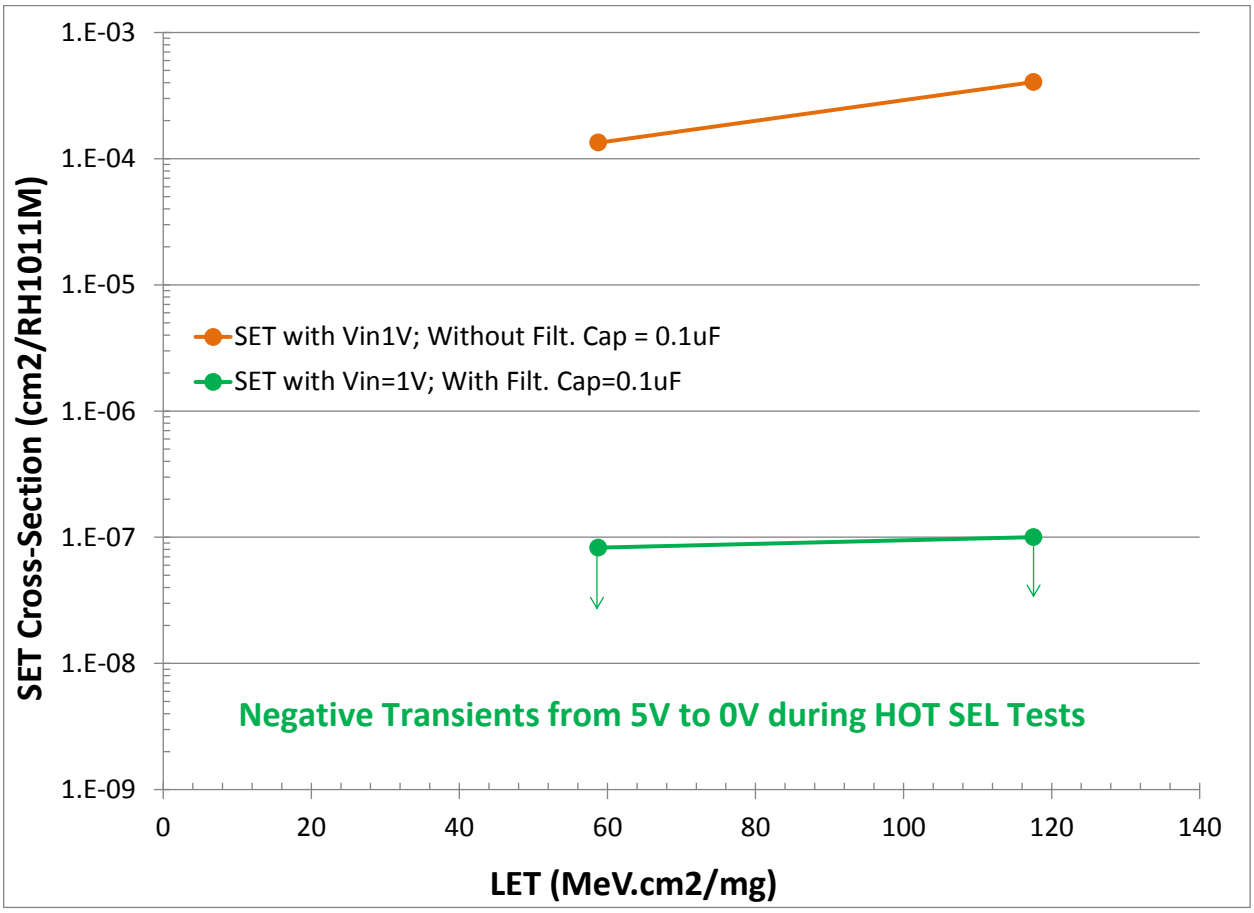

Fig. 22: Measured SET Cross-Sections vs. LET, Inverting Input Bias, and Temperature, with and without Filtering Capacitor (C18=0.1uF) at the Comparator Output

Arrows pointing down are indication of no observed SETs up to that fluence at tested LET

5) SEL Immunity With/Without Filtering (w/o capacitance at the Output Signal)

With 0.1uF at the comparator's output and at high temperature (100°C) at the DUT case, the test results (green circles in Fig. 23) showed immunity to SELs up to an LET of 114 MeV.cm^2/mg.

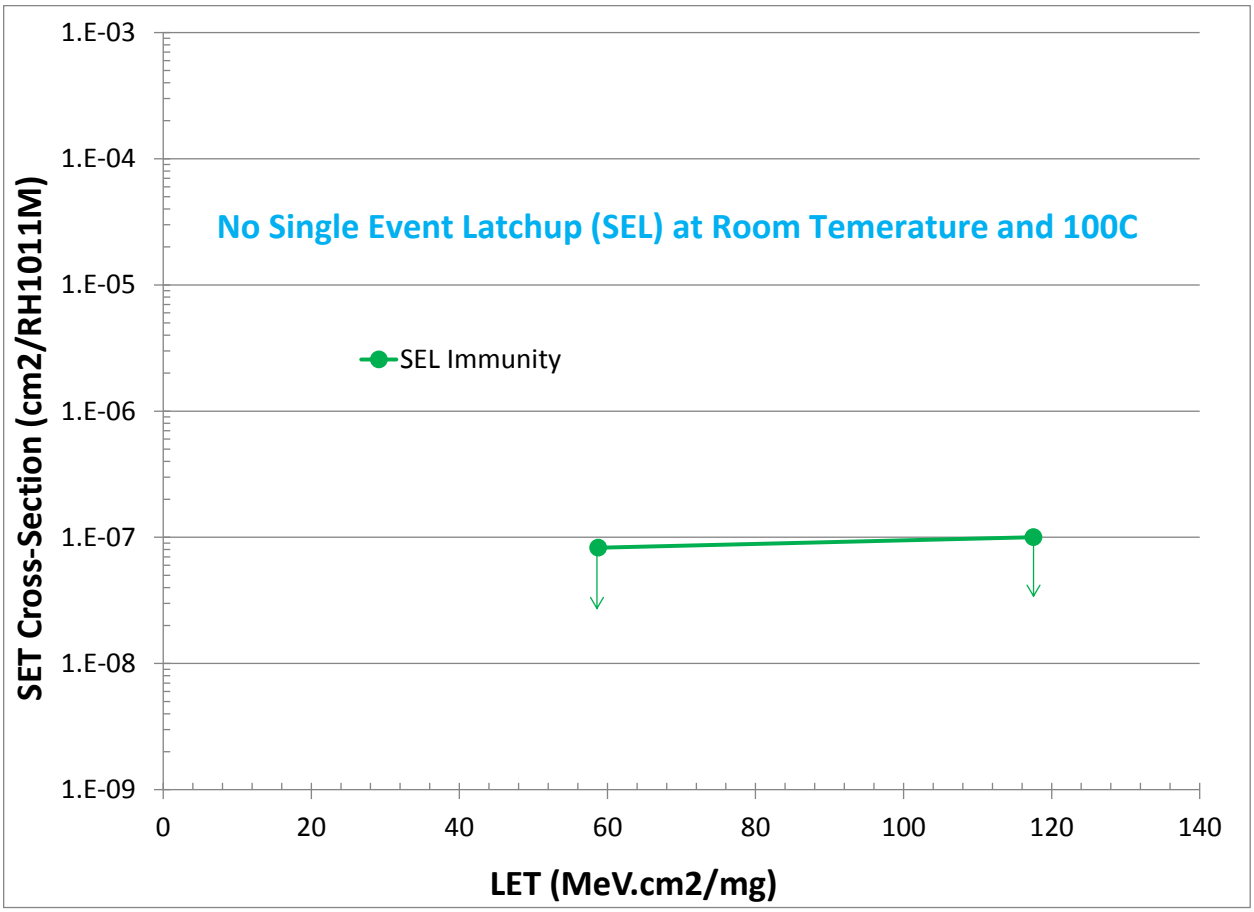

Fig. 23: Measured SEL Cross-Sections vs. LET, showing the comparator immunity to SELs

Arrows pointing down are indication of no observed SETs up to that fluence at tested LET

Table 2: Raw Data for the Heavy-Ion Beam Runs (Hysteresis Board)

Run	Design	DUT	Tb (Vacuum)	Vin	Inv. Input Bias	Vout	Trig Vout	Ion	Tilt Angle	Effective LET	Effective Fluence	Average Flux	Maximum Flux	TID (Run)	TID (Cumulative)	#SET	SET Cross-Section
			(°C)	(V)	(V)	(V)	(V)		degrees	MeV.cm2/mg	p/cm2	p/sec/cm2	p/sec/cm2	rads(Si)	rads(Si)		cm2/circuit
1	No Filtering	1	27	5.40	0.54	5	4.36	Xe	0	58.78	2.06E+05	1.61E+03	4.43E+03	1.94E+02	1.94E+02	20	9.71E-05
2	//	1	32	5.05	0.50	5	4.36	Xe	0	58.78	4.02E+05	1.88E+03	4.62E+03	3.78E+02	5.72E+02	22	5.47E-05
3	//	1	32	4.55	0.45	5	4.36	Xe	0	58.78	3.99E+05	1.64E+03	1.76E+03	3.75E+02	9.47E+02	20	5.01E-05
4	//	1	32	4.05	0.40	5	4.36	Xe	0	58.78	2.46E+05	1.68E+03	1.82E+03	2.31E+02	1.18E+03	20	8.13E-05
5	//	1	32	3.55	0.35	5	4.36	Xe	0	58.78	3.56E+05	1.37E+03	1.85E+03	3.35E+02	1.51E+03	22	6.18E-05
6	//	1	32	3.05	0.30	5	4.36	Xe	0	58.78	4.50E+05	1.95E+03	4.74E+03	4.23E+02	1.94E+03	20	4.44E-05
7	//	1	32	2.55	0.25	5	4.36	Xe	0	58.78	6.36E+05	1.56E+03	1.70E+03	5.98E+02	2.53E+03	21	3.30E-05
8	//	1	32	2.05	0.20	5	4.36	Xe	0	58.78	3.90E+05	1.79E+03	4.81E+03	3.67E+02	2.90E+03	21	5.38E-05
9	//	1	32	1.55	0.15	5	4.36	Xe	0	58.78	7.19E+05	1.63E+03	3.75E+03	6.76E+02	3.58E+03	20	2.78E-05
10	//	1	32	1.05	0.10	5	4.36	Xe	0	58.78	8.24E+05	1.61E+03	4.51E+03	7.75E+02	4.35E+03	21	2.55E-05
11	//	1	32	0.55	0.05	5	4.36	Xe	0	58.78	5.97E+05	1.72E+03	4.29E+03	5.61E+02	4.91E+03	21	3.52E-05
12	//	1	32	5.05	0.50	5	4.36	Xe	0	58.78	3.73E+05	1.66E+03	1.81E+03	3.51E+02	5.26E+03	20	5.36E-05
16	//	1	34.5	6.55	0.65	0	1	Xe	0	58.78	6.40E+04	3.81E+02	4.50E+02	6.02E+01	5.43E+03	20	3.13E-04
17	//	1	34.5	7.05	0.70	0	1	Xe	0	58.78	6.08E+04	1.55E+02	4.68E+02	5.72E+01	5.49E+03	20	3.29E-04
18	//	1	34.5	7.55	0.75	0	1	Xe	0	58.78	8.51E+04	3.27E+02	4.73E+02	8.00E+01	5.57E+03	20	2.35E-04
19	//	1	34.5	8.05	0.80	0	1	Xe	0	58.78	1.26E+05	3.55E+02	4.70E+02	1.19E+02	5.69E+03	20	1.59E-04
20	//	1	34.5	8.55	0.85	0	1	Xe	0	58.78	1.23E+05	5.36E+02	8.92E+02	1.16E+02	5.80E+03	21	1.71E-04
21	//	1	34.5	9.05	0.90	0	1	Xe	0	58.78	1.40E+05	8.07E+02	2.17E+03	1.32E+02	5.94E+03	20	1.43E-04
22	//	1	34.5	9.55	0.95	0	1	Xe	0	58.78	2.85E+05	7.52E+02	8.82E+02	2.68E+02	6.20E+03	40	1.40E-04

23	//	1	34.5	10.05	1.00	0	1	Xe	0	58.78	2.85E+05	7.62E+02	8.85E+02	2.68E+02	6.47E+03	25	8.77E-05
Run	**Design**	**DUT**	**Tb (Vacuum)**	**Vin**	**Inv. Input Bias**	**Vout**	**Trig Vout**	**Ion**	**Tilt Angle**	**Effective LET**	**Effective Fluence**	**Average Flux**	**Maximum Flux**	**TID (Run)**	**TID (Cumulative)**	**#SET**	**SET Cross-Section**
			(°C)	(V)	(V)	(V)	(V)		degrees	MeV.cm2/mg	p/cm2	p/sec/cm2	p/sec/cm2	rads(Si)	rads(Si)		cm2/circuit
28	//	1	34.5	4.55	0.45	5	4.32	Kr	0	30.86	5.45E+05	1.10E+03	2.06E+03	2.69E+02	7.31E+03	20	3.67E-05
29	//	1	34.5	4.05	0.40	5	4.32	Kr	0	30.86	4.70E+05	1.04E+03	1.18E+03	2.32E+02	7.55E+03	20	4.26E-05
30	//	1	34.5	3.55	0.35	5	4.32	Kr	0	30.86	6.11E+05	1.04E+03	1.77E+03	3.02E+02	7.85E+03	22	3.60E-05
31	//	1	34.5	3.05	0.30	5	4.32	Kr	0	30.86	6.80E+05	1.00E+03	1.94E+03	3.36E+02	8.18E+03	21	3.09E-05
32	//	1	34.5	2.55	0.25	5	4.32	Kr	0	30.86	1.00E+06	9.82E+02	1.69E+03	4.94E+02	8.68E+03	16	1.60E-05
33	//	1	34.5	2.05	0.20	5	4.32	Kr	0	30.86	6.27E+05	1.08E+03	1.79E+03	3.10E+02	8.99E+03	23	3.67E-05
34	//	1	34.5	1.55	0.15	5	4.32	Kr	0	30.86	7.24E+05	1.08E+03	1.89E+03	3.57E+02	9.34E+03	20	2.76E-05
35	//	1	34.5	1.05	0.10	5	4.32	Kr	0	30.86	8.42E+05	1.04E+03	1.21E+03	4.16E+02	9.76E+03	20	2.38E-05
36	//	1	34.5	0.55	0.05	5	4.32	Kr	0	30.86	1.00E+06	1.04E+03	1.22E+03	4.94E+02	1.03E+04	19	1.90E-05
37	//	1	34.5	6.20	0.62	0	1	Kr	0	30.86	7.19E+05	1.02E+03	1.67E+03	3.55E+02	1.06E+04	94	1.31E-04
38	//	1	34.5	6.55	0.65	0	1	Kr	0	30.86	4.64E+05	9.04E+02	1.14E+03	2.29E+02	1.08E+04	35	7.54E-05
39	//	1	37	7.05	0.70	0	1	Kr	0	30.86	4.63E+05	9.64E+02	1.62E+03	2.29E+02	1.11E+04	28	6.05E-05
40	//	1	37	7.55	0.75	0	1	Kr	0	30.86	5.93E+05	8.93E+02	1.15E+03	2.93E+02	1.14E+04	20	3.37E-05
41	//	1	37	8.05	0.80	0	1	Kr	0	30.86	5.25E+05	9.56E+02	1.86E+03	2.59E+02	1.16E+04	21	4.00E-05
42	//	1	37	8.55	0.85	0	1	Kr	0	30.86	4.60E+05	9.30E+02	1.20E+03	2.27E+02	1.18E+04	21	4.57E-05
43	//	1	37	9.05	0.90	0	1	Kr	0	30.86	5.32E+05	9.48E+02	1.17E+03	2.63E+02	1.21E+04	20	3.76E-05
44	//	1	37	9.55	0.95	0	1	Kr	0	30.86	3.78E+05	8.63E+02	1.10E+03	1.87E+02	1.23E+04	20	5.29E-05
45	//	1	37	10.05	1.00	0	1	Kr	0	30.86	4.05E+05	1.01E+03	1.76E+03	2.00E+02	1.25E+04	17	4.20E-05
46	//	1	37	20.05	2.00	0	1	Kr	0	30.86	1.00E+06	9.88E+02	1.98E+03	4.94E+02	1.30E+04	5	5.00E-06

47	//	1	39.5	5.40	0.54	5	4.32	Cu	0	21.17	6.09E+05	1.10E+03	1.31E+03	2.06E+02	1.32E+04	26	4.27E-05
48	//	1	39.5	5.05	0.50	5	4.32	Cu	0	21.17	8.14E+05	1.16E+03	1.29E+03	2.76E+02	1.35E+04	21	2.58E-05
Run	**Design**	**DUT**	**Tb (Vacuum)**	**Vin**	**Inv. Input Bias**	**Vout**	**Trig Vout**	**Ion**	**Tilt Angle**	**Effective LET**	**Effective Fluence**	**Average Flux**	**Maximum Flux**	**TID (Run)**	**TID (Cumulative)**	**#SET**	**SET Cross-Section**
			(°C)	(V)	(V)	(V)	(V)		degrees	MeV.cm2/mg	p/cm2	p/sec/cm2	p/sec/cm2	rads(Si)	rads(Si)		cm2/circuit
51	//	1	39.5	3.55	0.35	5	4.32	Cu	0	21.17	7.06E+05	1.24E+03	1.40E+03	2.39E+02	1.44E+04	11	1.56E-05
52	//	1	39.5	3.05	0.30	5	4.32	Cu	0	21.17	7.12E+05	1.45E+03	5.90E+03	2.41E+02	1.46E+04	18	2.53E-05
53	//	1	39.5	2.55	0.25	5	4.32	Cu	0	21.17	9.11E+05	1.19E+03	6.06E+03	3.09E+02	1.49E+04	10	1.10E-05
54	//	1	39.5	2.05	0.20	5	4.32	Cu	0	21.17	8.25E+05	1.09E+03	1.23E+03	2.79E+02	1.52E+04	13	1.58E-05
55	//	1	39.5	1.55	0.15	5	4.32	Cu	0	21.17	5.40E+05	8.96E+02	2.57E+03	1.83E+02	1.54E+04	10	1.85E-05
56	//	1	39.5	1.05	0.10	5	4.32	Cu	0	21.17	1.00E+06	7.90E+02	1.30E+03	3.39E+02	1.57E+04	3	3.00E-06
57	//	1	39.5	0.55	0.05	5	4.32	Cu	0	21.17	1.00E+06	8.61E+02	2.14E+03	3.39E+02	1.61E+04	8	8.00E-06
58	//	1	39.5	6.20	0.62	0	1	Cu	0	21.17	2.25E+05	7.24E+02	8.30E+02	7.62E+01	1.62E+04	16	7.11E-05
59	//	1	39.5	6.55	0.65	0	1	Cu	0	21.17	2.59E+05	9.41E+02	1.07E+03	8.77E+01	1.62E+04	15	5.79E-05
60	//	1	39.5	7.05	0.70	0	1	Cu	0	21.17	2.08E+05	9.35E+02	1.06E+03	7.05E+01	1.63E+04	16	7.69E-05
61	//	1	39.5	7.55	0.75	0	1	Cu	0	21.17	2.64E+05	8.72E+02	1.04E+03	8.94E+01	1.64E+04	16	6.06E-05
62	//	1	39.5	8.05	0.80	0	1	Cu	0	21.17	3.41E+05	6.83E+02	1.26E+03	1.16E+02	1.65E+04	11	3.23E-05
63	//	1	39.5	8.55	0.85	0	1	Cu	0	21.17	3.59E+05	8.31E+02	1.03E+03	1.22E+02	1.66E+04	13	3.62E-05
64	//	1	39.5	9.05	0.90	0	1	Cu	0	21.17	3.95E+05	1.51E+03	1.90E+03	1.34E+02	1.68E+04	13	3.29E-05
65	//	1	39.5	9.55	0.95	0	1	Cu	0	21.17	3.78E+05	1.64E+03	1.90E+03	1.28E+02	1.69E+04	13	3.44E-05
66	//	1	39.5	9.55	0.95	0	1	Cu	0	21.17	6.27E+05	1.59E+03	1.89E+03	2.12E+02	1.71E+04	13	2.07E-05
67	//	1	39.5	5.40	0.54	5	4.32	Ar	0	9.74	4.89E+05	1.35E+03	1.49E+03	7.62E+01	1.72E+04	13	2.66E-05
68	//	1	39.5	4.55	0.45	5	4.32	Ar	0	9.74	7.11E+05	1.43E+03	3.35E+03	1.11E+02	1.73E+04	14	1.97E-05

69	//	1	39.5	3.55	0.35	5	4.32	Ar	0	9.74	1.00E+06	2.94E+03	3.34E+03	1.56E+02	1.75E+04	10	1.00E-05
70	//	1	39.5	2.55	0.25	5	4.32	Ar	0	9.74	1.00E+06	2.88E+03	3.45E+03	1.56E+02	1.76E+04	6	6.00E-06
71	//	1	39.5	1.55	0.15	5	4.32	Ar	0	9.74	1.00E+06	1.87E+03	4.63E+03	1.56E+02	1.78E+04	4	4.00E-06

Run	Design	DUT	Tb (Vacuum)	Vin	Inv. Input Bias	Vout	Trig Vout	Ion	Tilt Angle	Effective LET	Effective Fluence	Average Flux	Maximum Flux	TID (Run)	TID (Cumulative)	#SET	SET Cross-Section
			(°C)	(V)	(V)	(V)	(V)		degrees	MeV.cm2/mg	p/cm2	p/sec/cm2	p/sec/cm2	rads(Si)	rads(Si)		cm2/circuit
74	//	1	39.5	7.05	0.70	0	1	Ar	0	9.74	3.02E+05	2.28E+03	3.11E+03	4.71E+01	1.80E+04	14	4.64E-05
76	//	1	39.5	8.05	0.80	0	1	Ar	0	9.74	7.01E+05	2.32E+03	6.02E+03	1.09E+02	1.82E+04	7	1.10E-05
77	//	1	39.5	9.05	0.90	0	1	Ar	0	9.74	1.00E+06	2.87E+03	3.21E+03	1.56E+02	1.84E+04	20	2.00E-05
78	//	1	39.5	10.05	1.00	0	1	Ar	0	9.74	1.00E+06	3.00E+03	3.63E+03	1.56E+02	1.85E+04	5	5.00E-06
79	//	1	39.5	5.40	0.54	5	4.32	Si	0	6.09	1.00E+06	1.79E+03	2.48E+03	9.74E+01	1.86E+04	2	2.00E-06
80	//	1	39.5	4.55	0.45	5	4.32	Si	0	6.09	1.00E+06	1.71E+03	2.62E+03	9.74E+01	1.87E+04	0	1.00E-06
81	//	1	39.5	3.55	0.35	5	4.32	Si	0	6.09	1.00E+06	1.11E+03	1.65E+03	9.74E+01	1.88E+04	1	1.00E-06
82	//	1	39.5	6.20	0.62	0	1	Si	0	6.09	3.81E+05	1.06E+03	1.44E+03	3.71E+01	1.88E+04	10	2.62E-05
83	//	1	39.5	7.05	0.70	0	1	Si	0	6.09	1.00E+06	1.28E+03	3.21E+03	9.74E+01	1.89E+04	7	7.00E-06
84	//	1	39.5	8.05	0.80	0	1	Si	0	6.09	1.00E+06	2.12E+03	3.33E+03	9.74E+01	1.90E+04	2	2.00E-06
85	//	1	39.5	9.05	0.90	0	1	Si	0	6.09	1.00E+06	2.59E+03	4.33E+03	9.74E+01	1.91E+04	3	3.00E-06
86	//	1	39.5	10.05	1.00	0	1	Si	0	6.09	1.00E+06	2.33E+03	3.30E+03	9.74E+01	1.92E+04	0	1.00E-06
87	//	1	39.5	5.40	0.54	5	4.32	Si	0	6.09	1.00E+06	2.74E+03	3.37E+03	9.74E+01	1.93E+04	1	1.00E-06
88	//	1	39.5	4.55	0.45	5	4.32	Si	0	6.09	1.00E+06	2.53E+03	3.42E+03	9.74E+01	1.94E+04	1	1.00E-06
89	//	1	39.5	3.55	0.35	5	4.32	Si	0	6.09	1.00E+06	2.84E+03	3.55E+03	9.74E+01	1.95E+04	1	1.00E-06
90	//	1	39.5	6.20	0.62	0	1	Si	0	6.09	1.00E+06	2.30E+03	3.35E+03	9.74E+01	1.96E+04	13	1.30E-05

91	//	1	39.5	7.05	0.70	0	1	Si	0	6.09	1.00E+06	2.10E+03	3.21E+03	9.74E+01	1.97E+04	3	3.00E-06
92	//	1	39.5	8.05	0.80	0	1	Si	0	6.09	1.00E+06	4.49E+03	5.98E+03	9.74E+01	1.98E+04	1	1.00E-06
94	//	1	39.5	10.05	0.90	0	1	Si	-0.3	6.09	1.00E+06	4.90E+03	7.64E+03	9.74E+01	1.99E+04	0	1.00E-06
95	//	1	39.5	5.40	1.00	5	4	Xe	-0.3	58.78	1.77E+05	1.01E+04	1.06E+04	1.66E+02	2.01E+04	0	5.65E-06
96	//	1	39.5	5.40	0.54	5	4	Xe	-0.3	58.78	2.23E+05	1.03E+03	1.16E+03	2.10E+02	2.03E+04	25	1.12E-04
Run	**Design**	**DUT**	**Tb (Vacuum)**	**Vin**	**Inv. Input Bias**	**Vout**	**Trig Vout**	**Ion**	**Tilt Angle**	**Effective LET**	**Effective Fluence**	**Average Flux**	**Maximum Flux**	**TID (Run)**	**TID (Cumulative)**	**#SET**	**SET Cross-Section**
			(°C)	(V)	(V)	(V)	(V)		degrees	MeV.cm2/mg	p/cm2	p/sec/cm2	p/sec/cm2	rads(Si)	rads(Si)		cm2/circuit
99	//	1	39.5	3.05	0.40	5	4	Xe	-0.3	58.78	4.09E+05	1.09E+03	3.26E+03	3.85E+02	2.14E+04	29	7.09E-05
100	//	1	39.5	2.05	0.30	5	4	Xe	-0.3	58.78	3.77E+05	1.05E+03	3.48E+03	3.55E+02	2.18E+04	16	4.24E-05
101	//	1	39.5	1.05	0.20	5	4	Xe	-0.3	58.78	5.61E+05	9.56E+02	1.11E+03	5.28E+02	2.23E+04	11	1.96E-05
102	//	1	39.5	0.55	0.10	5	4	Xe	-0.3	58.78	5.00E+05	1.05E+03	3.43E+03	4.70E+02	2.27E+04	22	4.40E-05
103	//	1	39.5	6.20	0.05	0	1	Xe	-0.3	58.78	1.52E+05	9.02E+02	9.89E+02	1.43E+02	2.29E+04	63	4.14E-04
104	//	1	39.5	6.55	0.62	0	1	Xe	-0.3	58.78	8.45E+04	9.66E+02	1.05E+03	7.95E+01	2.30E+04	23	2.72E-04
105	//	1	39.5	7.05	0.65	0	1	Xe	-0.3	58.78	4.45E+05	9.47E+02	1.06E+03	4.19E+02	2.34E+04	111	2.49E-04
106	//	1	39.5	8.05	0.70	0	1	Xe	-0.3	58.78	2.40E+05	9.03E+02	9.90E+02	2.26E+02	2.36E+04	51	2.13E-04
107	//	1	39.5	9.05	0.80	0	1	Xe	-0.3	58.78	4.69E+05	9.09E+02	3.09E+03	4.41E+02	2.41E+04	57	1.22E-04
108	//	1	39.5	10.05	0.90	0	1	Xe	-0.3	58.78	5.50E+05	8.02E+02	9.26E+02	5.17E+02	2.46E+04	50	9.09E-05
109	//	1	39.5	5.40	1.00	5	4	Ar	-0.3	9.74	7.05E+05	1.68E+03	2.14E+03	1.10E+02	2.47E+04	21	2.98E-05
110	//	1	39.5	4.05	0.54	5	4	Ar	-0.3	9.74	1.46E+06	1.77E+03	2.14E+03	2.28E+02	2.49E+04	21	1.44E-05
111	//	1	39.5	3.05	0.40	5	4	Ar	-0.3	9.74	1.00E+06	1.59E+03	3.05E+03	1.56E+02	2.51E+04	9	9.00E-06
112	//	1	39.5	2.05	0.30	5	4	Ar	-0.3	9.74	1.00E+06	1.63E+03	4.94E+03	1.56E+02	2.52E+04	2	2.00E-06
113	//	1	39.5	1.05	0.20	5	4	Ar	-0.3	9.74	1.00E+06	1.67E+03	3.37E+03	1.56E+02	2.54E+04	0	1.00E-06

114	//	1	39.5	6.20	0.10	0	4	Ar	-0.3	9.74	4.91E+05	1.76E+03	5.34E+03	7.65E+01	2.55E+04	20	4.07E-05
115	//	1	39.5	7.05	0.62	0	1	Ar	-0.3	9.74	1.00E+06	1.60E+03	2.06E+03	1.56E+02	2.56E+04	30	3.00E-05
116	//	1	42	8.05	0.70	0	1	Ar	-0.3	9.74	8.99E+05	1.57E+03	2.12E+03	1.40E+02	2.58E+04	22	2.45E-05
117	//	1	42	9.05	0.80	0	1	Ar	-0.3	9.74	1.00E+06	1.59E+03	3.66E+03	1.56E+02	2.59E+04	11	1.10E-05
118	//	1	42	10.05	0.90	0	1	Ar	-0.3	9.74	1.00E+06	1.59E+03	3.25E+03	1.56E+02	2.61E+04	0	1.00E-06
119	//	1	107	10.05	1.00	0	1	Xe	-0.3	58.78	1.00E+07	1.49E+04	1.69E+04	9.40E+03	3.55E+04	1338	1.34E-04
Run	**Design**	**DUT**	**Tb (Vacuum)**	**Vin**	**Inv. Input Bias**	**Vout**	**Trig Vout**	**Ion**	**Tilt Angle**	**Effective LET**	**Effective Fluence**	**Average Flux**	**Maximum Flux**	**TID (Run)**	**TID (Cumulative)**	**#SET**	**SET Cross-Section**
			(°C)	(V)	(V)	(V)	(V)		degrees	MeV.cm2/mg	p/cm2	p/sec/cm2	p/sec/cm2	rads(Si)	rads(Si)		cm2/circuit
122	With 0.1uF Cout	2	39.5	5.40	0.50	5	4	Xe	1.6	58.8	1.05E+06	1.63E+03	4.48E+03	9.88E+02	5.56E+04	0	9.52E-07
123	//	2	39.5	5.40	0.54	5	4	Xe	1.6	58.8	3.91E+06	4.80E+04	8.16E+04	3.68E+03	5.93E+04	0	2.56E-07
124	//	2	39.5	5.40	0.54	5	4	Xe	1.6	58.8	2.96E+07	8.79E+04	9.38E+04	2.78E+04	8.72E+04	0	3.38E-08
127	//	2	39.5	5.40	0.54	5	4	Xe	0	58.78	1.01E+07	9.11E+04	9.64E+04	9.50E+03	9.67E+04	0	9.90E-08
128	//	2	39.5	1.05	0.54	5	1	Xe	0	58.78	1.01E+07	9.13E+04	9.88E+04	9.50E+03	1.06E+05	0	9.90E-08
129	//	2	97	10.05	0.10	0	1	Xe	0	58.78	1.21E+07	9.43E+04	1.02E+05	1.14E+04	1.18E+05	0	8.26E-08
130	//	2	97	10.05	1.00	0	1	Xe	60	117.56	1.00E+07	8.03E+04	1.02E+05	1.88E+04	1.36E+05	0	1.00E-07

*Tb is the temperature sensed by the transistor on the board (as shown in Fig. 5)

3ft BNC cable (120pF)	Energy Cocktail 10MeV/nucleon

Table 3: Raw Data for the Heavy-Ion Beam Runs (VOS Board)

Run	Design	DUT	Tb (Vacuum)	Vin	Inverting Input Bias	Vout	Trig Vout	Ion	Tilt Angle	Effective LET	Effective Fluence	Average Flux	Maximum Flux	TID (Run)	TID (Cumulative)	#SET	SET Cross-Section
			(°C)	(V)	(V)	(V)	(V)		degrees	MeV.cm2/mg	p/cm2	p/sec/cm2	p/sec/cm2	rads(Si)	rads(Si)		cm2/circuit
131	With Cout=22nF	3	37	-0.55	-0.050	12	11	Xe	0	58.78	1.00E+07	1.72E+04	1.72E+04	5.69E+04	9.40E+03	46	4.60E-06
132	//	3	37	-0.55	-0.050	12	11	Xe	0	58.78	7.51E+06	3.45E+04	3.45E+04	5.90E+04	7.06E+03	45	5.99E-06
133	//	3	37	-0.55	-0.050	12	11	Xe	0	58.78	1.00E+06	1.07E+03	1.07E+03	2.25E+03	9.40E+02	8	8.00E-06
134	//	3	37	-1.05	-0.100	12	11	Xe	0	58.78	1.00E+06	1.29E+03	1.29E+03	6.97E+03	9.40E+02	2	2.00E-06
135	//	3	37	-1.55	-0.150	12	11	Xe	0	58.78	1.00E+06	2.01E+03	2.01E+03	7.11E+03	9.40E+02	8	8.00E-06
136	//	3	37	-2.05	-0.200	12	11	Xe	0	58.78	5.71E+03	1.77E+03	1.77E+03	1.70E+03	5.37E+00	5	8.76E-04
137	//	3	37	0.55	0.050	0	1	Xe	0	58.78	1.00E+06	4.65E+03	4.65E+03	7.36E+03	9.40E+02	0	1.00E-06
138	//	3	37	0.55	0.050	0	1	Xe	0	58.78	1.00E+06	1.23E+03	1.23E+03	2.16E+03	9.40E+02	0	1.00E-06
139	//	3	37	1.05	0.100	0	1	Xe	0	58.78	1.00E+06	1.95E+03	1.95E+03	5.63E+03	9.40E+02	0	1.00E-06
140	//	3	37	1.55	0.150	0	1	Xe	0	58.78	1.00E+06	2.03E+03	2.03E+03	6.32E+03	9.40E+02	0	1.00E-06

141	//	3	37	1.05	0.100	0	1	Xe	0	58.78	1.00E+06	1.50E+03	1.50E+03	1.92E+03	9.40E+02	0	1.00E-06
142	//	3	37	1.55	0.150	0	1	Xe	0	58.78	1.00E+06	1.77E+03	1.77E+03	1.93E+03	9.40E+02	0	1.00E-06
143	//	3	37	1.55	0.150	0	1	Xe	0	58.78	1.00E+06	6.52E+03	6.52E+03	7.33E+03	9.40E+02	0	1.00E-06
144	//	3	37	2.05	0.200	0	1	Xe	0	58.78	1.00E+06	1.30E+03	1.30E+03	2.26E+03	9.40E+02	0	1.00E-06
145	//	3	37	-2.05	-0.200	12	11	Xe	0	58.78	1.00E+06	1.77E+03	1.77E+03	2.14E+03	9.40E+02	4	4.00E-06
146	//	3	37	-1.55	-0.150	12	11	Xe	0	58.78	1.00E+06	1.85E+03	1.85E+03	2.10E+03	9.40E+02	4	4.00E-06
147	//	3	37	-0.25	-0.020	12	11	Xe	0	58.78	1.00E+06	1.82E+03	1.82E+03	2.11E+03	9.40E+02	7	7.00E-06
148	//	3	37	-0.25	-0.020	12	11	Ag	0	48.15	1.00E+06	1.01E+03	1.01E+03	1.68E+03	7.70E+02	0	1.00E-06
149	//	3	37	-0.55	-0.050	12	11	Ag	0	48.15	1.00E+06	1.06E+03	1.06E+03	1.23E+03	7.70E+02	0	1.00E-06
150	//	3	37	-1.55	-0.150	12	11	Ag	0	48.15	1.00E+06	1.33E+03	1.33E+03	3.00E+03	7.70E+02	0	1.00E-06
Run	**Design**	**DUT**	**Tb (Vacuum)**	**Vin**	**Inv. Input Bias**	**Vout**	**Trig Vout**	**Ion**	**Tilt Angle**	**Effective LET**	**Effective Fluence**	**Average Flux**	**Maximum Flux**	**TID (Run)**	**TID (Cumulative)**	**#SET**	**SET Cross-Section**
			(°C)	(V)	(V)	(V)	(V)		degrees	MeV.cm2/mg	p/cm2	p/sec/cm2	p/sec/cm2	rads(Si)	rads(Si)		cm2/circuit
153	//	3	37	-0.55	-0.050	12	11	Ag	0	48.15	6.18E+05	1.34E+03	1.34E+03	2.65E+03	4.76E+02	20	3.24E-05
154	//	3	37	-1.05	-0.100	12	11	Ag	0	48.15	7.21E+05	1.39E+03	1.39E+03	3.76E+03	5.55E+02	20	2.77E-05
155	//	3	37	-1.55	-0.150	12	11	Ag	0	48.15	8.10E+05	4.01E+03	4.01E+03	4.45E+03	6.24E+02	20	2.47E-05
156	//	3	37	-2.05	-0.200	12	11	Ag	0	48.15	1.00E+06	5.35E+03	5.35E+03	1.13E+04	7.70E+02	28	2.80E-05
157	//	3	37	-0.25	-0.020	12	11	Xe	-2.7	58.85	1.00E+06	3.37E+03	3.37E+03	3.61E+03	9.42E+02	230	2.30E-04
158	//	3	37	-0.55	-0.050	12	11	Xe	-2.7	58.85	2.01E+05	3.75E+03	3.75E+03	3.93E+03	1.89E+02	23	1.14E-04
159	//	3	37	-1.05	-0.100	12	11	Xe	-2.7	58.85	4.02E+05	3.81E+03	3.81E+03	4.05E+03	3.79E+02	20	4.98E-05
160	//	3	37	-1.55	-0.150	12	11	Xe	-2.7	58.85	2.83E+05	3.79E+03	3.79E+03	4.00E+03	2.66E+02	20	7.07E-05
161	//	3	37	-1.55	-0.150	12	11	Xe	-2.7	58.85	3.64E+05	3.75E+03	3.75E+03	3.97E+03	3.43E+02	26	7.14E-05
162	//	3	37	0.25	0.020	0	2	Xe	-2.7	58.85	7.77E+04	3.57E+03	3.57E+03	3.69E+03	7.32E+01	93	1.20E-03

163	//	3	37	0.25	0.020	0	2	Xe	-2.7	58.85	1.87E+05	3.51E+03	3.51E+03	3.69E+03	1.76E+02	62	3.32E-04
164	//	3	37	0.55	0.050	0	2	Xe	-2.7	58.85	1.81E+05	3.53E+03	3.53E+03	3.69E+03	1.70E+02	28	1.55E-04
165	//	3	37	1.05	0.100	0	2	Xe	-2.7	58.85	3.98E+05	3.50E+03	3.50E+03	3.68E+03	3.75E+02	52	1.31E-04
166	//	3	37	1.55	0.150	0	2	Xe	-2.7	58.85	2.17E+05	3.54E+03	3.54E+03	3.69E+03	2.04E+02	23	1.06E-04
167	//	3	37	2.05	0.200	0	2	Xe	-2.7	58.85	3.37E+05	3.48E+03	3.48E+03	3.65E+03	3.17E+02	22	6.53E-05
168	//	3	42	0.25	0.020	0	2	Ag	-2.7	48.15	3.65E+05	4.47E+03	4.47E+03	7.35E+03	2.81E+02	28	7.67E-05
169	//	3	42	0.55	0.050	0	2	Ag	-2.7	48.15	4.84E+05	4.44E+03	4.44E+03	7.99E+03	3.73E+02	20	4.13E-05
170	//	3	42	1.05	0.100	0	2	Ag	-2.7	48.15	5.89E+05	4.25E+03	4.25E+03	4.48E+03	4.54E+02	22	3.74E-05
171	//	3	42	1.55	0.150	0	2	Ag	-2.7	48.15	5.51E+05	4.22E+03	4.22E+03	4.43E+03	4.24E+02	20	3.63E-05
172	//	3	42	2.05	0.200	0	2	Ag	-2.7	48.15	7.62E+05	4.23E+03	4.23E+03	4.59E+03	5.87E+02	22	2.89E-05

*Tb is the temperature sensed by the transistor on the board (as shown in Fig. 6)

References:

[1] RH1011M DataSheet: http://www.linear.com/product/RH1011

[2] LT1011 Datasheet: http://www.linear.com/product/LT1011

[3] S. Rezgui et al., *IEEE TNS* Papers, NO. 6, Dec. 2007- 2011.

[4] R. Koga et al., "Single Event Upset (SEU) Sensitivity Dependence of Linear Integrated Circuits (ICs) on Bias Conditions", *IEEE TNS*, Vol. 44, NO. 6, Dec. 1997.

[5] LTSpice: http://www.linear.com/designtools/software/#LTspice

[6] RH1011M Spec.: http://cds.linear.com/docs/Spec%20Notice/RH1011_05-08-5012_SPEC_REV.M.pdf