						I	REVIS	SION F	RECOF	RD								
REV							DESC	CRIPT	ION								DA	TE
0	INITIA	L RELEAS	SE														06/0	1/06
A	• PA	GE 3, PAI	RAGR.	APH 3	3.7.1 C	HANC	BED V	ERBI.	AGE								05/0	06/08
		GE 4, PAI	RAGR	APH 5	5.8 CH.	ANGE	ED AL	LOY 4	42 TO	KOVA	AR RE	QUIR	ED O	N TOS	5			
В	• PACKA	к <u>бе.</u> GE 11, АІ	ODED	NOTE	ES 2 A1	ND CE	DECIV	I NO	TE ON	WAF	ED TI	SCTIN	G AN	D.			04/0	06/09
В		RMANCE		NOTI	33 2 A	וט טוי	LCIA	L NO	IL ON	WAI	LK II	20111	O AN	D			04/0	10/09
		GE 13, CF									-					S		
		O TEMPEI			-				CELER	ATIO	N & R	EMO	VED F	PIND	ΓEST.			
С		VED THE amended s							n more	accur	ately d	lescrib	e our o	curren	t		03/3	30/12
C		ires and red			рестаг	Tanan	ing or	Dicc t	o more	accur	atery c	030110	c our c	curren	·		03/2	70/12
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		of the dic										-			test			
		$T_A = 25^{\circ}C$													~ .		0.7.10	20/10
Е	_	, Changed hanged fro			-				-			_	-	-			07/0)2/13
F		, amended															06/2	24/14
1	_	to 75 μA a							-						•		00/2	,,,,,,,
G	Update	d Die Sales	s table	on pg	13.												03/2	26/15
CAU'	TIO]	N: EI	LE(CTF	ROS	TA	TI	\mathbf{C} \mathbf{D}	IS(CHA	AR	GE	SE	NS	ITI	VE	PA	RT
REVISIO		GE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13			
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												<u>ANA</u>	LOC	F DE	VICE	ES IN	<mark>IC</mark> .	
			RIG SGN							TIT	I E.							
		-	NGR							- 111		IICR	OCI	RCII	IT R	H10	78M	
		-	ИFG														NGL	E
		(CM								SU						AMP	
		(QA							SIZ	Œ	CAG COD		DRA	WING	NUM	1BER	REV
		P	ROG									6415		0	5-08	-5209)	H
APPLIC	ATION	I FU	JNCT	1	SI	GNO:	FFS	D	ATE	CO	NTRA	.CT:						

FOR OFFICIAL USE ONLY

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 <u>Government Specifications and Standards</u>: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

2.2 <u>Order of Precedence:</u> In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

- 3.1 <u>General Description</u>: This specification details the requirements for the RH1078M, MICROPOWER, DUAL, SINGLE SUPPLY PRECISION OP AMP DICE and Element Evaluation Test Samples, processed to space level manufacturing flow as specified herein.
- 3.2 Part Number: RH1078M, Dice
- 3.3 Special Handling of Dice: Rad Hard dice require special handling as compared to standard IC dice. Rad Hard dice are susceptible to surface damage due to the absence of silicon nitride passivation that is present on most standard dice. Silicon nitride protects the dice surface from scratches by its hard and dense properties. The passivation on Analog Devices Rad Hard dice is silicon dioxide which is much "softer" than silicon nitride. During the visual and preparation for shipment, ESD safe Tweezers are used and only the edge of the die are touched.

LTC recommends that dice handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die in or out of the chip shipment tray (waffle pack), use an ESD-Safe-Plastic-tipped Bent Metal Vacuum Probe, preferably .020" OD x .010" ID (for use with tiny parts). The wand should be compatible with continuous air vacuums. The tip material should be static dissipative Delrin (or equivalent) plastic.

During die attach, care must be exercised to ensure no tweezers, or other equipment, touch the top of the dice.

3.4 The Absolute Maximum Ratings:

Supply Voltage												. <u>+</u> 22V
Differential Input Voltage												. <u>+</u> 30V
Input Voltage	 	 		E	Equ	al t	o P	osi	tiv	e Si	upp	ly Voltage
	 	 	.0.5	5V	Be	low	N	ega	tiv	e S	upp	ly Voltage
Output Short-Circuit Duration												Indefinite
Operating Temperature Range										-5	5°(C to 125°C

- 3.5 <u>Design, Construction, and Physical Dimensions</u>: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.
- 3.6 <u>Outline Dimensions and Pad Functions</u>: Dice outline dimensions, pad functions, and locations shall be specified in **Figure 1**.
- 3.7 Radiation Hardness Assurance (RHA):
 - 3.7.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.
 - 3.7.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.
 - 3.7.3 Total dose bias circuit is specified in **Figure 2**.
- 3.8 <u>Wafer (or Dice) Probe</u>: Dice shall be 100% probed at Ta = +25°C to the limits shown in **Table I** herein. All reject dice shall be removed from the lot. This testing is normally performed prior to dicing the wafer into chips. Final specifications after assembly are sample tested during the element evaluation.
- 3.9 <u>Wafer Lot Acceptance</u>: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Top side glassivation thickness shall be a **minimum of 4KÅ**.
- 3.10 <u>Wafer Lot Acceptance Report</u>: SEM is performed per MIL-STD-883, Method 2018. Copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.
- 3.11 <u>Traceability</u>: Wafer Diffusion Lot and Wafer traceability shall be maintained through Quality Conformance Inspection.
- 4.0 QUALITY CONFORMANCE INSPECTION: Quality Conformance Inspection shall consist of the tests and inspections specified herein.
- 5.0 SAMPLE ELEMENT EVALUATION: A sample from **each wafer supplying dice** shall be assembled and subjected to element evaluation per **Table III** herein.
 - 5.1 <u>100 Percent Visual Inspection</u>: All dice supplied to this specification shall be inspected in accordance with MIL-STD-883, Method 2010, Condition A. All reject dice shall be removed from the lot.
 - 5.2 <u>Electrical Performance Characteristics for Element Evaluation</u>: The electrical performance characteristics shall be as specified in **Table I** and **Table II** herein.
 - 5.3 <u>Sample Testing</u>: Each wafer supplying dice for delivery to this specification shall be subjected to element evaluation sample testing. No dice shall be delivered until all the lot sample testing has been performed and the results found to be acceptable unless the customer supplies a written approval for shipment prior to completion of wafer qualification as specified in this specification.

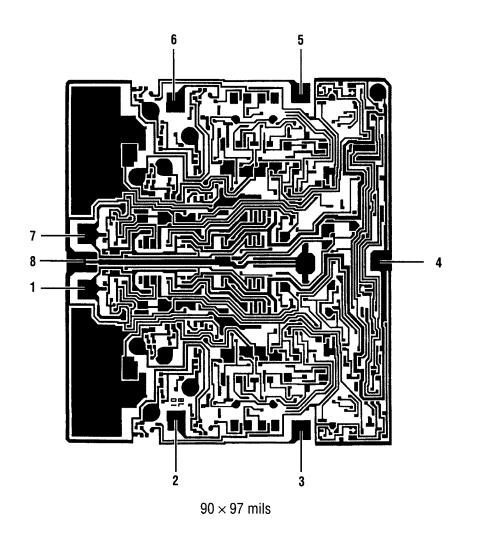
- 5.4 Part Marking of Element Evaluation Sample Includes:
 - 5.4.1 LTC Logo
 - 5.4.2 LTC Part Number
 - 5.4.3 Date Code
 - 5.4.4 Serial Number
 - 5.4.5 ESD Identifier per MIL-PRF-38535, Appendix A
 - 5.4.6 Diffusion Lot Number
 - 5.4.7 Wafer Number
- 5.5 Burn-In Requirement: Burn-In circuit for TO5 package is specified in **Figure 3**.
- 5.6 <u>Mechanical/Packaging Requirements</u>: Case Outline and Dimensions are in accordance with **Figure 4.**
- 5.7 <u>Terminal Connections</u>: The terminal connections shall be as specified in **Figure 5**.
- 5.8 <u>Lead Material and Finish:</u> The lead material and finish shall be Kovar with hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.
- 6.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)
 - 6.1 <u>Quality Assurance Provisions</u>: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. <u>Analog Devices</u> is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.
 - 6.2 <u>Sampling and Inspection</u>: Sampling and Inspection shall be in accordance with **Table III** herein.
 - 6.3 <u>Screening</u>: Screening requirements shall be in accordance with **Table III** herein.
 - 6.4 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:
 - 6.4.1 Lot Serial Number Sheets identifying all Canned Sample devices accepted through final inspection by serial number.
 - 6.4.2 100% attributes (completed element evaluation traveler).
 - 6.4.3 Element Evaluation variables data, including Burn-In and Op Life
 - 6.4.4 SEM photographs (3.10 herein)
 - 6.4.5 Wafer Lot Acceptance Report (3.9 herein)
 - 6.4.6 A copy of outside test laboratory radiation report if ordered

6.4.7 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 6.4.1 and 6.4.7 will be delivered as a minimum, with each shipment.

7.0 <u>Packaging Requirements</u>: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All dice shall be packaged in multicavity containers composed of conductive, anti-static, or static dissipative material with an external conductive field shielding barrier.

DICE OUTLINE DIMENSIONS AND PAD FUNCTIONS

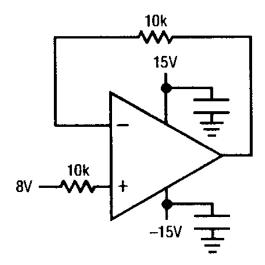


PAD FUNCTION

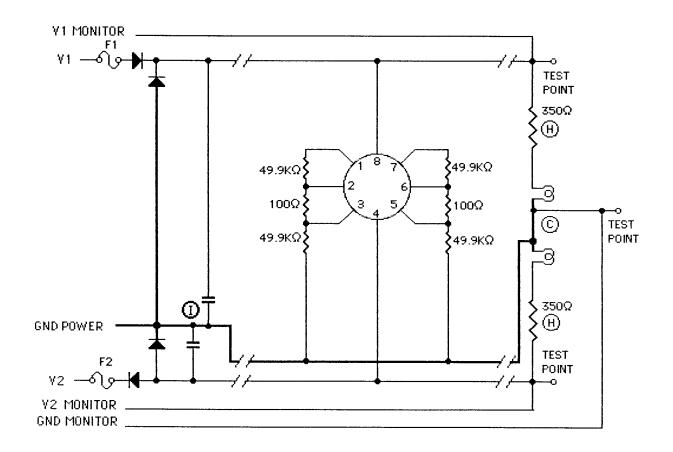
- 1. OUTA
- 2. **-INA**
 - . +INA
- 4. **-V**
- 5. **+INB**
- 6. **-INB**
- 7. **OUTB**
- 8. **+V**

12mils thick, backside (substrate) is an alloyed gold layer. Connect backside to V⁻.

TOTAL DOSE BIAS CIRCUIT



BURN-IN CIRCUIT



NOTES:

- Unless otherwise specified, component tolerances shall be per military specification.
- 2. Tj = +134°C maximum.
- 3. Ta = +125 °C.
- 4. Burn-in Voltages: V1 = +20V to +22VV2 = -20V to -22V

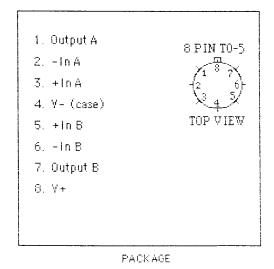
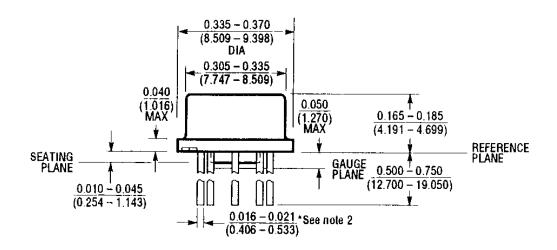
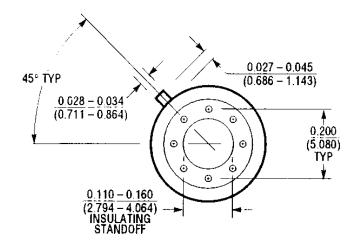


FIGURE 3

TO5, 8 LEADS, CASE OUTLINE



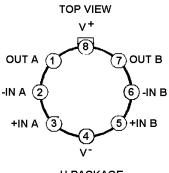


NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016-0.024}{(0.406-0.610)}$

 θ ja = +150°C/W θ jc = +40°C/W

TERMINAL CONNECTIONS



H PACKAGE 8-LEAD TO-5 METAL CAN

TABLE I DICE ELECTRICAL CHARACTERISTICS – Element Evaluation (Note 1)

DICE ELECTRICAL TEST LIMITS $T_A = 25^{\circ}C$, $V_S = 5V$, $V_{CM} = 0.1V$, $V_{OUT} = 1.4V$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
AvoL	Large-Signal Voltage Gain	V _O = 0.03V to 4V, No Load V _O = 0.03V to 3.5V, R _L = 50k V _O = 0.05V to 4V, No Load V _O = 0.05V to 3.5V, R _L = 50k	150 120		V/mV V/mV V/mV V/mV
V _{OUT}	Output Voltage Swing	Output Low, No Load Output Low, 2k to GND Output Low, 1 _{SINK} = 100µA Output High, No Load Output High, 2k to GND	4.2 3.5	6 2 130	mV mV mV V
SR	Siew Rate	A _V = 1, V _S = ±2.5V	0.04		V/µs
lg	Supply Current	Per Amplifier		75	μA
	Minimum Supply Voltage	Note 2		2.3	V

$T_A = 25$ °C, $V_S = \pm 15$ V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
Vos	Input Offset Voltage			350	Vų
los	Input Offset Current			0.8	nA
l _B	Input Bias Current			15	пA
	Input Voltage Range		13.5 -15.0		V V
CMRR	Common Mode Rejection Ratio	V _{CM} = 13.5V, -15V V _{CM} = 13V, -14.9V	97		dB dB
PSRR	Power Supply Rejection Ratio	V _S = 5V, 0V to ±18V	100		₫B
AvoL	Large-Signal Voltage Gain	$V_0 = \pm 10 \text{V}, R_L = 50 \text{k}$ $V_0 = \pm 10 \text{V}, R_L = 2 \text{k}$ $V_0 = \pm 10 \text{V}, R_L = 5 \text{k}$	1000 300		V/mV V/mV V/mV
V _{OUT}	Output Voltage Swing	RL = 50k RL = 2k RL = 5k	±13 ±11		V V
SR	Slew Rate		0.06		V/µs
Is	Supply Current	Per Amplifier		100	Αų

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Power supply rejection ratio is measured at the minimum supply voltage.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

TABLE II ELECTRICAL CHARACTERISTICS – Post-Irradiation

 $V_{S}=5V,\ 0V,\ V_{CM}=0.1V,\ V_{0}=1.4V,\ T_{A}=25^{\circ}C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		AD(Si)	1	AD(Si)		AD(Si)		AD(Si)	100KRAD(Si)	1
		COMDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN MAX	UNITS
V _{OS}	Input Offset Voltage		<u> </u>	120		175		250		500]	μV
los	Input Offset Current			2		8		13		18		nA
l _B	Input Bias Current			20		40		80		100		nA
	Input Voltage Range		3.5		3.5		3.5		3.5			V
CMRR	Common-Mode Rejection Ratio	V _{CM} = 0V to 3.5V	91		89		87		85			dB
PSRR	Power Supply Rejection Ratio	V _S = 2.3V to 12V	100		100		98		88			dB
A _{VOL}	Large-Signal Voltage Gain	V ₀ = 0.03V to 4V, No Load V ₀ = 0.03V to 3.5V, R _L = 50k	150 120		150 50		100 20		50 10			V/mV V/mV
V _{OUT}	Output Voltage Swing	Output Low, No Load Output Low, 2k to GND Output Low, I _{SINK} = 100µA Output High, No Load Output High, 2k to GND	4.2 3.5	6 2 130	4.2 3.5	9 2 140	4.2 3.5	13 2 150	4.2 3.5	20 2 160		mV mV mV V
S _R	Slew Rate	$A_V = 1, V_S = \pm 2.5V$	0.04		0.03		0.02		0.01			V/µs
Is	Supply Current	per Amplifier		75		75		75		75		μА

$V_S = \pm 15V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	10KRA Min	D(Si) Max	25KR/ MIN	AD(Si) Max	50KR/	ND(Si) Max	75KR/ MIN	D(Si)	100KR	. ,	UNITS
V _{OS}	Input Offset Voltage			350		500	171114	650	171314	800	19114	1000	μV
los	Input Offset Current			2		8		13		18		23	nA
I _B	Input Bias Current			20		40		80		100		120	nA
	Input Voltage Range		13.5 -15.0		13.5 -15.0		13.5 -15.0		13.5 -15.0		13.5 -15.0		V
CMRR	Common-Mode Rejection Ratio	V _{CM} = 13.5V, -15V	94		92		90		88		86		dB
PSRR	Power Supply Rejection Ratio	$V_S = 5V$, 0V to $\pm 18V$	100	•	100		98		88		78	7	dB
A _{VOL}	Large-Signal Voltage Gain	V ₀ = 10V, R _L = 50k V ₀ = 10V, R _L = 2k	1000 300		700 200	. 1910	400 120		150 45		50 15		V/mV V/mV
V _{OUT}	Output Voltage Swing	R _L = 50k R _L = 2k	±13 ±11		±13	.=14	±13 ±11		±13 ±11		±13 ±10	-10	V
SR	Slew Rate		0.05		0.04		0.03		0.02		0.01		V/µs
ls	Supply Current	per Amplifier		100		100		100		100		100	μΑ

TABLE III RH ELEMENT EVALUATION TABLE QUALIFICATION OF DICE SALES



RH CANNED SAMPLE TABLE FOR QUALIFYING DICE SALES

]	l]	KH CANNED SAMPLE TABLE FOR QUALIFYING DICE SALES	ING DICE SALES		
SUBGROUP	K/S	CLASS	S H/B	OPERATION	METHOD	MIL-STD-883 CONDITION	QUANTITY (ACCEPT NUMBER)
1	×			SEM	2018	N/A	REF. METHOD 2018 FOR S/S
2	×	×	×	ELEMENT ELECTRICAL (WAFER SORT @ 25°C)			100%
3	×	X	×	ELEMENT VISUAL (2nd OP)	2010	А	100%
4	×	×	×	INTERNAL VISUAL (3rd OP)	2010	Α	ASSEMBLED PARTS ONLY
	×	×		DIE SHEAR MONITOR	2019		
	X	Х		BOND PULL MONITOR	2011		
5	X	×		STABILIZATION BAKE	1008	С	ASSEMBLED PARTS ONLY
	×	×		TEMPERATURE CYCLE	1010	С	
	×	×		CONSTANT ACCELERATION	2001	Е	
	×	X		FINE LEAK	1014	А	
	×	Х		GROSS LEAK	1014	С	
6	×	×		FIRST ROOM ELECTRICAL - READ & RECORD			45(0)
				(REPLACE ANY ASSEMBLY-RELATED REJECTS)			
	×	×		PRE BURN-IN ELECT. READ & RECORD @ +125°C or +150°C, -55°C			
	×	×		BURN-IN: +125°C/240 hrs. or +150°C/120 hrs.	1015	+ 125°c MINIMUM 240 HOURS	
	×	×		POST BURN-IN ELECT. READ & RECORD @ 25°C			
	×	×		POST BURN-IN ELECT. READ & RECORD @ +125°C or +150°C, -55°C			
		X		TOTAL IRRADIATION DOSE	1019	A	
	×	×		PRE OP-LIFE ELECTRICAL @ 25°C READ & RECORD			
	×	×		OPERATING LIFE: +125°C/1000 hrs. or +150°C/500 hrs.	1005	+ 125% MINIMUM	
	×	×		POST OP-LIFE ELECT. (R & R @ 25°C, +125°C OR +150°C, -55°C			
7	×	X	×	WIRE BOND EVALUATION	2011		15(0) OR 25(1) - # of wires
NOTE:	M Ci	S no	t qua	LTC is not qualified to process to MIL-PRF-38534. This is an LTC imposed element evaluation that follows. MIL-STD-883 test methods and conditions. Please note the quantity and accept number from Sample Size Series of	ment evaluation	that follows	ps of
	5%,	ассе	pt o	5%, accept on 0, and note that the actual sample and accept number does not begin until Subgroup 6 OP-LIFE.	not begin until S	ubgroup 6 OP-LIFI	1.,
NOTE:	Test	s wit	hin	Tests within Subgroup 5 may be performed in any sequence.			
NOTE:	LTC's	s rad	iatio	LTC's radiation tolerance (RH) die has a topside glassivation thickness of 4KA minimum.	minimum.		
NOTE:	Sam	ple s	izes	Sample sizes on the travelers may be larger than that indicated in the above table; however, the larger sample size is to accommodate extra units for replacement devices in the event of equipment or operator error and for assembly	table; however,	the larger sample error and for asse	nbly
	relat kept	ed re	eject egat	related rejects in Subgroup 6, and for Wire Bond Evaluation, Surgroup 7. The larger sample size kept segregated and, if used for qualification, has all the required processing imposed.	larger sample s imposed.	ize is at all times	