Ultralow Noise Precision High Speed Op Amps

DESCRIPTION

The RH1028(gain of –1 stable)/RH1128(gain of +1 stable) achieve a new standard of excellence in noise performance with 0.9nV/√Hz 1kHz noise, 1.0nV/√Hz 10Hz noise. This ultralow noise is combined with excellent high speed specifications (gain-bandwidth product is 75MHz for RH1028, 20MHz for RH1128), distortion-free output, and true precision parameters (0.25µV/°C drift, 20µV offset voltage, 25 million voltage gain). Although the RH1028/RH1128 input stage operates at nearly 1mA of collector current to achieve low voltage noise, input bias current is only 50nA.

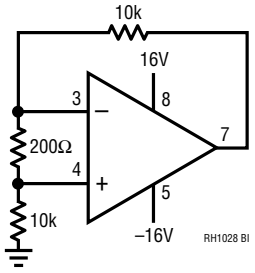
The RH1028/RH1128's voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transducer or audio amplifier applications, the RH1028/RH1128's contribution to total system noise will be negligible.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (–55°C to 125°C).....±16V
Differential Input Current (Note 9) .....±25mA
Input Voltage.....Equal to Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range..... –55°C to 125°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

BURN-IN CIRCUIT



PACKAGE INFORMATION

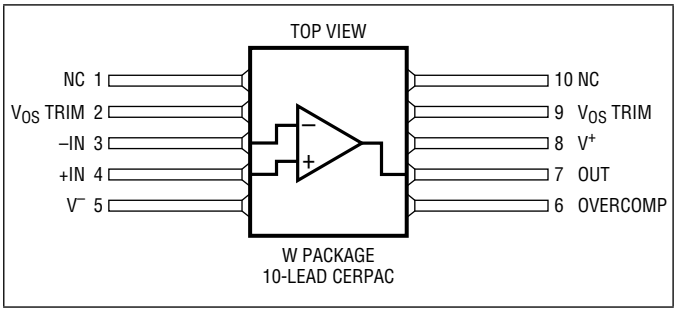


TABLE 1: ELECTRICAL CHARACTERISTICS

(Preirradiation) V_S = ±15V, V_{CM} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDTIONS	NOTES	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	SUB-GROUP	–55°C ≤ T_A ≤ 125°C MIN	–55°C ≤ T_A ≤ 125°C TYP	–55°C ≤ T_A ≤ 125°C MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage		2		20	80	1		45	180	2, 3	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long-Term Input Offset Voltage Stability		3		0.3							µV/M_O
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		8						0.25	1.0		µV/°C
I_{OS}	Input Offset Current	V_{CM} = 0V			18	150	1		30	200	2, 3	nA
I_B	Input Bias Current	V_{CM} = 0V			±50	±400	1		±100	±600	2, 3	nA
e_n	Input Noise Voltage Density	f_O = 10Hz f_O = 1000Hz, 100% Tested	5		1.0 0.9	2.5 1.6						nV/√Hz nV/√Hz

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I_n	Input Noise Current Density	f_O = 10Hz f_O = 1000Hz, 100% Tested	4, 6		4.7 1.0	24 3.6						pA/√Hz pA/√Hz
	Input Resistance Common Mode Differential Mode				 300 20							 MΩ kΩ
	Input Capacitance				5							pF
	Input Voltage Range			±11.0	±12.2			±10.3	±11.7			V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11V V_{CM} = ±10.3V		110	126		1	 100	 120		2, 3	dB
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±18V V_S = ±4.5V to ±16V		110	132		1	 104	 130		2, 3	dB
A_{VOL}	Large-Scale Voltage Gain	R_L ≥ 2k, V_O = ±10V R_L ≥ 1k, V_O = ±10V R_L ≥ 600Ω, V_O = ±10V		5.0 3.5 2.0	25 20 15		4	2.0 1.5	14 10		5, 6	V/µV V/µV V/µV
V_{OUT}	Maximum Output Voltage Swing	R_L ≥ 2k R_L ≥ 600Ω		±12.0 ±10.5	±13.0 ±12.2		4	±10.3	±11.6		5, 6	V V
SR	Slew Rate	A_{VCL} = –1 (RH1028) A_{VCL} = –1 (RH1128)		11.0 4.5	15 6		4					V/µs V/µs
GWB	Gain Bandwidth Product	f_O = 20kHz (RH1028) f_O = 200kHz (RH1128)	7 7	50 11	75 20							MHz MHz
Z_O	Open-Loop Output Impedance	V_O = 0, I_O = 0			80							Ω
I_S	Supply Current				7.6	10.5	1		9	13	2, 3	mA

TABLE 1A: ELECTRICAL CHARACTERISTICS

(Postirradiation) V_S = ±15V, V_{CM} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDTIONS	NOTES	10KRAD(Si) MIN	10KRAD(Si) MAX	20KRAD(Si) MIN	20KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	200KRAD(Si) MIN	200KRAD(Si) MAX	UNITS
V_{OS}	Input Offset Voltage		2		100		120		140		160		180	µV
I_{OS}	Input Offset Current				200		200		200		300		500	nA
I_B	Input Bias Current				±600		±700		±950		±1100		±1700	nA
SR	Slew Rate	A_{VCL} = –1 (RH1028) A_{VCL} = –1 (RH1128)		7.5 3.0		7.5 3.0		7.5 3.0		7.5 3.0		7.5 3.0		V/µs V/µs
	Input Voltage Range			±11		±11		±11		±11		±11		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11V		106		106		106		106		106		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±18V		104		104		104		104		104		dB
A_{VOL}	Large-Signal Voltage Gain	R_L ≥ 2k, V_O = ±10V		2		2		2		2		2		V/µV
V_{OUT}	Maximum Output Voltage Swing	R_L ≥ 2k R_L ≥ 600Ω		±11.5 ±10		±11.5 ±10		±11.5 ±10		±11.5 ±10		±11.5 ±10		V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power. In addition, at T_A = 25°C, offset voltage is measured with the chip heated to approximately 55°C to account for the chip temperature rise when the device is fully warmed up.

Note 3: Long-term input offset voltage stability refers to the average trend line of Offset Voltage vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5µV.

Note 4: This parameter is tested on a sample basis only.

Note 5: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 6: Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise. Maximum 10Hz current noise can be inferred from 100% testing at 1kHz.

Note 7: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

Note 8: This parameter is not 100% tested.

Note 9: The inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.8V, the input current should be limited to 25mA.

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4
Group A Test Requirements (Method 5005)	1,2,3,4
Group B** and D for Class S, and Group C and D for Class B End Point Electrical Parameters (Method 5005)	1,2,3,4

*PDA Applies to subgroup 1. See PDA Test Notes.
**Post B5 and B6 25°C Limits are as follows:

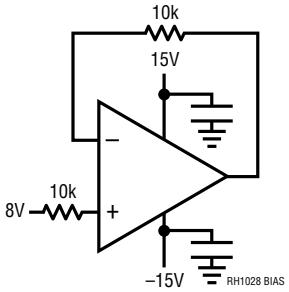
	SUBGROUP 1	SUBGROUP 2, 3	UNITS
V_{OS}	±240	±340	µV
I_{OS}	±350	±400	nA
I_B	±760	±960	nA

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures (including Delta parameters) of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

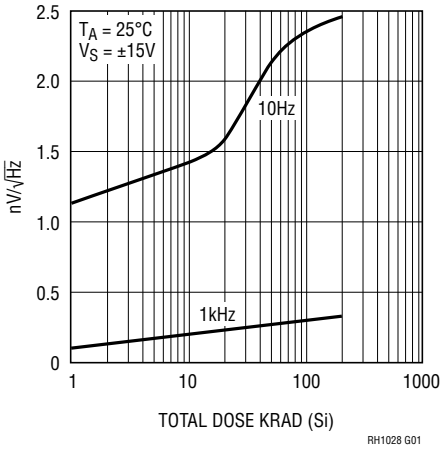
Linear Technology Corporation reserves the right to test to tighter limits than those given.

TOTAL DOSE BIAS CIRCUIT

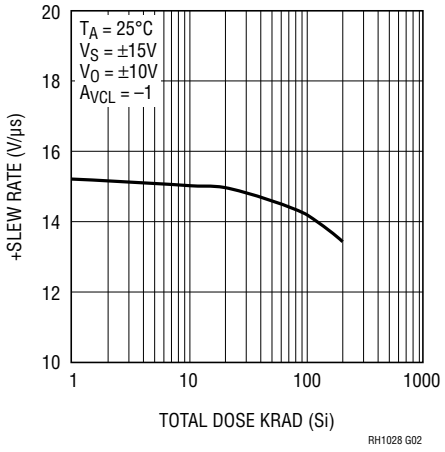


TYPICAL PERFORMANCE CHARACTERISTICS

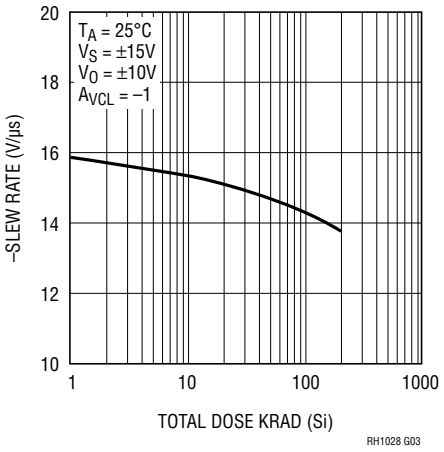
Noise Voltage Density



RH1028 Positive Slew Rate

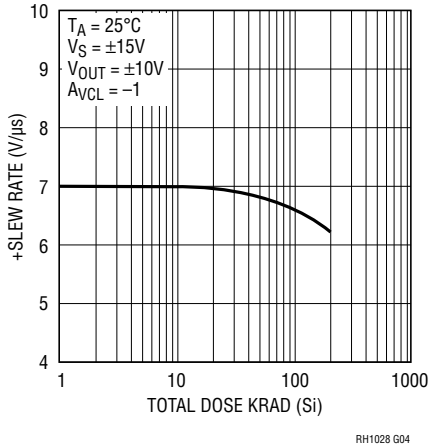


RH1028 Negative Slew Rate

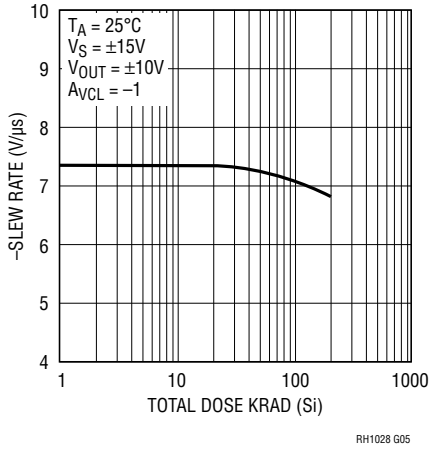


TYPICAL PERFORMANCE CHARACTERISTICS

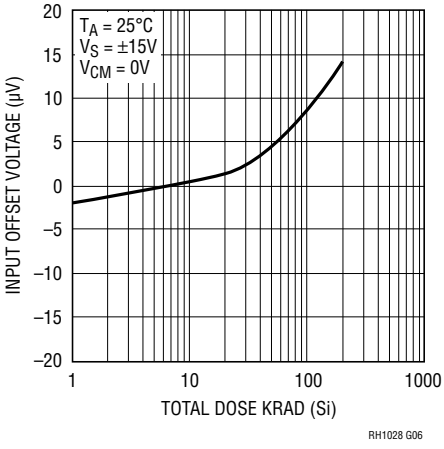
RH1128 Positive Slew Rate



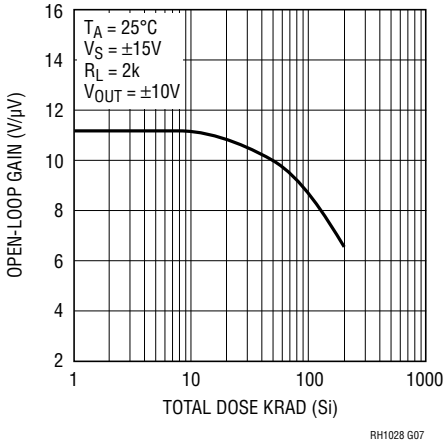
RH1128 Negative Slew Rate



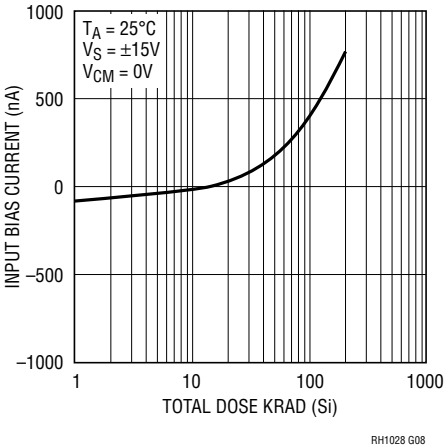
Input Offset Voltage



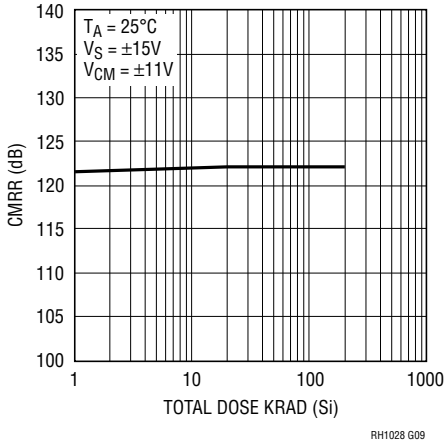
Open-Loop Gain



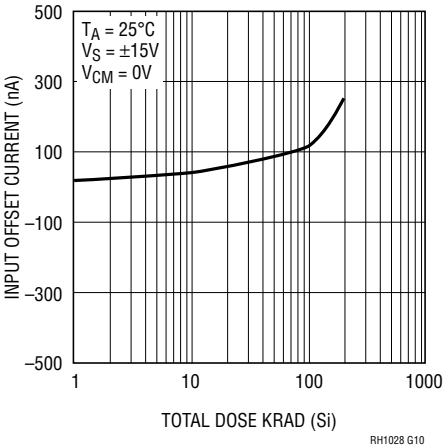
Input Bias Current



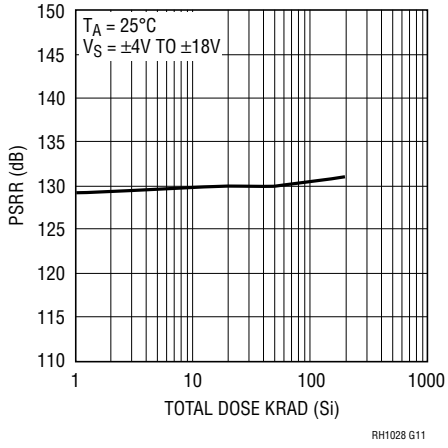
Common Mode Rejection Ratio



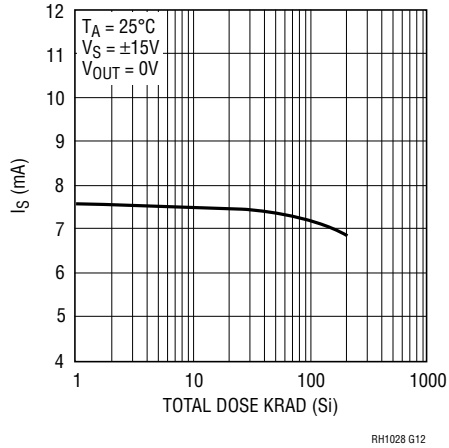
Input Offset Current



Power Supply Rejection Ratio



Supply Current



REVISION HISTORY (Revision history begins at Rev E)

REV	DATE	DESCRIPTION	PAGE NUMBER
E	04/15	Update postirradiation 20/500/100/200k Rad Input Bias Current Specification	2

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