

REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	09/22/08
A	<ul style="list-style-type: none"> PAGE 8, CHANGED OUT ORIGINAL BURN-IN CIRCUIT WITH THE ACTUAL BURN-IN CIRCUIT FROM 04-06-0689. PAGE 13, CHANGED RH CANNED SAMPLE TABLE III FOR QUALIFYING DICE SALES ADDED TEMPERATURE CYCLE, CONSTANT ACCELERATION & REMOVED PIND TEST. 	03/03/09
B	Page 2, amended section 3.3 <u>Special Handling of Dice</u> to more accurately describe our current procedures and requirements.	04/03/12
C	Page 13, Changed RH Canned Sample Table for Qualifying Dice Sales: Subgroup 6 Sample Size Series changed from 45 (3) to 65 (3). First note had the Sample Size Series from "15%" to "10%".	07/02/13
D	Updated Die Sales table on pg 13.	06/01/15
E	Update To remove SI and to change Linear to Analog.	2/19/21

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13			
INDEX	REVISION	E	E	E	E	E	E	E	E	E	E	E	E	E			
REVISION	PAGE NO.																
INDEX	REVISION																
										ANALOG DEVICES INC.							
		ORIG								TITLE: MICROCIRCUIT, LINEAR, RH1573K LOW DROPOUT PNP REGULATOR DRIVER DICE							
		DSGN															
		ENGR															
		MFG															
		CM															
		QA								SIZE	CAGE CODE	DRAWING NUMBER		REV			
		PROG									64155	05-08-5223		E			
APPLICATION	FUNCT	SIGNOFFS		DATE		CONTRACT:											

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1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH1573K, DICE and Element Evaluation Test Samples, processed to space level manufacturing flow as specified herein.

3.2 Part Number: RH1573K Dice

3.3 Special Handling of Dice: Rad Hard dice require special handling as compared to standard IC dice. Rad Hard dice are susceptible to surface damage due to the absence of silicon nitride passivation that is present on most standard dice. Silicon nitride protects the dice surface from scratches by its hard and dense properties. The passivation on Analog Devices Rad Hard dice is silicon dioxide which is much “softer” than silicon nitride. . During the visual and preparation for shipment, ESD safe Tweezers are used and only the edge of the die are touched.

ADI recommends that dice handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die in or out of the chip shipment tray (waffle pack), use an ESD-Safe-Plastic-tipped Bent Metal Vacuum Probe, preferably .020” OD x .010” ID (for use with tiny parts). The wand should be compatible with continuous air vacuums. The tip material should be static dissipative Delrin (or equivalent) plastic.

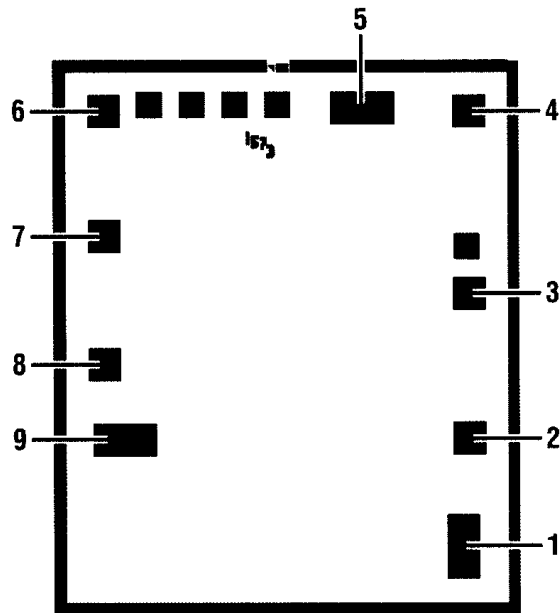
During die attach, care must be exercised to ensure no tweezers, or other equipment, touch the top of the dice.

3.4 The Absolute Maximum Ratings:

Input Pin Voltage (V _{IN} TO GND)	10V
Drive Pin Voltage (V _{DRIVE} TO GND)	10V
Output Pin Voltage (V _{OUT} TO GND)	10V
Shutdown Pin Voltage (V _{SHDN} TO GND)	10V
Operating Junction Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C

- 3.5 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.
- 3.6 Outline Dimensions and Pad Functions: Dice outline dimensions, pad functions, and locations shall be specified in Figure 1.
- 3.7 Radiation Hardness Assurance (RHA):
- 3.7.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.
- 3.7.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.
- 3.7.3 Total dose bias circuit is specified in Figure 2.
- 3.8 Wafer (or Dice) Probe: Dice shall be 100% probed at $T_a = +25^{\circ}\text{C}$ to the limits shown in Table I herein. All reject dice shall be removed from the lot. This testing is normally performed prior to dicing the wafer into chips. Final specifications after assembly are sample tested during the element evaluation.
- 3.9 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Top side glassivation thickness shall be a minimum of $4\text{K}\text{\AA}$.
- 3.10 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018. Copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.
- 3.11 Traceability: Wafer Diffusion Lot and Wafer traceability shall be maintained through Quality Conformance Inspection.
- 4.0 **QUALITY CONFORMANCE INSPECTION**: Quality Conformance Inspection shall consist of the tests and inspections specified herein.
- 5.0 **SAMPLE ELEMENT EVALUATION**: A sample from each wafer supplying dice shall be assembled and subjected to element evaluation per Table III herein.
- 5.1 100 Percent Visual Inspection: All dice supplied to this specification shall be inspected in accordance with MIL-STD-883, Method 2010, Condition A. All reject dice shall be removed from the lot.
- 5.2 Electrical Performance Characteristics for Element Evaluation: The electrical performance characteristics shall be as specified in Table I, Table II and Table III herein.
- 5.3 Sample Testing: Each wafer supplying dice for delivery to this specification shall be subjected to element evaluation sample testing. No dice shall be delivered until all the lot sample testing has been performed and the results found to be acceptable unless the customer supplies a written approval for shipment prior to completion of wafer qualification as specified in this specification.
- 5.4 Part Marking of Element Evaluation Sample Includes:
- 5.4.1 LTC Logo
- 5.4.2 LTC Part Number

- 5.4.3 Date Code
 - 5.4.4 Serial Number
 - 5.4.5 ESD Identifier per MIL-PRF-38535, Appendix A
 - 5.4.6 Diffusion Lot Number
 - 5.4.7 Wafer Number
 - 5.5 Burn-In Requirement: Burn-In circuit for CERDIP / 8 lead package is specified in Figure 3.
 - 5.6 Mechanical/Packaging Requirements: Case Outline and Dimensions are in accordance with Figure 4.
 - 5.7 Terminal Connections: The terminal connections shall be as specified in Figure 5.
 - 5.8 Lead Material and Finish: The lead material and finish shall be alloy 42 with hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.
- 6.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)
- 6.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Analog Devices is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.
 - 6.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with Table III herein.
 - 6.3 Screening: Screening requirements shall be in accordance with Table III herein.
 - 6.4 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:
 - 6.4.1 Lot Serial Number Sheets identifying all Canned Sample devices accepted through final inspection by serial number.
 - 6.4.2 100% attributes (completed element evaluation traveler).
 - 6.4.3 Element Evaluation variables data, including Burn-In and Op Life
 - 6.4.4 SEM photographs (3.10 herein)
 - 6.4.5 Wafer Lot Acceptance Report (3.9 herein)
 - 6.4.6 A copy of outside test laboratory radiation report if ordered
 - 6.4.7 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.
- Note: Items 6. 4.1 and 6. 4.7 will be delivered as a minimum, with each shipment.
- 7.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All dice shall be packaged in multicavity containers composed of conductive, anti-static, or static dissipative material with an external conductive field shielding barrier.



PAD FUNCTION

- 1. DRIVE
- 2. V_{IN}
- 3. V_{OUT}
- 4. COMP
- 5. GND1**
- 6. FB
- 7. LATCH
- 8. SHDN
- 9. GND2**

**GND1 and GND2 are connected together to form GND

DICE OUTLINE AND PAD

DIMENSIONS FUNCTIONS

61mils × 72mils,
12mils thick.

†Backside metal: Alloyed gold layer
(K designator)

Backside potential: lowest (GND) voltage

ANALOG DEVICE:

FIGURE 1

TOTAL DOSE BIAS CIRCUIT

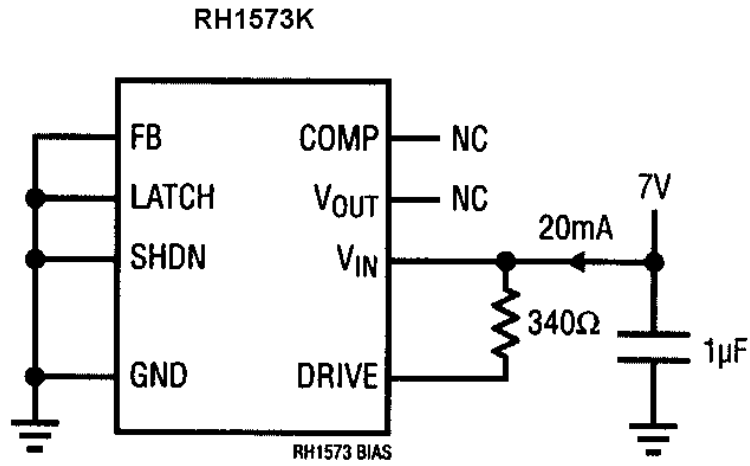
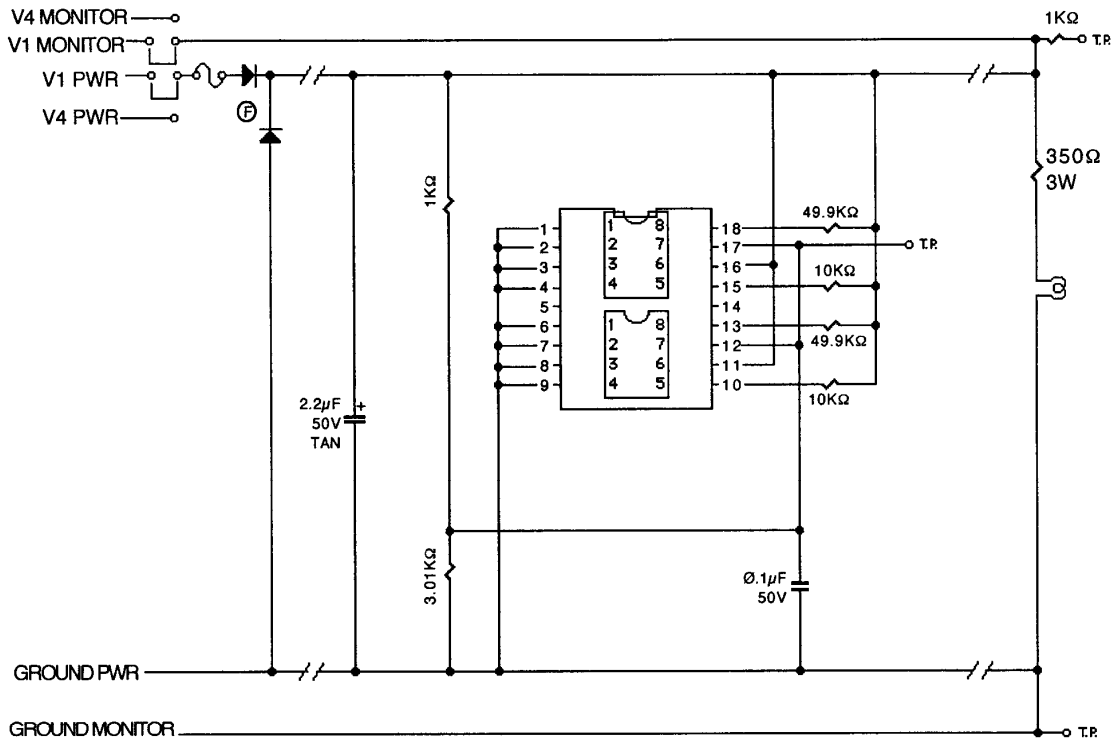


FIGURE 2

BURN-IN CIRCUIT



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Burn-in voltages : V1 = +20V to +22V
3. Ta = +125°C minimum.
4. Tj = +143 °C maximum.
5. Tc = +131°C minimum.
6. Thermal shutdown = +170 °C = +/-5 °C

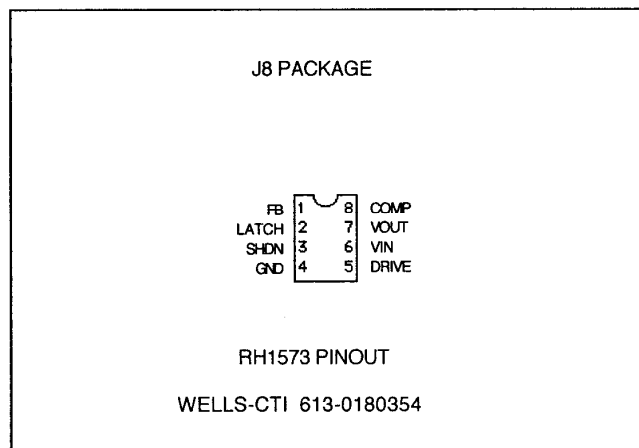
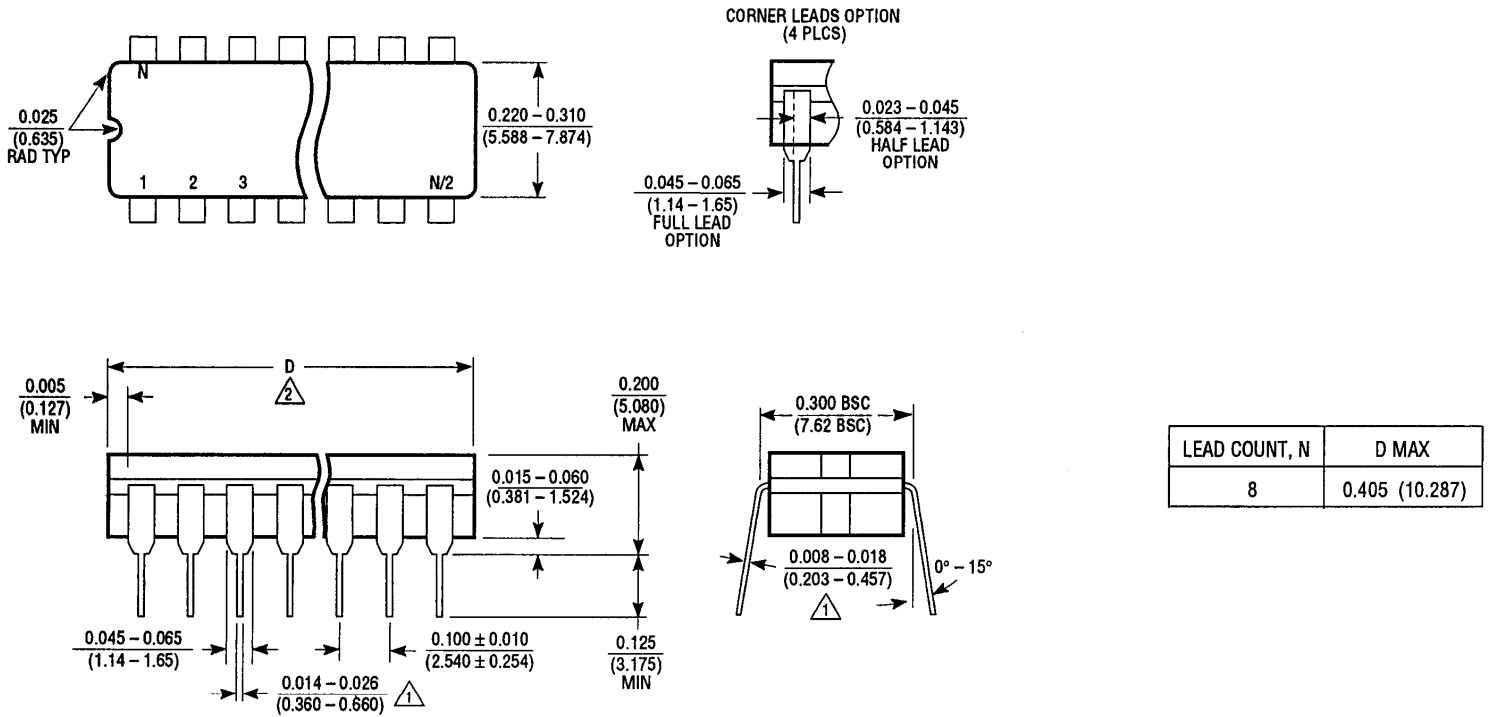


FIGURE 3

(J) Cerdip / 8 LEADS, CASE OUTLINE



NOTE: 1. LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.
 2. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS, AND GLASS OVERRUN

$\theta_{ja} = +110^\circ\text{C/W}$
 $\theta_{jc} = +30^\circ\text{C/W}$

FIGURE 4

TERMINAL CONNECTIONS

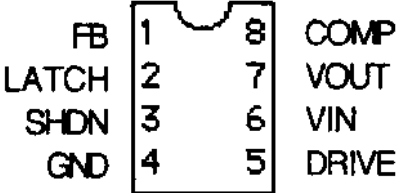


FIGURE 5

TABLE I DICE ELECTRICAL CHARACTERISTICS – ELEMENT EVALUATION

$T_A = 25^\circ\text{C}$

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Reference Voltage	$I_{\text{DRIVE}} = 20\text{mA}$, $T_J = 25^\circ\text{C}$	1.252	1.278	V
Line Regulation (V_{FB})	$I_{\text{DRIVE}} = 20\text{mA}$, $3\text{V} < V_{\text{IN}} < 7\text{V}$		2	mV
Load Regulation (V_{FB})	$I_{\text{DRIVE}} = 20\text{mA}$ to 250mA		18	mV
FB Pin Bias Current	$V_{\text{FB}} = 1.265\text{V}$		4	μA
DRIVE Pin Current	$V_{\text{FB}} = 1.35\text{V}$, $V_{\text{DRIVE}} = 7\text{V}$ $V_{\text{FB}} = 1.15\text{V}$, $V_{\text{DRIVE}} = 1.5\text{V}$	290	1.2	mA mA
DRIVE Pin Saturation Voltage	$I_{\text{DRIVE}} = 20\text{mA}$, $V_{\text{FB}} = 1.15\text{V}$ $I_{\text{DRIVE}} = 250\text{mA}$, $V_{\text{FB}} = 1.15\text{V}$		0.2 1	V V
SHDN Pin Threshold Voltage		1	1.5	V
SHDN Pin Current	$V_{\text{SHDN}} = 5\text{V}$		300	μA
LATCH Pin Latch-Off Threshold Voltage		1.1	1.8	V
LATCH Pin Charging Current		4	10	μA
LATCH Pin Latching Current			0.85	mA
$V_{\text{IN}} - V_{\text{OUT}}$ Differential Threshold for Latch Disable		0.55	0.8	V
Input Quiescent Current	$V_{\text{IN}} = 7\text{V}$		2.8	mA
Minimum Input Voltage for Bias Operation		2.4		V

Note 1: For circuit operation and application information refer to LT1573 data sheet.

TABLE II ELECTRICAL CHARACTERISTICS – Post-Irradiation

 $T_A = 25^\circ\text{C}$

PARAMETER	CONDITIONS	NOTES	10KRAD(Si)		20KRAD(Si)		50KRAD(Si)		100KRAD(Si)		200KRAD(Si)		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Reference Voltage	$I_{\text{DRIVE}} = 20\text{mA}$, $T_J = 25^\circ\text{C}$	2	1.252	1.278	1.252	1.278	1.249	1.281	1.245	1.285	1.239	1.291	V
Line Regulation (V_{FB})	$I_{\text{DRIVE}} = 20\text{mA}$, $3\text{V} < V_{\text{IN}} < 7\text{V}$			2.1		2.2		2.5		3		4	mV
Load Regulation (V_{FB})	$I_{\text{DRIVE}} = 20\text{mA}$ to 250mA			19		20		22		25		30	mV
FB Pin Bias Current	$V_{\text{FB}} = 1.265\text{V}$			4.2		4.5		5		6		7	μA
DRIVE Pin Current	$V_{\text{FB}} = 1.35\text{V}$, $V_{\text{DRIVE}} = 7\text{V}$ $V_{\text{FB}} = 1.15\text{V}$, $V_{\text{DRIVE}} = 1.5\text{V}$		290	1.3	288	1.4	285	1.7	275	2.2	260	3	mA mA
DRIVE Pin Saturation Voltage	$I_{\text{DRIVE}} = 20\text{mA}$, $V_{\text{FB}} = 1.15\text{V}$ $I_{\text{DRIVE}} = 250\text{mA}$, $V_{\text{FB}} = 1.15\text{V}$			0.2 1		0.21 1.02		0.23 1.05		0.25 1.1		0.3 1.2	V V
SHDN Pin Threshold Voltage			1	1.5	1	1.5	1	1.52	1	1.55	1	1.6	V
SHDN Pin Current	$V_{\text{SHDN}} = 5\text{V}$			300		300		300		300		300	μA
LATCH Pin Latch-Off Threshold Voltage			1	1.9	1	2	0.9	2.1	0.8	2.2	0.8	2.2	V
LATCH Pin Charging Current			4.4	10	4.4	10	4.2	10.5	4	11	4	11	μA
LATCH Pin Latching Current				0.85		0.85		0.85		0.85		0.85	mA
$V_{\text{IN}} - V_{\text{OUT}}$ Differential Threshold for Latch Disable			0.5	0.81	0.5	0.82	0.48	0.85	0.45	0.9	0.4	1	V
Input Quiescent Current	$V_{\text{IN}} = 7\text{V}$			2.8		2.8		2.85		2.9		3.1	mA
Minimum Input Voltage for Bias Operation			2.4		2.4		2.4		2.4		2.4		V

Note 2: Operating conditions are limited by maximum junction temperature. The regulated feedback or output voltage specification will not apply for all possible combinations of input voltage, drive voltage and drive current. When operating at maximum drive current, the drive voltage range must be limited. When operating at maximum input and drive voltage, the drive current must be limited.



RH CANNED SAMPLE TABLE FOR QUALIFYING DICE SALES

SUBGROUP	CLASS			OPERATION	MIL-STD-883		QUANTITY (ACCEPT NUMBER) REF. METHOD 2018 FOR S/S
	K/S	V	H/B		METHOD	CONDITION	
1	X	X		SEM	2018	N/A	100%
2	X	X	X	ELEMENT ELECTRICAL (WAFER SORT @ 25°C)			100%
3	X	X	X	ELEMENT VISUAL (2nd OP)	2010	A	100%
4	X	X	X	INTERNAL VISUAL (3rd OP)	2010	A	ASSEMBLED PARTS ONLY
	X	X		DIE SHEAR MONITOR	2019		
5	X	X		BOND PULL MONITOR	2011		ASSEMBLED PARTS ONLY
	X	X		STABILIZATION BAKE	1008	C	
	X	X		TEMPERATURE CYCLE	1010	C	
	X	X		CONSTANT ACCELERATION	2001	E	
	X	X		FINE LEAK	1014	A	
6	X	X		GROSS LEAK	1014	C	45(0)
	X	X		FIRST ROOM ELECTRICAL - READ & RECORD (REPLACE ANY ASSEMBLY-RELATED REJECTS)			
	X	X		PRE BURN-IN ELECT. READ & RECORD @ +125°C or +150°C, -55°C			
	X	X		BURN-IN: +125°C/240 hrs. or +150°C/120 hrs.	1015	+ 125°C MINIMUM 240 HOURS	
	X	X		POST BURN-IN ELECT. READ & RECORD @ 25°C			
	X	X		POST BURN-IN ELECT. READ & RECORD @ +125°C or +150°C, -55°C			
7	X	X		TOTAL IRRADIATION DOSE	1019	A	15(0) OR 25(1) - # of wires
	X	X		PRE OP-LIFE ELECTRICAL @ 25°C READ & RECORD			
	X	X		OPERATING LIFE: +125°C/1000 hrs. or +150°C/500 hrs.	1005	+ 125°C MINIMUM 1000 HOURS	
7	X	X		POST OP-LIFE ELECT. (R & R @ 25°C, +125°C DR +150°C, -55°C)	2011		

NOTE: LTC is not qualified to process to MIL-PRF-38534. This is an LTC imposed element evaluation that follows MIL-STD-883 test methods and conditions. Please note the quantity and accept number from Sample Size Series of 5%, accept on 0, and note that the actual sample and accept number does not begin until Subgroup 6 OP-LIFE.

NOTE: Tests within Subgroup 5 may be performed in any sequence.

NOTE: LTC's radiation tolerance (RH) die has a topside glassivation thickness of 4KA minimum.

NOTE: Sample sizes on the travelers may be larger than that indicated in the above table; however, the larger sample size is to accommodate extra units for replacement devices in the event of equipment or operator error and for assembly related rejects in Subgroup 6, and for Wire Bond Evaluation, Subgroup 7. The larger sample size is at all times kept segregated and, if used for qualification, has all the required processing imposed.