RH27, PRECISION OPERATIONAL AMPLIFIER

										RECO	ORD									
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0		TIAL RE																	6/12	
A	 PAGE 2 - ADDED PARAGRAPHS 3.2.1 - 3.2.3 REFERENCING THE PACKAGE OPTIONS. PARAGRAPH 3.3.b, ADDED "(SEE PARAGRAPH 3.2)". PARAGRAPH 3.2.3, CHANGED PACKAGE OPTION FROM "10LEAD FLATPACK" TO "10 LEAD BOTTOM BRAZED FLATPACK". PAGE 3, PARAGRAPH 3.6 – CHANGED "TABLE I" AND "TABLE IA" TO "TABLE 1" AND 										08/01	/97								
	 PAGE 3, PARAGRAPH 3.6 – CHANGED "TABLE I" AND "TABLE IA" TO "TABLE 1" AND "TABLE 1A" TO MATCH THE ACTUAL TABLES ON PAGES 17 AND 18. PAGE 4 – DELETED PARAGRAPH 3.12.1. 																			
	•	PAGE 6 PAGE 9	, FIGUR	E 1, F	PAGE	7, FIC	URE	2, ANI		-					jc, A	ND T	ıMAX			
	•	PAGES	10 - 13,	FIGU	RES 7	7 – 10 -	– REM	10VEI	O REF	EREN	CE TC	LT	C SPEC							
	•	PAGES SUPPLI BRAZE	ED BY (CUST	OME	R. CH	[ANG]	ED PA												
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C		PAGE 4									AC DI	-DE	ENIED					1	2/01	/97
		PAGE 5 PAGE 6				-				-					.GR A	NPH 4	.5.			
		SOURC	E INSPE	ECTIC	N W	AS RE	DEFI	NED.												
D	•	PAGE 5 CATAS	TROPHI	IC FA	ILUR	ES. A	DDEI	A SE	CONI) PAG	E FOR	RE	VISION						3/20	/98
Е	•									E ADDITIONAL PAGE. GE OPTION FROM "10 LEAD BOTTOM				1	10/16/98					
		BRAZE FLATPA BRAZE "BOTTO	ACK" TO D FLAT	O "(W Pack) CER (" TO	PAK' "(W)	'. PAC CERP	GE 10 (AK".	CHAN PAGE	GED (15, 16	OPTIO 5, CHA	N 3 NG	FROM ED FIG	"(WB) URE 11	BOT , 12,	TOM FROM	М	,,,		
F		PAGE 7	, TO5 C														MAK		7/19/99	
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G	• PAGE 9, FIGURE 3, CHANGED θja AND θjc.	09/29/99
Н	 PAGE 3, PARAGRAPHS 3.2.1, 3.2.2, 3.2.3 HAD FIGURES 1, 2, 3 REMOVED. PAGE 4, PARAGRAPH 3.7 CHANGED VERBIAGE FROM "SPECIFIED IN TABLE III" TO "AND AS SPECIFIED IN TABLE III HEREIN", LINE 2. PARAGRAPH 3.9 ADDED "HEREIN" AFTER "TABLE II", LINE 2. PAGE 5, PARAGRAPH 4.3, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.1, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.2.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IIA OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IIA IN MIL-STD-883". PAGE 6, PARAGRAPH 4.4.3.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IV OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IV IN MIL-STD-883". 	01/04/00
J	• PAGE 9, CHANGED THETA JA TO θJA=170°C/W AND THETA JC TO θJC=40°C/W FROM θJA=225°C/W AND θJC=18°C/W PER PACKAGE ENGINEER.	09/05/00
K	 PAGE 3, PARAGRAPHS 3.2.1, 3.2.2, 3.2.3, ADDED "OPTION" BEFORE EACH DEVICE SELECTION. PAGE 4, PARAGRAPH 3.6, TABLE IA CHANGED TO TABLE II. PARAGRAPH 3.7, TABLE III CHANGED TO TABLE IV. PARAGRAPH 3.10.3, ADDED "DEVICE OPTIONS 1, 2, AND 3" TO LINE 1. 	11/07/02
	 PAGE 5, PARAGRAPH 3.11.1 WAS CHANGED FROM "dosage rate of approximately 20 Rads per second" TO "dosage rate of less than or equal to 10 Rads per second". PARAGRAPHS 4.1 THROUGH 4.4.2.1 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. 	
	PAGE 6, PARAGRAPH 4.4.3 CHANGE WAS DONE TO CLARIFY GROUP SAMPLING. PARAGRAPHS 4.6.2 THROUGH 4.6.4 WERE RE-WRITTEN. THESE DATA PROVIDED, AND DATA AVAILABLE. PARAGRAPH 4.6.10 NOTE, ADDED FURTHER EXPLANATION OF MINIMUM DELIVERED DATA.	
	PAGES 8 THROUGH 18, ALL FIGURE TITLES CHANGED TO HAVE DEVICE OPTIONS AND PACKAGE TYPES AT TOP OF PAGE, AND HAVE ALL FIGURES AT BOTTOM OF PAGE.	
	PAGE 9, CASE OUTLINE EDITED TO REFLECT ONLY THE 8 LEAD PACKAGE INFORMATION. FIGURE 2, SHOULDER OF LEAD WIDTH MAXIMUM INCREASED BY .003 INCHES.	
	PAGE 10, CASE OUTLINE WAS UPDATED TO MEET MIL-STD-1835. FIGURE 3, PACKAGE THICKNESS MAXIMUM INCREASED BY .005 INCHES. PACKAGE WIDTH AND LENGTH MAXIMUMS INCREASED BY .01 AND .02 INCHES, RESPECTIVELY.	
	PAGE 11, MOVED FIGURES 4, 5, 6 FOR BETTER FIT ON PAGE.	
	PAGE 13, FIGURE 8, ADDED PACKAGE PINOUTS.	
	PAGE 14, FIGURE 9, ADDED PACKAGE PINOUTS.	
	PAGE 15, FIGURE 10, ADDED PACKAGE PINOUTS.	
	PAGE 16, FIGURE 11, ADDED PACKAGE PINOUTS.	
	PAGE 17, FIGURE 12, ADDED PACKAGE PINOUTS.	
	PAGE 19, ADDED NOTE 8 AFTER TABLE II.	
L	PAGE 9, CHANGED OUTLINE DRAWING PIN 1 NOTCH MOVED TO INSIDE LEAD LOCATION.	05/19/03
M	PAGE 4, CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC.	03/16/05
N	• PAGE 5, CHANGED IN 4.2 & 4.3 PARAGRAPHS IN CONJUNCTION TO 3.3 CHANGED TO PARAGRAPH 3.4	07/16/07
P	• PAGE 5, PARAGRAPH 4.3 CHANGED 3.1.1 TO 3.1 AND 3.2.1 TO 3.1.1	09/10/07
Q	PAGE 4, PARAGRAPH 3.10.3 ADDED OPTION 3 IS ALLOY 42 FOR FLATPACK.	10/19/07

	REVISION RECORD	
REV	DESCRIPTION	DATE
R	 PAGE 6, PARAGRAPH 3.11.1 CHANGED VERBIAGE PAGE 5, PARAGRAPH 3.10.3 CHANGED OPTION 2 TO ALLOY 42 PACKAGE REQUIREMENT. 	04/29/08
S	 PAGE 6, PARAGRAPH 4.4.2 CHANGED VERBIAGE. PAGE 10, FIGURE 3 NOTE 2 ADDED TO LEAD THICKNESS. 	05/27/08
Т	 ADDED OPTION 4 & OPTION 5 THROUGH OUT SPEC. Page 16, ADDED DYNAMIC BURN-IN CIRCUIT INFORMATION Removed the "C" from RH27 header. Page 19, 20, Added updated data sheet. 	01/23/09
U	 PAGE 4, PARAGRAPH 3.2.6, ADDED OPTION 6, RH27AEW (GLASS SEAL FLATPACK, 10 LEADS). PAGE 5, PARAGRAPH 3.8.3, ADDED OPTION 6 TO BURN-IN REQUIREMENT. PAGE 5, PARAGRAPH 3.10.3, ADDED OPTION 6 TO LEAD MATERIAL AND FINISH. PAGE 10, FIGURE 3, ADDED DEVICE OPTION 6 TO W10 GLASS SEALED FLATPACK. PAGE 11, FIGURE 6, ADDED DEVICE OPTION 6 TO GLASS SEALED FLATPACK TERMINAL CONNECTIONS. PAGE 16, FIGURE 11, ADDED OPTION 6 TO STATIC BURN-IN CIRCUIT. PAGE 17, FIGURE 12, ADDED OPTION 6 TO DYNAMIC BURN-IN CIRCUIT. 	01/20/12
V	PAGE 5, PARAGRAPH 3.5, AMENDED ESD CLASSIFICATION FROM CLASS 1 TO CLASS 2.	05/23/12
W	TO REMOVE SI AND CHANGE LINEAR TECHNOLOGY TO ANALOG DEVICES	3/22/21

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535	Integrated Circuits	(Microcircuits)	Manufacturing.	General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

- 3.1 General Description: This specification details the requirements for the RH27 Precision Operational Amplifier, processed to space level manufacturing flow.
- 3.2 Part Number:
 - 3.2.1 Option 1 RH27CH (TO5 Metal Can, 8 Leads)
 - 3.2.2 Option 2 RH27CJ8 (Ceramic Dip, 8 Leads)
 - 3.2.3 Option 3 RH27CW (Glass Seal Flatpack, 10 Leads)
 - 3.2.4 Option 4 RH27EW (Glass Seal Flatpack, 10 Leads)
 - 3.2.5 Option 5 RH27EH (TO5 Metal Can, 8 Leads)
 - 3.2.6 Option 6 RH27AEW (Glass Seal Flatpack, 10 Leads)

Note: RH27AEW is marked and processed as RH27EW. Orders will be delivered with an additional screening at 25°C, -55°C to 125°C to the VOS specification shown on Table 1.

- 3.3 Part Marking Includes:
 - a. LTC Logo
 - b. LTC Part Number (See Paragraph 3.2)
 - c. Date Code
 - d. Serial Number
 - e. ESD Identifier per MIL-PRF-38535, Appendix A
- 3.4 The Absolute Maximum Ratings:

Input Voltage Equal to Supply Voltage

Lead Temperature (Soldering, 10 sec) +300°C

<u>1</u>/ The RH27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ± 0.7 V, the input current should be limited to 25mA.

- 3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 2.
- 3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and **Table II.**
- 3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in **Table IV** herein.
- 3.8 Burn-In Requirement:
 - 3.8.1 Option 1, 5 (TO5): Static Burn-In, Figure 7; Dynamic Burn-In, Figure 8
 - 3.8.2 Option 2 (Ceramic Dip): Static Burn-In, Figure 9; Dynamic Burn-In, Figure 10
 - 3.8.3 Options 3, 4, 6: (Glass Sealed Flatpack): Static Burn-In, Figure 11; Dynamic Burn-In, Figure 12
- 3.9 Delta Limit Requirement: Delta limit parameters are specified in **Table III** herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.
- 3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.
 - 3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1, Figure 2, and Figure 3.
 - 3.10.2 Terminal Connections: The terminal connections shall be as specified in Figure 4, Figure 5, and Figure 6.

- 3.10.3 Lead Material and Finish: The lead material and finish for Device Options 1, 5 shall be Kovar and Options 2, 3, 4, and 6 are Alloy 42. The lead finishes shall be hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.
- 3.11 Radiation Hardness Assurance (RHA):
 - 3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.
 - 3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.
 - 3.11.3 Total dose bias circuit is specified in Figure 13.
- 3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.
- 3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.
- 4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)
 - 4.1 <u>Quality Assurance Provisions</u>: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Analog Devices is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.
 - 4.2 <u>Sampling and Inspection</u>: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.
 - 4.3 <u>Screening</u>: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1, and 3.4 of the test method. Electrical testing shall be as specified in **Table IV** herein.
 - 4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.
 - 4.4 <u>Quality Conformance Inspection</u>: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:
 - 4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in **Table IV** herein.
 - 4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, subgroups 1-4 plus 6 are performed on every assembly lot, and Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1 Group B, Subgroup 2c = 10%

Group B, Subgroup **3** = 10%

Group B, Subgroup 4 = 5%

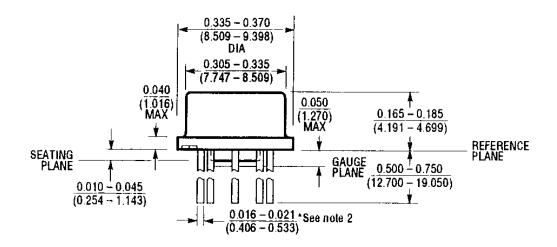
Group B, Subgroup **5** = *5% (*per wafer or inspection lot whichever is the larger quantity) Group B, Subgroup **6** = 15%

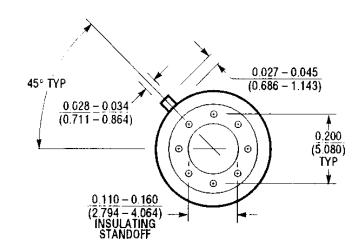
- 4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.
- 4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.
 - 4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).
 - 4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

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- 4.5 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:
 - 4.5.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.
 - 4.5.2 100% attributes (completed lot specific traveler; includes Group A Summary)
 - 4.5.3 Burn-In Variables Data and Deltas (if applicable)
 - 4.5.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)
 - 4.5.5 Generic Group D data (4.4.3 herein)
 - 4.5.6 SEM photographs (3.13 herein)
 - 4.5.7 Wafer Lot Acceptance Report (3.13 herein)
 - 4.5.8 X-Ray Negatives and Radiographic Report
 - 4.5.9 A copy of outside test laboratory radiation report if ordered
 - 4.5.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.
 - Note: Items 4.5.1 and 4.5.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as "No Charge Data".
- 5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

DEVICE OPTION # 1, 5 (H) TO5 / 8 LEADS CASE OUTLINE





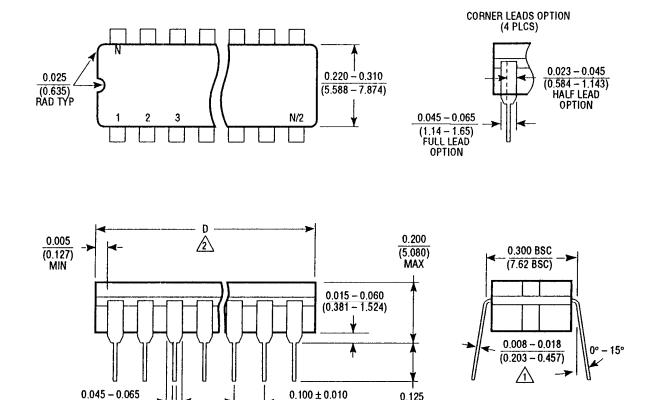
NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

 θ ja = +150°C/W θ jc = +40°C/W

FIGURE 1

DEVICE OPTION # 2 (J8) CERAMIC DIP / 8 LEADS CASE OUTLINE



 0.100 ± 0.010

 (2.540 ± 0.254)

0.014 - 0.026(0.360 - 0.660) 0.125

(3,175) MIN

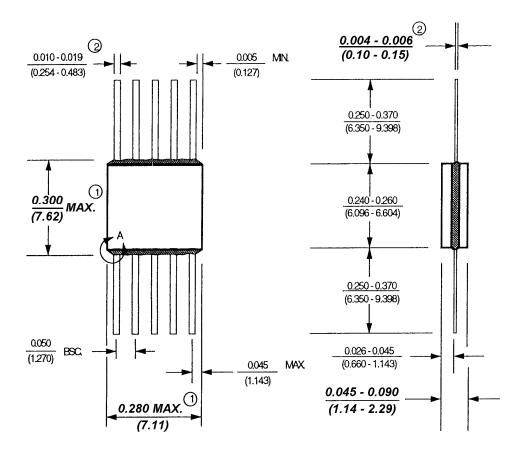
NOTE: 1. LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS. 2. 8 LEAD D MAX = .405 (10.287)

 θ ja = +110°C/W $\theta jc = +30$ °C/W

(1.14 - 1.65)

FIGURE 2

DEVICE OPTION #3, 4, 6 (W10) GLASS SEALED FLATPACK / 10LEADS CASE OUTLINE



NOTE: 1. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVER RUN.

NOTE: 2. INCREASE DIMENSION BY 0.003 INCH WHEN LEAD FINISH IS APPLIED (SOLDER DIPPED).

$$\theta$$
ja = +170°C/W
 θ jc = +40°C/W

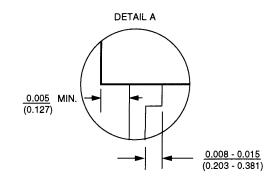
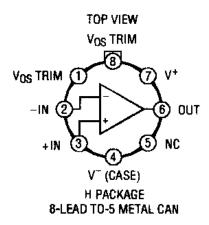


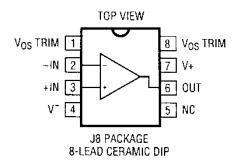
FIGURE 3

TERMINAL CONNECTIONS

DEVICE OPTION #1, 5 TO5 10 LEAD METAL CAN



DEVICE OPTION #2, 8 LEAD CERAMIC DIP



<u>DEVICE OPTION #3, 4, 6 GLASS SEALED</u> <u>10 LEAD FLATPACK</u>

FIGURE 5

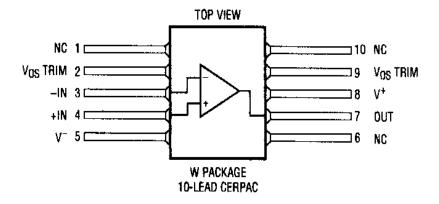
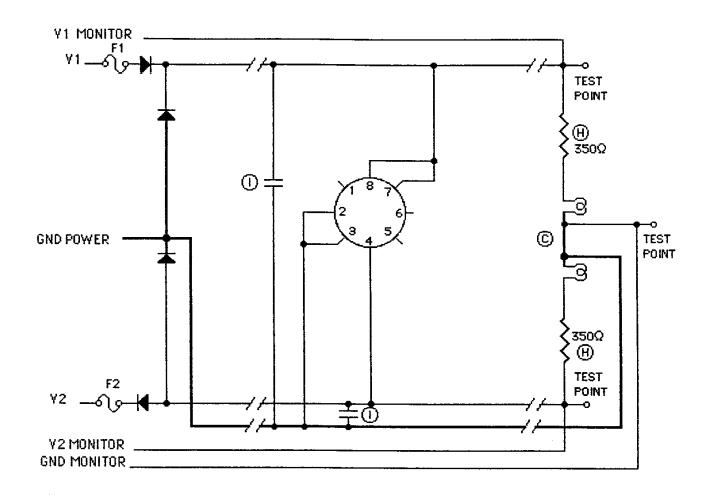


FIGURE 6

STATIC BURN-IN CIRCUIT

OPTION 1, 5 TO5 METAL CAN / 8 LEADS



NOTES:

- 1. Unless otherwise specified, component tolerances shall be per military specification.
- 2. Tj = +181 °C maximum.
- 3. Ta = +150 °C to +158 °C maximum ambient.
- 4. Burn-in Yoltages: Y1 = + 18Y to +19.8Y Y2= - 18Y to -19.8Y

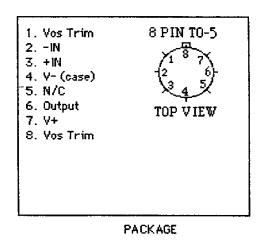
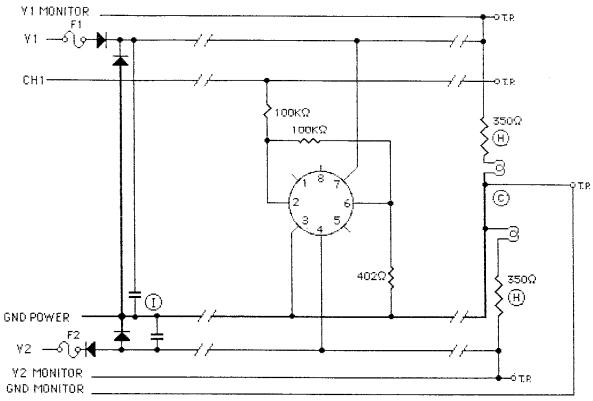


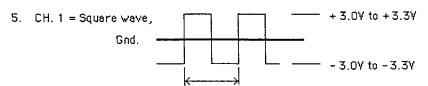
FIGURE 7

DYNAMIC BURN-IN CIRCUIT OPTION 1, 5 TO5 METAL CAN / 8 LEADS



NOTES:

- Unless otherwise specified, component tolerances shall be per military specification.
- 2. Tj = +175 °C maximum.
- 3. Ta = +125 °C to +133 °C maximum ambient.
- 4. Burn-in Yoltages: Y1 = + 18Y to +19.8Y Y2 = - 18Y to -19.8Y



Frequency, 4.5hz(222ms) to 5.5hz(182ms)

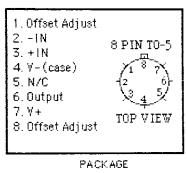
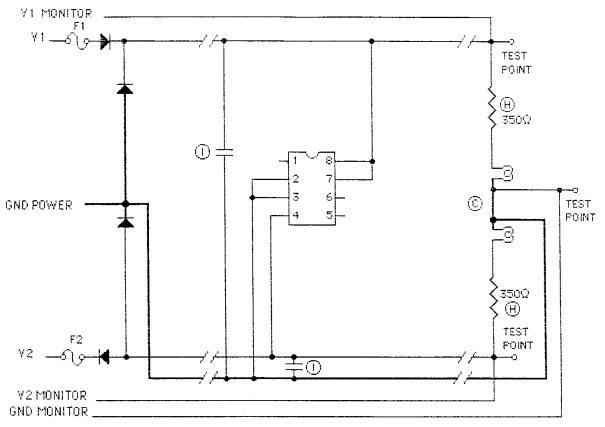


FIGURE 8

STATIC BURN-IN CIRCUIT

OPTION #2, CERDIP / 8 LEADS



NOTES:

- 1. Unless otherwise specified, component tolerances shall be per military specification.

- 2. Tj = +175 °C maximum.
 3. Ta = +150 °C to +158 °C maximum ambient.
 4. Burn-in Yoltages:Y1 = + 18Y to +19.8Y
 Y2= 18Y to -19.8Y

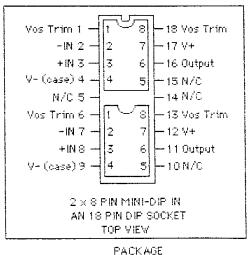
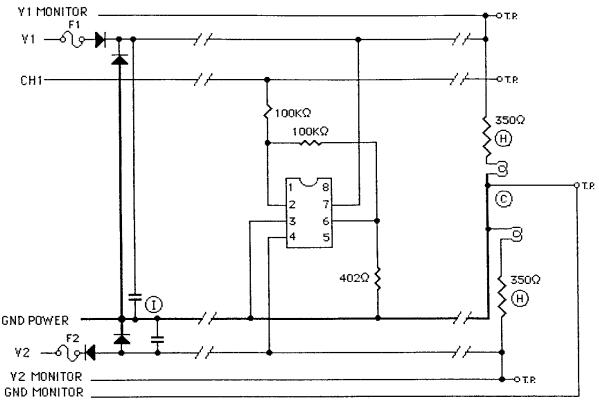


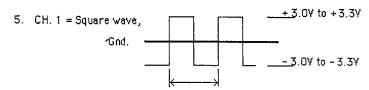
FIGURE 9

DYNAMIC BURN-IN CIRCUIT OPTION 2, CERDIP / 8 LEADS



NOTES:

- Unless otherwise specified, component tolerances shall be per military specification.
- 2. Tj = +163 °C maximum.
- 3. Ta = +125 °C to +133 °C maximum ambient.
- 4. Burn-in Yoltages: Y1 = + 18Y to +19.8Y Y2= - 18Y to -19.8Y



Frequency, 4.5hz(222ms) to 5.5hz(182ms)

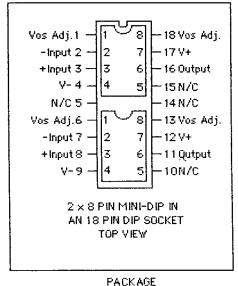
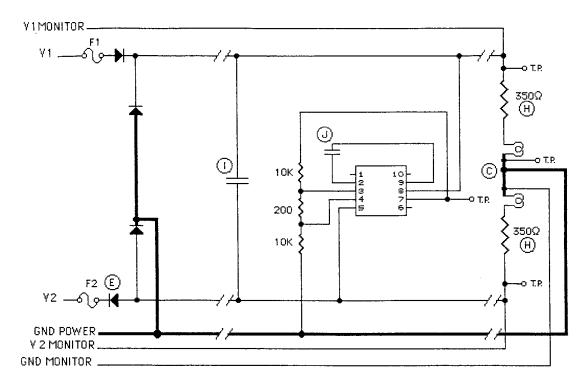


FIGURE 10

STATIC BURN-IN CIRCUIT

OPTION 3, 4, 6 GLASS SEALED FLATPACK / 10 LEAD



Notes:

- 1. Unless otherwise specified, components tolerances shall be per military specification.
- 2. Tj = 150°C maximum *
- 3. Ta = 125°C
- 4. Burn-in Voltages: V1 = +18V to +19.8V V2 = -18V to -19.8V
- *Tj Calculation is based on:
- a) Icc = 3.85mA maximum @ ±19.8V
- b) θja of 112°C/W as supplied by customer

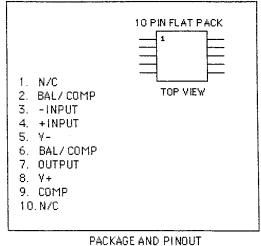
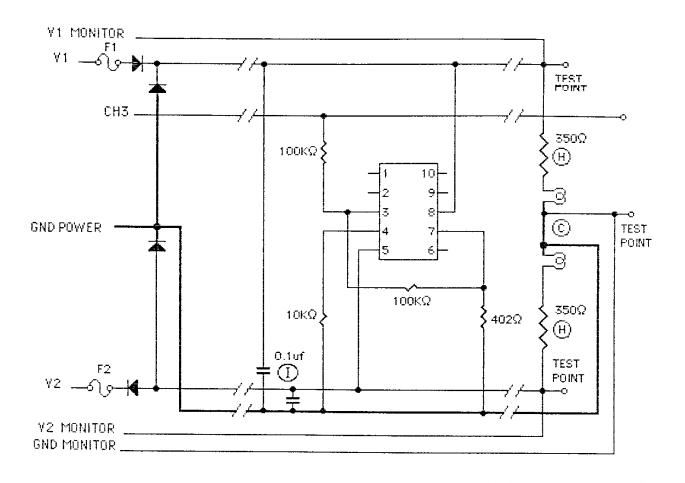


FIGURE 11

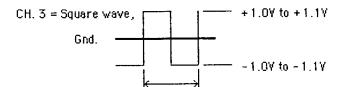
DYNAMIC BURN-IN CIRCUIT

OPTION 3, 4, 6 GLASS SEALED FLATPACK / 10 LEAD



NOTES:

- 1. Unless otherwise specified, component tolerances shall be per military specification.
- 2. Tj = 156°C maximum. *
- 3. Ta = 125°C.
- 4. Burn-in Voltages: V1 = +18V to +19.8V V2 = -18V to -19.8V



Frequency, 4.5hz(222ms) to 5.5hz(182ms)

- *Tj Calculation is based on:
 - a) lcc = 3.85mA maximum @±19.8¥
 - b) 0ja of 112 °C/W as supplied by customer.
- 1. N/C
 2. Yos TRIM
 3. INPUT
 4. + INPUT
 5. Y6. N/C
 7. OUTPUT
 7. OUTPUT
 7. Y9. Yos TRIM
 10. N/C

PACKAGE AND PINOUT

FIGURE 12

TOTAL DOSE BIAS CIRCUIT

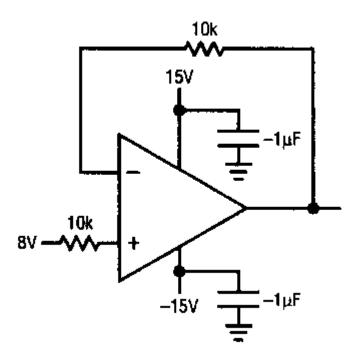


FIGURE 13

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION) NOTE 9

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	A = 25°(TYP	C MAX	SUB- GROUP	–55°(MIN	C ≤ T _A ≤ 125° TYP M		UB- ROUP	UNITS
V _{OS}	Input Offset Voltage	RH27AE RH27E RH27C	11 1 1			35 55 100	4 4 4		6 10 30	00 2	2, 3 2, 3 2, 3	۷ب ۷ب ۷ب
ΔV _{OS} ΔTemp	Average Offset Drift	RH27E RH27C	4, 7 4, 7						1	8		μV/°C μV/°C
$\Delta V_{OS} \over \Delta Time$	Long-Term Input Offset Voltage Stability	RH27E RH27C	2, 4 2, 4	·		1 2						μV/ Month
los	Input Offset Current	RH27E RH27C				35 75	1		5 10	0 2 35 2	2, 3 2, 3	nA nA
l _B	Input Bias Current	RH27E RH27C				±40 ±80	1			50 2 50 2	2, 3 2, 3	nA nA
en	Input Noise Voltage	0.1Hz to 10Hz (RH27E) 0.1Hz to 10Hz (RH27C)	4, 5 4, 5			0.18 0.25						μV _{P-P} μV _{P-} p
	Input Noise Voltage Density	f ₀ = 10Hz (RH27E) f ₀ = 30Hz (RH27E) f ₀ = 1000Hz (RH27E) f ₀ = 10Hz (RH27C) f ₀ = 30Hz (RH27C) f ₀ = 1000Hz (RH27C)	3 4 4 3 4 4			5.5 4.5 3.8 8 5.6 4.5						nV/√Hz nV/√Hz nV/√Hz nV/√Hz nV/√Hz nV/√Hz
in	Input Noise Current Density	f ₀ = 1000Hz	4, 6			0.6						pA∕√Hz
	Input Resistance Common Mode	RH27E RH27C			3 2							GΩ GΩ
	Input Voltage Range	RH27E RH27C	4 4	±11				±10.3 ±10.2	,			V
CMRR	Common Mode Rejection Ratio	V _{CM} = ±11V (RH27E) V _{CM} = ±10V (RH27E) V _{CM} = ±11V (RH27C) V _{CM} = ±10V (RH27C)		114 100			1	108 94			2, 3 2, 3	dB dB dB dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$ (RH27E) $V_S = \pm 4.5V$ to $\pm 18V$ (RH27E) $V_S = \pm 4V$ to $\pm 18V$ (RH27C) $V_S = \pm 4.5V$ to $\pm 18V$ (RH27C)		100 94			1	96 86			2, 3 2, 3	dB dB dB
AvoL	Large-Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_0 = \pm 10V$ (RH27E) $R_L \ge 600\Omega$, $V_0 = \pm 1V$ (RH27E) $V_S = \pm 4V$	4	1000 250			4	600			5, 6	V/mV V/mV
		$R_L \ge 2k\Omega$, $V_0 = \pm 10V$ (RH27C) $R_L \ge 600\Omega$, $V_0 = \pm 1V$ (RH27C) $V_S = \pm 4V$	4	700 200			4	300			5, 6	V/mV V/mV
V _{OUT}	Maximum Output Voltage Swing	$\begin{array}{l} R_L \geq 2k\Omega \ (RH27E) \\ R_L \geq 600\Omega \ (RH27E) \\ R_L \geq 2k\Omega \ (RH27C) \\ R_L \geq 600\Omega \ (RH27C) \end{array}$		±12 ±10 ±11.5 ±10			4 4 4 4	±11.5 ±10.5			5, 6 5, 6	V
SR	Slew Rate	$R_L \ge 2k\Omega$		1.7			7	<u> </u>		_		V/µs
GBW	Gain-Bandwidth Product	f ₀ = 100kHz	4	5								MH2
Z ₀	Open-Loop Output Resistance	$V_0 = 0$, $I_0 = 0$			70							Ω
$\overline{P_0}$	Power Dissipation	RH27E RH27C				140 170	1 1				·	mW mW

NOTES ARE ON THE NEXT PAGE.

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION) NOTE 10

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD(Si) MIN MAX	20KRAD(Si) MIN MAX	50KRAD(Si) MIN MAX	100KRAD(Si) Min Max	200KRAD(Si) Min Max	UNITS
V _{0S}	Input Offset Voltage	RH27E RH27C	1	55 100	80 130	100 180	150 280	200 400	μV μV
los	Input Offset Current	RH27E RH27C		35 75	40 75	50 90	60 120	90 180	nA nA
IB	Input Bias Current	RH27E RH27C		±40 ±80	±50 ±80	±80 ±125	±100 ±200	±200 ±400	nA nA
	Input Resistance Common Mode	RH27E RH27C		3 (Typ) 2 (Typ)	GΩ GΩ				
	Input Voltage Range		4	±11	±11	±11	±11	±11	٧
CMRR	Common Mode Rejection Ratio	V _{CM} = ±11V (RH27E) V _{CM} = ±11V (RH27C)		114 100	114 100	110 97	105 94	100 90	dB dB
PSRR	Power Supply Rejection Ratio	V _S = ±4V to ±18V (RH27E) V _S = ±4V to ±18V (RH27C)		100 94	100 94	98 92	96 90	94 86	dB dB
Avol	Large-Signal Voltage Gain	$\begin{array}{l} R_L \geq 2k\Omega, V_0 = \pm 10V \; (RH27E) \\ R_L \geq 2k\Omega, V_0 = \pm 10V \; (RH27C) \end{array}$		1000 700	1000 700	1000 700	900 700	800 400	V/mV V/mV
V _{OUT}	Maximum Output Voltage Swing	$\begin{array}{l} R_L \geq 2k\Omega \ (RH27E) \\ R_L \geq 600\Omega \ (RH27E) \\ R_L \geq 2k\Omega \ (RH27C) \\ R_L \geq 600\Omega \ (RH27C) \end{array}$		±12 ±10 ±11.5 ±10	±12 ±10 ±11.5 ±10	±12 ±10 ±11.5 ±10	±12 ±10 ±11.5 ±10	±12 ±10 ±11.5 ±10	V V V
Z ₀	Open-Loop Output Resistance	$V_0 = 0, I_0 = 0$		70 (Typ)	Ω				
PD	Power Dissipation	RH27E RH27C		140 170	140 170	140 170	140 170	140 170	mW mW

Note 1: Input offset voltage measurements are performed by automatic **test equipment approximately 0.5** seconds after application of power.

Note 2: Long-term input offset voltage stability refers to the averaged trend line of offset voltage vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5 μ V. Refer to the typical performance curve.

Note 3: Sample tested to an LTPD of 15 on every lot. Contact factory for 100% testing of 10Hz voltage density noise.

Note 4: Parameter is guaranteed by design, characterization, or correlation to other tested parameters.

Note 5: See test circuit and frequency response curve for 0.1Hz to 10Hz tester on OP-27/OP-37 data sheet.

Note 6: See test circuit for current noise measurement on OP-27/OP-37 data sheet.

Note 7: The average input offset drift performance is within the specifications unnulled or when nulled with a pot having a range $8k\Omega$ to $20k\Omega$.

Note 8: The RH27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

Note 9: $V_S = \pm 15V$, $V_{CM} = 0V$ unless otherwise noted.

Note 10: $T_A = 25$ °C, $V_S = \pm 15$ V, $V_{CM} = 0$ V, unless otherwise noted.

Note 11: RH27AEW is marked and processed as RH27EW. Orders will be delivered through box stock screening at 25°C, -55°C to 125°C to the V_{OS} specification shown on Table 1.

0.1Hz TO 10Hz NOISE TEST CIRCUIT

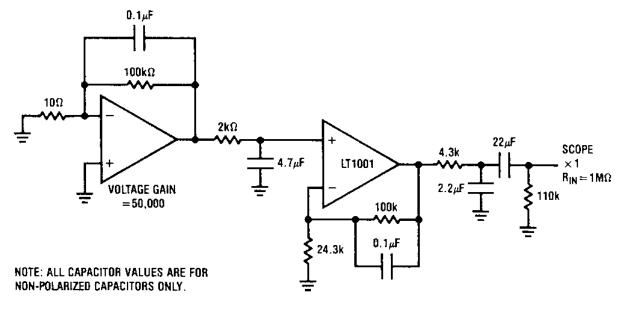


FIGURE 14

CURRENT NOISE MEASUREMENT

Current Noise is measured and calculated by the following formula:

$$i_n = \frac{[e^2_{no} - (130 \text{nV})^2]}{1 \text{M}\Omega \times 100}^{\frac{1}{2}}$$

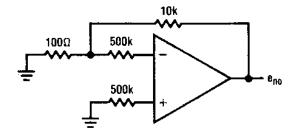


FIGURE 15

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

 $T_A = 25$ °C, $V_{CC} = \pm 15$ V

	ENDPOIN	NT LIMIT	DEI		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
Vos	-100	100	-75	75	μV
$+I_{B}$	-80	80	-30	30	nA
-I _B	-80	80	-30	30	nA

TABLE IV: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
FINAL ELECTRICAL TEST REQUIREMENTS (METHOD	1*, 2, 3, 4, 5, 6, 7
5004)	
GROUP A TEST REQUIREMENTS (METHOD 5005)	1, 2, 3, 4, 5, 6, 7
GROUP B AND D FOR CLASS S ENDPOINT ELECTRICAL	1, 2, 3
PARAMETERS (METHOD 5005)	

^{*}PDA APPLIES TO SUBGROUP 1.

PDA TEST NOTE: The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1 and delta rejects after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.