REVISION RECORD

REV	DESCRIPTION	DATE
0	INITIAL RELEASE	09/10/15
A	**CHANGE FOOTER FROM LTC TO ANALOG DEVICE INC. REMOVED 6.4.1 - THE MANUFACTURER WILL COORDINATE SOURCE INSPECTION AT WAFER LOT ACCEPTANCE AND PRE-SEAL INTERNAL VISUAL**	**01/15/19**
B	**ALIGNED EC TABLES TO ALIGN WITH PACKAGE PART DATA SHEET; ADDED DETAIL TO NOTE 4 AND ADDED NOTE 5; CORRECTED BURN-IN AND RADIATION CIRCUITS; ADDED BURN-IN DELTA PARAMETERS TABLE; REMOVED DWF OPTION REMOVE SI AND CHANGE LINEAR TECHNOLOGY TO ANALOG DEVICE**	**02/01/2021**

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

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				ANALOG DEVICES INC.
	ORIG			
	DSGN			TITLE: **MICROCIRCUIT, LINEAR, RH3845MK HIGH VOLTAGE SYNCHRONOUS STEP-DOWN CONTROLLER DICE**
	ENGR			
	MFG			
	CM			
	QA			SIZE: — / CAGE CODE: **64155** / DRAWING NUMBER: **05-08-5745** / REV: **B**
	PROG			
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:

FOR OFFICIAL USE ONLY

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-STD-883	Test Method and Procedures for Microcircuits
MIL-STD-1835	Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH3845 STEP-DOWN CONTROLLER DICE and Element Evaluation Test Samples, processed to space level manufacturing flow as specified herein.

3.2 Part Number: **RH3845MKDice**

3.3 **Special Handling of Dice:** Rad Hard dice require special handling as compared to standard IC dice. Rad Hard dice are susceptible to surface damage due to the absence of silicon nitride passivation that is present on most standard dice. Silicon nitride protects the dice surface from scratches by its hard and dense properties. The passivation on Analog Devices Rad Hard dice is silicon dioxide which is much “softer” than silicon nitride. During the visual and preparation for shipment, ESD safe Tweezers are used and only the edges of the die are touched.

ADI recommends that dice handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die in or out of the chip shipment tray (waffle pack), use an ESD-Safe-Plastic-tipped Bent Metal Vacuum Probe, preferably .020” OD x .010” ID (for use with tiny parts). The wand should be compatible with continuous air vacuums. The tip material should be static dissipative Delrin (or equivalent) plastic.

During die attach, care must be exercised to ensure no tweezers, or other equipment, touch the top of the dice.

3.4 The Absolute Maximum Ratings:
(Note 1, 5) (All voltages relative to V_{OUT})

V_{IN}	65V
BOOST	80V
BOOST to SW	24V
V_{CC} MODE	24V
$SENSE^+$, $SENSE^-$	40V
$SENSE^+$ to $SENSE^-$	±1V
SYNC, V_{FB} AND C_{SS}	5V
SHDN Pin Current	1mA
Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C

3.5 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.6 Outline Dimensions and Pad Functions: Dice outline dimensions, pad functions, and locations shall be specified in **Figure 1**.

3.7 Radiation Hardness Assurance (RHA):

3.7.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.7.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.7.3 Total dose bias circuit – Run Mode is specified in **Figure 2**.

3.7.4 Total dose bias circuit – Shutdown Mode is specified in **Figure 3.**

3.8 Wafer (or Dice) Probe: Dice shall be 100% probed at T_A = +25°C to the limits shown in **Table I** herein. All reject dice shall be removed from the lot. This testing is normally performed prior to dicing the wafer into chips. Final specifications after assembly are sample tested during the element evaluation.

3.9 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Top side glassivation thickness shall be a **minimum of 4KÅ.**

3.10 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018. Copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

3.11 Traceability: Wafer Diffusion Lot and Wafer traceability shall be maintained through Quality Conformance Inspection.

4.0 QUALITY CONFORMANCE INSPECTION: Quality Conformance Inspection shall consist of the tests and inspections specified herein.

5.0 SAMPLE ELEMENT EVALUATION: A sample from each wafer supplying dice shall be assembled and subjected to element evaluation per **Table VI** herein.

5.1 100 Percent Visual Inspection: All dice supplied to this specification shall be inspected in accordance with MIL-STD-883, Method 2010, Condition A. All reject dice shall be removed from the lot.

5.2 Electrical Performance Characteristics for Element Evaluation: The electrical performance characteristics shall be as specified in **Table I, Table II, Table III, Table IV, and Table V** herein.

5.3 Sample Testing: Each wafer supplying dice for delivery to this specification shall be subjected to element evaluation sample testing. No dice shall be delivered until all the lot sample testing has been performed and the results found to be acceptable unless the customer supplies a written approval for shipment prior to completion of wafer qualification as specified in this specification.

5.4 Part Marking of Element Evaluation Sample Includes**:**

5.4.1 LTC Logo

5.4.2 LTC Part Number

5.4.3 Date Code

5.4.4 Serial Number

5.4.5 ESD Identifier per MIL-PRF-38535, Appendix A

5.4.6 Diffusion Lot Number

5.4.7 Wafer Number

5.5 Burn-In Requirement: Burn-In circuit for W16 package:

5.5.1 Burn-In – Run Mode is specified in **Figure 4.**

5.6 Mechanical/Packaging Requirements: Case Outline and Dimensions are in accordance with **Figure 5.**

5.7 Terminal Connections: The terminal connections shall be as specified in **Figure 6.**

5.8 Die Bonding Pad Locations and Electrical Functions: Die layout (X-Y Coordinates) is specified in **Table A**.

5.8.1 Die physical dimensions:

5.8.1.1 Die size: 113 mils x 124 mils

5.8.1.2 Die thickness: 12 mils

5.8.2 Interface materials:

5.8.2.1 Top metallization: Al

5.8.2.2 Backside metallization: (Substrate) Alloyed gold layer

5.8.3 Glassivation:

5.8.3.1 Type: SiO2

5.8.3.2 Thickness: Minimum of 4 kÅ

5.8.4 Substrate: Single crystal silicon

5.8.5 Assembly related information:

5.8.5.1 Substrate potential: GND

5.8.5.2 Die Attach: AuSi 30 x 30 x 2 mils

5.8.5.3 Bond Wire: 1 mil AlSi

5.9 Lead Material and Finish: The lead material and finish shall be Kovar with hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

6.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

6.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Analog Devices is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

6.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with **Table VI** herein.

6.3 Screening: Screening requirements shall be in accordance with **Table VI** herein.

6.3.1

6.4 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

6.4.1 Lot Serial Number Sheets identifying all Canned Sample devices accepted through final inspection by serial number.

6.4.2 100% attributes (completed element evaluation traveler).

6.4.3 Element Evaluation variables data, including Burn-In and Op Life

6.4.4 SEM photographs (3.10 herein)

6.4.5 Wafer Lot Acceptance Report (3.9 herein)

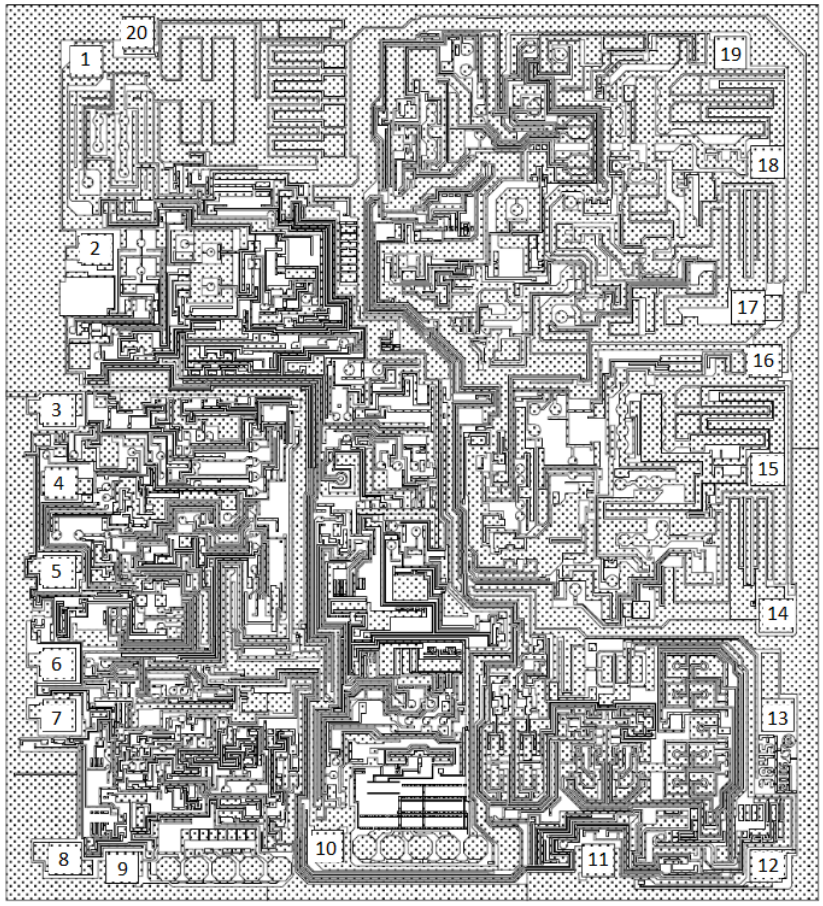
6.4.6 A copy of outside test laboratory radiation report if ordered

6.4.7 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 6. 4.1 and 6. 4.7 will be delivered as a minimum, with each shipment.

7.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All dice shall be packaged in multicavity containers composed of conductive, anti-static, or static dissipative material with an external conductive field shielding barrier.

DICE OUTLINE DIMENSIONS AND PAD FUNCTIONS



1.	V_{IN}	11.	GND
2.	$\overline{SHDN}$	12.	$SENSE^-$
3.	C_{SS}	13.	$SENSE^+$
4.	MODE	14.	PGND
5.	V_{FB}	15.	BG
6.	V_C	16.	V_{CC}
7.	SYNC	17.	SW
8.	f_{SET}	18.	TG
9.	GND	19.	BOOST
10.	GND	20.	GND

113 mils x 124 mils,
Backside Metal: Alloyed Gold Layer
Backside Potential: GND

FIGURE 1

TABLE A: DIE LAYOUT – X-Y COORDINATES

Pad Name	X (µm)	Y (µm)	W (µm)	H (µm)
SYNC	-1205	-897.5	98	98
VC	-1205	-722	98	98
VFB	-1206	-407.5	98	98
MODE	-1199.5	-105	98	98
SS	-1206	142	98	98
SHDN	-1076.5	693	98	98
VIN	-1112.5	1332.5	98	98
GND	-936.5	1431	98	98
BOOST	1085	1364.5	98	98
TG	1213	992	100	98
SW	1146.5	493.5	98	100
VCC	1205	312	98	98
BG	1213	-58	100	98
PGND	1241.5	-555	98	98
SENSE_P	1246	-895	98	98
SENSE_N	1207.5	-1412	98	98
GND	634.5	-1392	98	98
VREF	216	-1347.5	68	68
GND:G	-289	-1343	98	98
GND	-991.5	-1415	98	98
FSET	-1187.5	-1385.5	98	98

Notes:

1. **Origin of coordinates is the centroid of the dice.**

TABLE A

TOTAL DOSE BIAS CIRCUIT

TOTAL DOSE BIAS – RUN MODE:

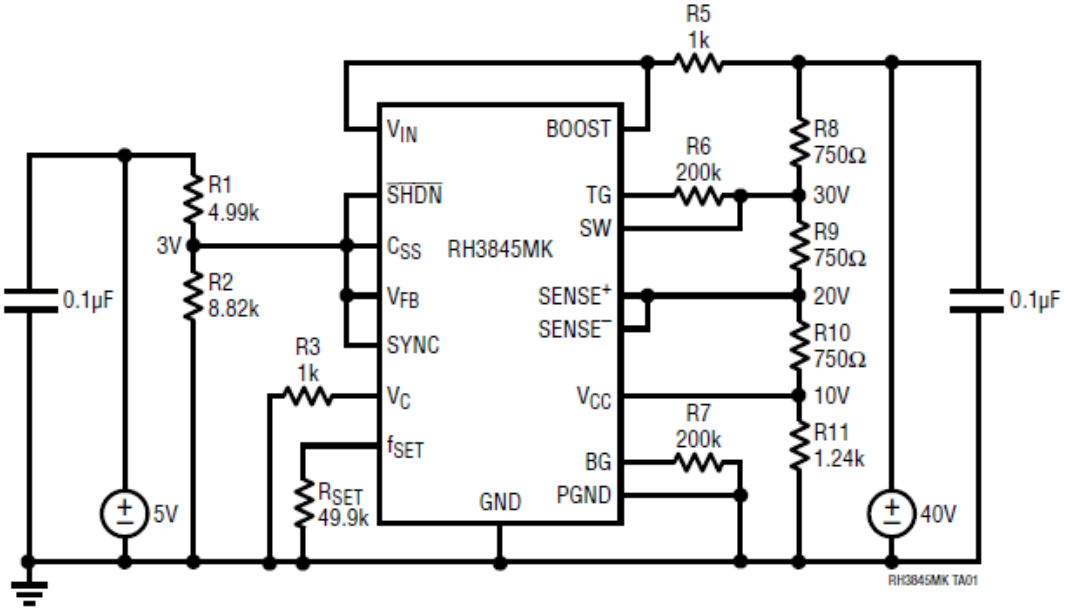


FIGURE 2

TOTAL DOSE BIAS – SHUTDOWN MODE:

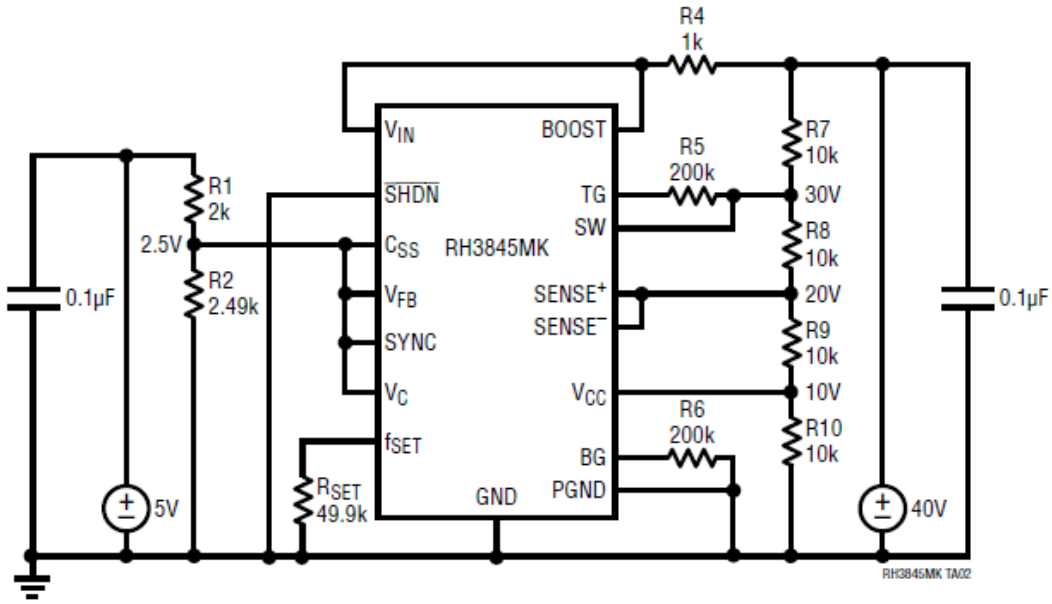


FIGURE 3

BURN-IN CIRCUIT

BURN-IN – RUN MODE:

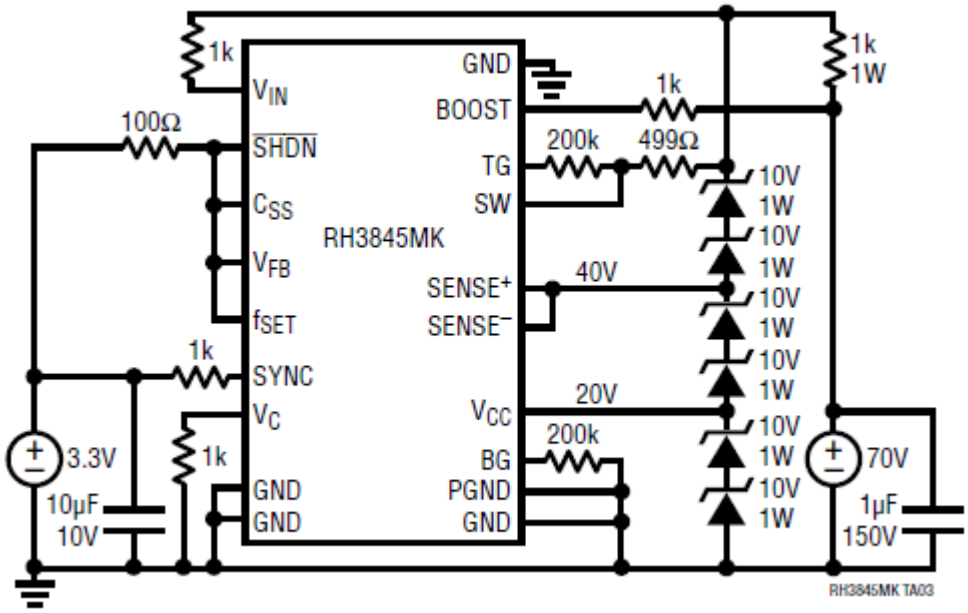
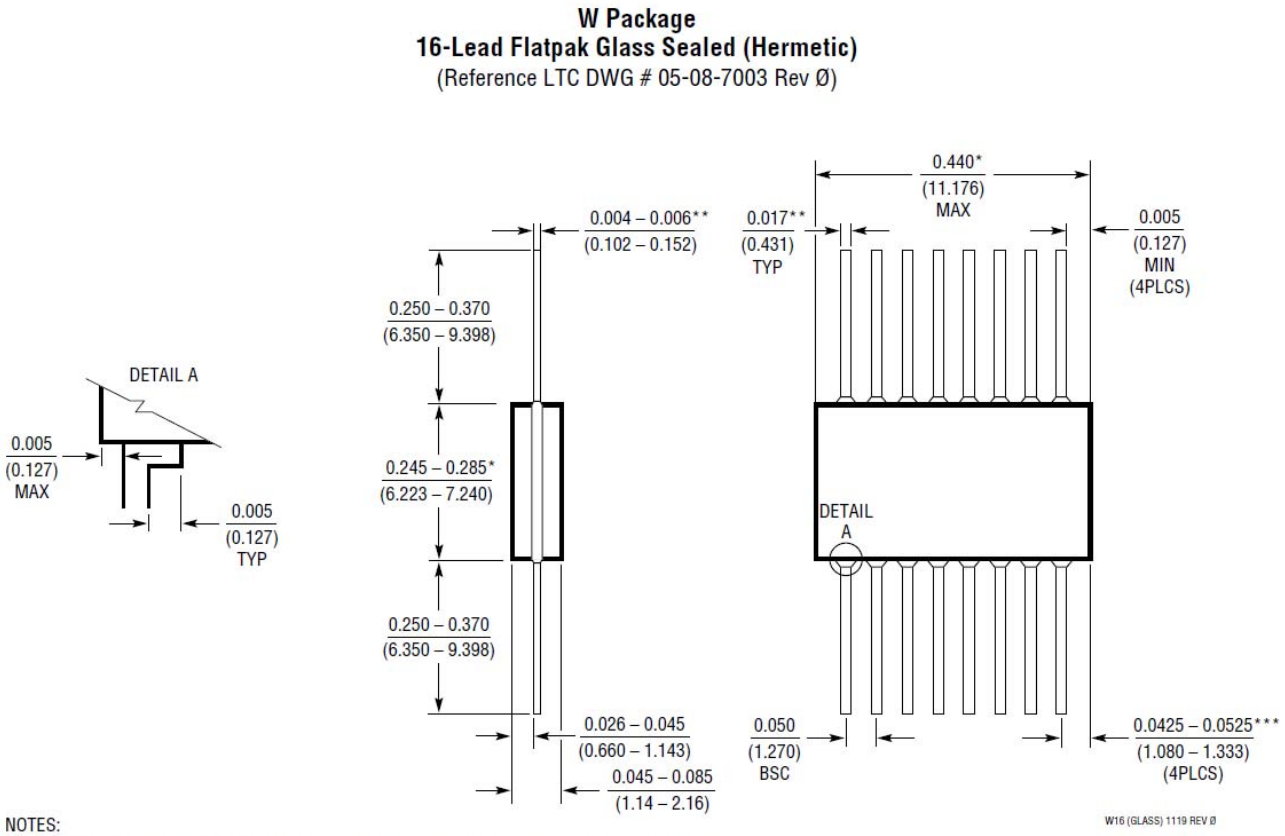


FIGURE 4

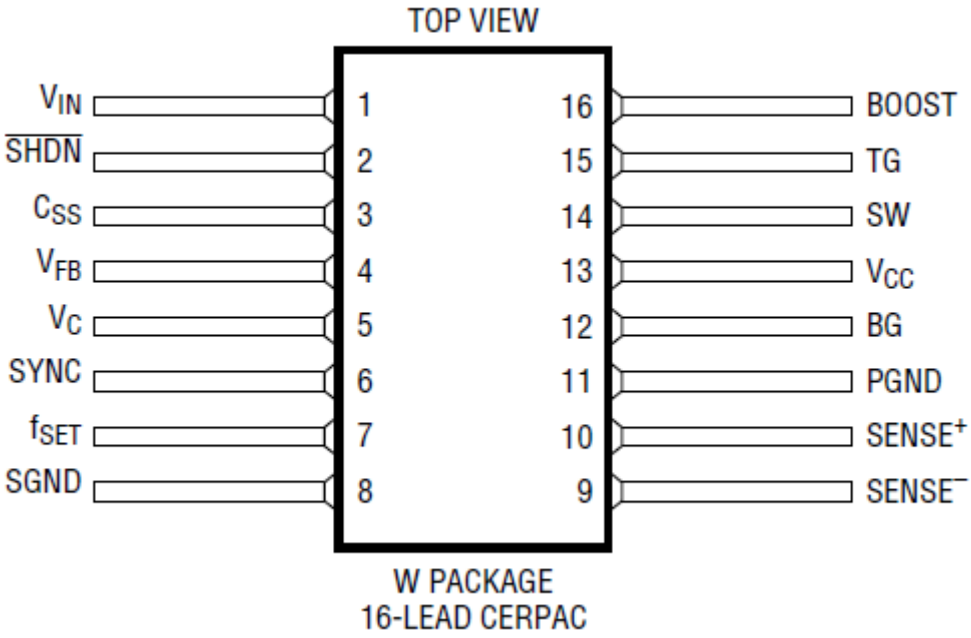
(W) CERPAC / 16 LEADS CASE OUTLINE



NOTES:
*THIS DIMENSION DOES NOT ALLOW FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN
**INCREASE DIMENSIONS BY 0.003 INCHES (0.076mm) WHEN LEAD FINISH A IS APPLIED (SOLDER DIPPED)
***THIS DIMENSION NOT INCLUDE FOR A MAXIMUM 0.020 INCHES (0.508mm) OFF-SET TO CENTER LID

FIGURE 5

TERMINAL CONNECTIONS



W Package, 16-Lead CERPAC

FIGURE 6

TABLE I: DICE ELECTRICAL TEST LIMITS

Specifications are at T_A = 25°C, V_{IN} = 20V,
VCC = BOOST = 10V, SHDN = 2V, RSET = 49.9k, SENSE– = SENSE+ = 10V, SGND = PGND = SW = 0V

PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{IN} Minimum Start Voltage (Note 2)			7.5	V
V_{IN} UVLO Threshold (Falling)		3.6	4.0	V
V_{IN} Supply Current	V_{CC} > 9V		200	µA
V_{IN} Shutdown Current	$V_{\overline{SHDN}}$ = 0.3V		100	µA
BOOST Supply Current (Note 3)			2	mA
V_{CC} Supply Current			4.5	mA
$\overline{SHDN}$ Enable Threshold (Rising)		1.30	1.40	V
Reference Voltage		1.214	1.250	V
V_{FB} Input Bias Current			±100	nA
V_{FB} Error Amp Transconductance		350		µS
Error Amp Sink/Source Current		35		µA
MODE Pin Current (Note 4)			2	µA
Peak Current Limit Sense Voltage		90	120	mV
Soft-Start Charge Current		8	14	µA
Sense Pins Common-Mode Range		0	36	V
Sense Pins Input Current	$V_{SENSE(CM)}$ > 4V		400	µA
Reverse Protect Sense Voltage	V_{MODE} = 7.5V		120	mV
Reverse Current Sense Voltage Offset	V_{MODE} = V_{FB}		20	mV
Switching Frequency	R_T = 49.9k	270	360	kHz
Programmable Frequency Range		100	500	kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability.

Note 2: V_{IN} voltages below the start-up threshold (7.5V) are only supported when the V_{CC} is externally driven above 6.5V.

Note 3: Supply current specification does not include switch drive currents. Actual supply currents will be higher.

Note 4: Connect the MODE pin to V_{FB} for pulse-skipping mode or V_{CC} for forced continuous mode. Burst Mode operation is not available in the RH3845 version of this part. Mode pin functionality is tested only at wafer sort and is not tested individually during die qualification due to using RH3845MW-2, which has mode pin internally bonded to V_{CC} pin. See RH3845MW-1, in the RH3845MW product data sheet, for expected electrical parameters when Mode pin is tied to V_{FB} pin.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. When junction temperature exceed 140°C, nominally, the device will cease operation until temperature decreases. Continuous operation above specified maximum operation temperature may impair device reliability.

TABLE II. ELECTRICAL CHARACTERISTICS

Specifications are at TA = 25°C, VIN = 20V, VCC = BOOST = 10V, SHDN = 2V, RSET = 49.9k, SENSE– = SENSE+ = 10V, SGND = PGND = SW = 0V. (Pre-Irradiation)

PARAMETER	CONDITIONS	SUB-GROUP	T_A = 25°C MIN	TYP	MAX	SUB-GROUP	–55°C ≤ T_A ≥ 125°C MIN	TYP	MAX	UNITS
V_{IN} Minimum Start Voltage (Note 2)		1			7.5	2, 3			7.5	V
V_{IN} UVLO Threshold (Falling)		1	3.6	3.8	4.0	2, 3	3.6	3.8	4.0	V
V_{IN} Supply Current	V_{CC} > 9V	1		130	200	2, 3			800	µA
V_{IN} Shutdown Current	V_{SHDN} = 0.3V	1		65	100	2, 3			200	µA
BOOST Supply Current (Note 3)		1		1.4	2	2, 3			3.5	mA
V_{CC} Supply Current		1		3.8	4.5	2, 3			5.5	mA
V_{CC} Current Limit		1	–40	–150		2, 3	–40			mA
$\overline{SHDN}$ Enable Threshold (Rising)		1	1.30	1.35	1.4	2, 3	1.30		1.5	V
$\overline{SHDN}$ Hysteresis		1		140		2, 3	100		200	mV
Reference Voltage		1	1.222	1.232	1.244	2, 3	1.214		1.250	V
V_{FB} Input Bias Current		1		±20	±150	2, 3		±20		nA
V_{FB} Error Amp Transconductance		1	350	450		2, 3	340		540	µS
Error Amp Sink/Source Current		1	35	50		2, 3	20			µA
Peak Current Limit Sense Voltage		1	90	105	120	2, 3	85		125	mV
Soft-Start Charge Current		1	8	12	14	2, 3	8		16	µA
Sense Pins Common-Mode Range		1	0		36	2, 3	0		36	V
Sense Pins Input Current	$V_{SENSE(CM)}$ > 4V	1		320	400	2, 3			500	µA
Reverse Protect Sense Voltage	V_{MODE} = V_{CC}	1		108	120	2, 3			140	mV
Switching Frequency	R_T = 49.9k	1	270	300	360	2, 3	240		390	kHz
Programmable Frequency Range		1	100		500	2, 3	100		500	kHz
External Sync Frequency Range		1	100		600	2, 3	100		600	kHz
Non-Overlap Time TG to BG		1		250		2, 3				ns
Non-Overlap Time BG to TG		1		250		2, 3				ns
TG Minimum On-Time		1		400		2, 3				ns
TG Minimum Off-Time		1		300		2, 3				ns
TG, BG Drive On Voltage	V_{CC} = 10V	1	8	8.75		2, 3	8			V
TG, BG Drive Off Voltage		1			0.1	2, 3			0.1	V
TG, BG Drive Rise Time	C_{TG} = C_{BG} = 3300pF	1		45		2, 3				ns
TG, BG Drive Fall Time	C_{TG} = C_{BG} = 3300pF	1		45		2, 3				ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability.

Note 2: V_{IN} voltages below the start-up threshold (7.5V) are only supported when the V_{CC} is externally driven above 6.5V.

Note 3: Supply current specification does not include switch drive currents. Actual supply currents will be higher.

Note 4: Connect the MODE pin to V_{FB} for pulse-skipping mode or V_{CC} for forced continuous mode. Burst Mode operation is not available in the RH3845 version of this part. Mode pin functionality is tested only at wafer sort and is not tested individually during die qualification due to using RH3845MW-2, which has mode pin internally bonded to V_{CC} pin. See RH3845MW-1, in the RH3845MW product data sheet, for expected electrical parameters when Mode pin is tied to V_{FB} pin.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. When junction temperature exceed 140°C, nominally, the device will cease operation until temperature decreases. Continuous operation above specified maximum operation temperature may impair device reliability.

TABLE III. ELECTRICAL CHARACTERISTICS

Specifications are at TA = 25°C, VIN = 20V, VCC = BOOST = 10V, SHDN = 2V, RSET = 49.9k, SENSE– = SENSE+ = 10V, SGND = PGND = SW = 0V. (Post-Irradiation)

PARAMETER	CONDITIONS	10KRADS (Si)		20KRADS (Si)		50KRADS (Si)		100KRADS (Si)		200KRADS (Si)		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{IN} Minimum Start Voltage (Note 2)			7.5		7.5		7.5		7.5		7.5	V
V_{IN} UVLO Threshold (Falling)			4		4		4		4		4	V
V_{IN} Supply Current	V_{CC} > 9V		200		200		200		200		200	µA
V_{IN} Shutdown Current	V_{SHDN} = 0.3V		100		100		100		100		100	µA
BOOST Supply Current (Note 3)			2		2		2		2		2	mA
V_{CC} Supply Current			4.5		4.5		4.5		4.5		4.5	mA
V_{CC} Current Limit		–40		–40		–40		–40		–40		mA
$\overline{SHDN}$ Enable Threshold (Rising)		1.30	1.5	1.30	1.5	1.30	1.5	1.30	1.5	1.30	1.5	V
$\overline{SHDN}$ Hysteresis		100	180	100	180	100	180	100	180	80	180	mV
Reference Voltage		1.222	1.244	1.218	1.244	1.216	1.244	1.212	1.244	1.195	1.244	V
V_{FB} Input Bias Current			±150		±200		±250		±350		±400	nA
V_{FB} Error Amp Transconductance		350		330		300		280		250		µS
Error Amp Sink/Source Current		35		35		35		35		30		µA
Peak Current Limit Sense Voltage		90	120	85	120	85	120	80	120	75	120	mV
Soft-Start Charge Current		8	16	8	16	6	16	5	16	4	16	µA
Sense Pins Common-Mode Range			36		36		36		36		36	V
Sense Pins Input Current	$V_{SENSE(CM)}$ > 4V		400		400		400		400		400	µA
Reverse Protect Sense Voltage	V_{MODE} = V_{CC}		120		120		120		120		120	mV
Switching Frequency	R_T = 49.9k	270	370	270	370	270	370	270	370	270	370	kHz
Programmable Frequency Range		100	500	100	500	100	500	100	500	100	500	kHz
TG, BG Drive On Voltage	V_{CC} = 10V	8		8		8		8		8		V
TG, BG Drive Off Voltage			0.1		0.1		0.1		0.1		0.1	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability.

Note 2: V_{IN} voltages below the start-up threshold (7.5V) are only supported when the V_{CC} is externally driven above 6.5V.

Note 3: Supply current specification does not include switch drive currents. Actual supply currents will be higher.

Note 4: Connect the MODE pin to V_{FB} for pulse-skipping mode or V_{CC} for forced continuous mode. Burst Mode operation is not available in the RH3845 version of this part. Mode pin functionality is tested only at wafer sort and is not tested individually during die qualification due to using RH3845MW-2, which has mode pin internally bonded to V_{CC} pin. See RH3845MW-1, in the RH3845MW product data sheet, for expected electrical parameters when Mode pin is tied to V_{FB} pin.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. When junction temperature exceed 140°C, nominally, the device will cease operation until temperature decreases. Continuous operation above specified maximum operation temperature may impair device reliability.

TABLE IV. ELECTRICAL CHARACTERISTICS BURN-IN DELTA PARAMETERS

PARAMETER	CONDITIONS	ENDPOINT LIMITS MIN	ENDPOINT LIMITS MAX	DELTA LIMITS MIN	DELTA LIMITS MAX	UNITS
Reference Voltage	V_{IN} = 20V, V_{CC} = Boost = 10V, SHDN = 2V, R_{SET} = 49.9k, $SENSE^-$ = $SENSE^+$ = 10V, SGND = PGND = SW = 0	1.222	1.244			V
				–3	3	mV

TABLE V. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*, 2, 3
Group A Test Requirements (Method 5005)	1, 2, 3
Group B and D for Class S, End Point Electrical Parameters (Method 5005)	1, 2, 3

*PDA applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.

TABLE VI. RH ELEMENT EVALUATION TABLE FOR QUALIFICATION OF DICE SALE

RH CANNED SAMPLE TABLE FOR QUALIFYING DICE SALES

SUBGROUP	CLASS K/S	CLASS V	CLASS H/B	OPERATION	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	QUANTITY (ACCEPT NUMBER)
1	X	X		SEM	2018	N/A	REF. METHOD 2018 FOR S/S
2	X	X	X	ELEMENT ELECTRICAL (WAFER SORT @ 25ºC)			100%
3	X	X	X	ELEMENT VISUAL (2nd OP)	2010	A	100%
4	X	X	X	INTERNAL VISUAL (3rd OP)	2010	A	ASSEMBLED PARTS ONLY
	X	X		DIE SHEAR MONITOR	2019		
	X	X		BOND PULL MONITOR	2011		
5	X	X		STABILIZATION BAKE	1008	C	ASSEMBLED PARTS ONLY
	X	X		TEMPERATURE CYCLE	1010	C	
	X	X		CONSTANT ACCELERATION	2001	E	
	X	X		FINE LEAK	1014	A	
	X	X		GROSS LEAK	1014	C	
6	X	X		FIRST ROOM ELECTRICAL - READ & RECORD (REPLACE ANY ASSEMBLY-RELATED REJECTS)			45(0)
	X	X		PRE BURN-IN ELECT. READ & RECORD @ +125ºC or +150ºC, -55ºC			
	X	X		BURN-IN: +125ºC/240 hrs. or +150ºC/120 hrs.	1015	+ 125ºc MINIMUM 240 HOURS	
	X	X		POST BURN-IN ELECT. READ & RECORD @ 25ºC			
	X	X		POST BURN-IN ELECT. READ & RECORD @ +125ºC or +150ºC, -55ºC			
		X		TOTAL IRRADIATION DOSE	1019	A	
	X	X		PRE OP-LIFE ELECTRICAL @ 25ºC READ & RECORD			
	X	X		OPERATING LIFE: +125ºC/1000 hrs. or +150ºC/500 hrs.	1005	+ 125ºc MINIMUM 1000 HOURS	
	X	X		POST OP-LIFE ELECT. (R & R @ 25ºC, +125ºC OR +150ºC, -55ºC			
7	X	X	X	WIRE BOND EVALUATION	2011		15(0) OR 25(1) - # of wires

NOTE: LTC is not qualified to process to MIL-PRF-38534. This is an LTC imposed element evaluation that follows MIL-STD-883 test methods and conditions. Please note the quantity and accept number from Sample Size Series of 5%, accept on 0, and note that the actual sample and accept number does not begin until Subgroup 6 OP-LIFE.

NOTE: Tests within Subgroup 5 may be performed in any sequence.

NOTE: LTC's radiation tolerance (RH) die has a topside glassivation thickness of 4KA minimum.

NOTE: Sample sizes on the travelers may be larger than that indicated in the above table; however, the larger sample size is to accommodate extra units for replacement devices in the event of equipment or operator error and for assembly related rejects in Subgroup 6, and for Wire Bond Evaluation, Surgroup 7. The larger sample size is at all times kept segregated and, if used for qualification, has all the required processing imposed.