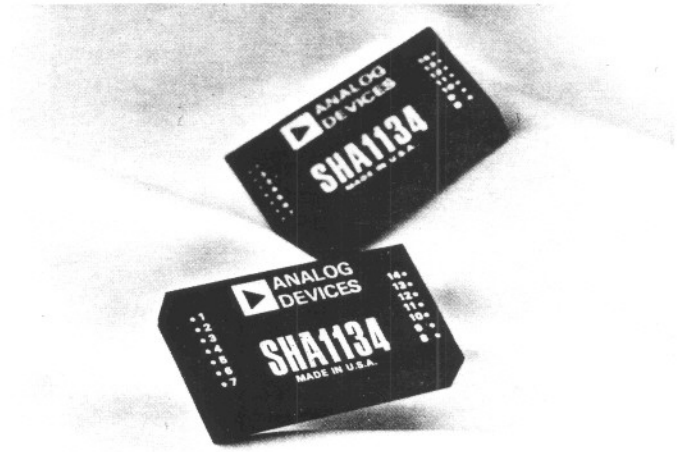


PRELIMINARY TECHNICAL DATA

FEATURES

- 3.4 μ s Acquisition Time
- Short 35ns Aperture Delay
- $\pm 0.005\%$ Maximum Linearity Error
- High Input Impedance: $> 10^7 \Omega$
- DTL/TTL Compatible
- Compact Module: 1 1/8" x 2" x 0.4" (29 x 51 x 10mm)



OBSOLETE

GENERAL DESCRIPTION

The SHA1134 is a moderately fast, general purpose sample-and-hold amplifier which has been optimized for use in data acquisition applications with 12-bit analog-to-digital converters. When in the "sample" mode, the module appears as a fast amplifier with a 3.2 μ s settling time to $\pm 0.01\%$ accuracy. When switched to the "hold" mode, the output is held at a level corresponding to the input signal voltage at the instant of switching. The operating mode of the SHA1134 is controlled by a TTL/DTL compatible logic input.

The SHA1134 features an aperture delay time of 35ns and an aperture delay time uncertainty, or "jitter", of 2ns. The droop rate of 50mV/s makes it suitable for operation with virtually all successive approximation A/D converters. Package size for this compact module is 1.12" x 2" x 0.4" (29 x 51 x 10mm). It needs no adjustments and requires only $\pm 15V$ external power for operation.

PRINCIPLE OF OPERATION

The SHA1134 consists basically of two high speed operational amplifiers, a storage capacitor, and a digitally controlled switch connected in a feedback loop as shown below.

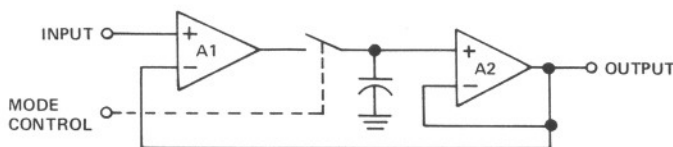


Figure 1. SHA1134 Basic Configuration

When the mode control input is shifted to logic "1", the switch closes, causing the capacitor voltage and output voltage to match the input voltage. In addition to providing input buffering, amplifier A1 supplies the current needed to quickly charge the storage capacitor in this mode of operation. The high gain feedback loop contributes to high tracking accuracy.

When the mode control is shifted back to logic "0", the switch opens and the output remains fixed at a voltage equal to the voltage "stored" across the capacitor. The low input current of amplifier A2 and the low "off" leakage current of the field-effect-transistor switch minimize the leakage of the capacitor's charge and, thus, the "droop" in the output voltage. Amplifier A2 provides the SHA1134 with low output impedance and good current drive capability.

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SPECIFICATIONS

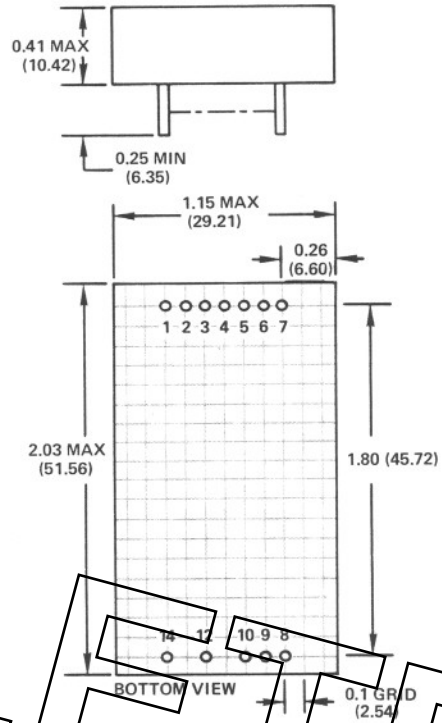
(typical @ +25°C and ±15V, unless otherwise noted)

MODEL	SHA1134
ACCURACY	
Gain	+1
Gain Error	±0.036% (0.04% max)
Gain Temperature Coefficient	6.5ppm/°C (10ppm/°C max)
Gain Nonlinearity	±0.001% (±0.005% max)
STATIC INPUT CHARACTERISTICS	
Voltage Range for Rated Accuracy	±10V max
Impedance	>10 ⁷ Ω
Bias Current	0.5μA max
Input Offset Voltage	0.5mV (1.5mV max)
Temperature Coefficient	135μV/°C (200μV/°C max)
Supply Coefficient	20μV/%ΔV _S (30μV/%ΔV _S)
OUTPUT CHARACTERISTICS	
Voltage	±10V
Current	±5mA max
Resistance	0.05Ω
Capacitive Load	100pF max
Noise @ 100kHz Bandwidth	0.3mV (0.5mV max)
@ 1MHz Bandwidth	1.8mV (2.2mV max)
SAMPLE MODE DYNAMICS	
Frequency Response	
Small Signal (-3dB)	800kHz
Full Power	600kHz
Slew Rate	15V/μs
Settling Time to ±0.01% (20V Step)	3.2μs (4.0μs max)
Overload Recovery (50% Overload)	0.6μs (1μs max)
SAMPLE-TO-HOLD SWITCHING	
Aperture Delay Time	35ns (50ns max)
Aperture Uncertainty	2ns (5ns max)
Offset Step	3.3mV (5.5mV max)
Offset Linearity	±3mV
Switching Transient	
Amplitude	±70mV
Settling Time to ±0.01%	1μs
HOLD MODE DYNAMICS	
Droop Rate	±50mV/s (±200mV/s max)
Variation with Temperature	Doubles Every 10°C
Feedthrough (for ±10V Input @ 1kHz)	1.0mV (2.0mV max)
HOLD-TO-SAMPLE SWITCHING	
Acquisition Time to ±0.01%	3.4μs (4.1μs max)
DIGITAL INPUT	
Sample Mode (Logic "1")	+2V ≤ LOGIC "1" ≤ +5.5V @ 15nA max
Hold Mode (Logic "0")	0V ≤ LOGIC "0" ≤ +0.8V @ 5μA (20μA max)
POWER REQUIRED	
	+15V ±3% @ +20mA
	-15V ±3% @ -17mA
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55 to +85°C
PRICE (1-9)	
	\$99
(100+)	
	\$75

B S O L E

OUTLINE DIMENSIONS and PIN CONNECTIONS

Dimensions shown in inches and (mm).



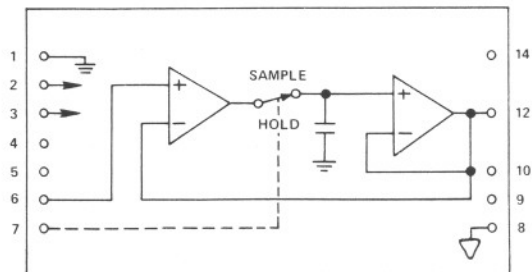
NOTES:

1. Pins: 0.019 ± 0.001 (0.48mm ± 0.02mm) dia. half-hard brass/gold plated per MIL-G-45204B, Class I, Type II.
2. Mating socket AC4102 @ \$15, or pin sockets P/N 2-330808-8 (7 required). \$20 ea.

PIN DESIGNATIONS

- | | |
|------------------|-------------------|
| 1. ANALOG GROUND | 8. LOGIC GROUND |
| 2. -15V | 9. N.C. |
| 3. +15V | 10. N.C. |
| 4. N.C. | 11. NO PIN |
| 5. N.C. | 12. ANALOG OUTPUT |
| 6. SIGNAL IN | 13. NO PIN |
| 7. CONTROL IN | 14. N.C. |

BLOCK DIAGRAM



DATA ACQUISITION APPLICATION

Successive-approximation A/D converters can generate substantial linearity errors if the analog input varies during the period of conversion; even the fastest 12-bit models available cannot tolerate input signal frequencies of greater than 10Hz. For this reason, sample-and-hold amplifiers like the SHA1134 are often connected between the A/D and its signal source to hold the analog input constant during conversion.

When the SHA1134 is connected to an A/D, its aperture time uncertainty, rather than the A/D's conversion time, is the factor which limits the allowable input signal slew rate. The SHA1134, with a typical aperture delay time of 35ns and an uncertainty of 2ns, will change from the sample mode to the hold mode 33 to 35ns after the "1" to "0" transition of the mode control input. If the system timing is so arranged as to initiate the mode control signal 33ns early, then switching will actually occur within 2ns of the desired time as shown below.

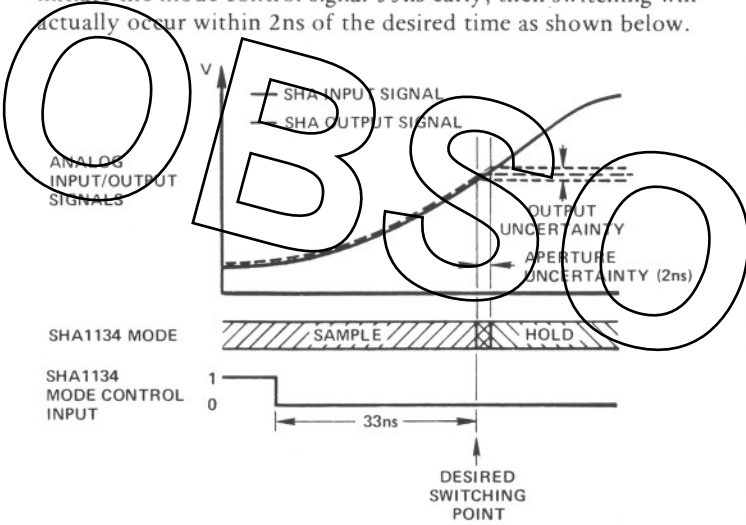


Figure 2. Aperture Uncertainty

The maximum allowable slew rate will thus equal the quotient of the maximum allowable voltage uncertainty and the 2ns aperture uncertainty. For sinewave inputs, the corresponding maximum frequency is expressed by:

$$f_{\max} = \left(\frac{\Delta E}{E_{FS}}\right) \left(\frac{1}{2\pi\Delta t}\right) \cong 8 \times 10^7 \left(\frac{\Delta E}{E_{FS}}\right)$$

where: ΔE = the allowable voltage uncertainty

E_{FS} = the sinewave magnitude

For a system containing a SHA1134 and a 12-bit A/D with $\pm 10V$ input signals and an allowable input uncertainty of $\pm 1/2$ LSB ($\pm 2.44mV$), the maximum allowable slew rate will be $\pm 1.22V/\mu s$. This corresponds to the maximum rate of change of a 19.5kHz sinewave signal.

OPERATION WITH AN A/D CONVERTER

Figure 3 below shows the appropriate connections between the SHA1134 and a successive approximation A/D converter in block diagram form.

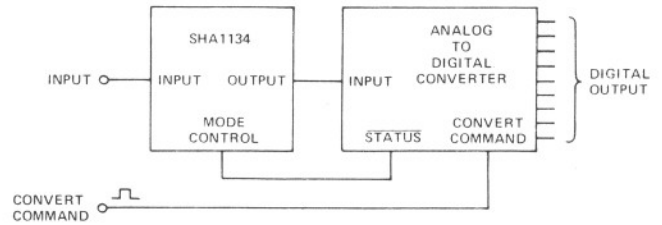


Figure 3. SHA1134 and A/D Connections

The resulting timing sequence at the start of conversion is illustrated in Figure 4.

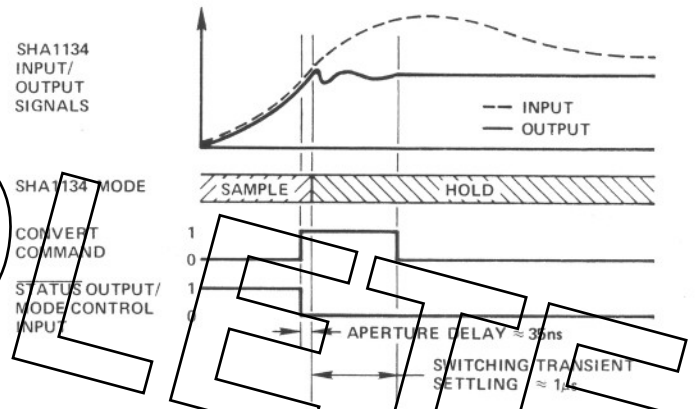


Figure 4. A/D and SHA Timing at Start of Conversion

Note that the leading edge of the convert command pulse causes the converter's STATUS output to go to logic "0" which in turn switches the SHA1134 from sample to hold. As discussed previously, the typical SHA1134 actually changes modes 33 to 35ns after the "1" to "0" transition of the mode control input. This mode switching causes a transient on the output terminal which decays to within 0.01% of the final value in approximately 1µs. Once the transient has settled, the convert command input is returned to logic "0" and the conversion proceeds. As shown in Figure 5, the STATUS signal returns to logic "1" and the SHA1134 returns to the sample mode at the end of conversion. Within 3.4µs, it will have acquired the input signal to 0.01% accuracy and a new conversion cycle may be started.

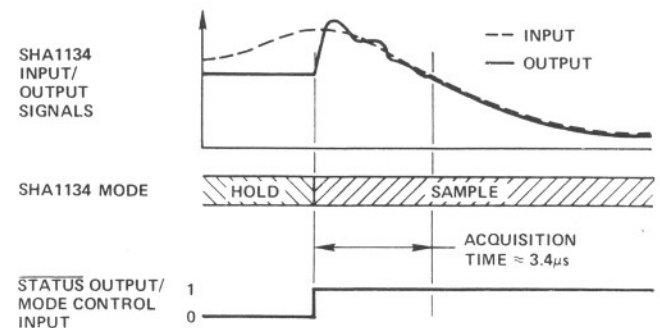


Figure 5. A/D and SHA Timing at End of Conversion

OPERATION WITH AN A/D AND MULTIPLEXER

The subsystem of Figure 3 may also be connected to a multiplexer like Analog Devices' model MPX-8A as shown below:

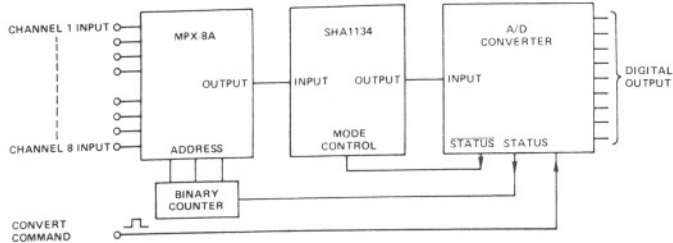


Figure 6. A/D, SHA, and MPX Connections

The leading edge of the convert command pulse sets the STATUS output to logic "0" thereby switching the SHA1134 to "hold"; the corresponding change to logic "1" of the STATUS output increments the binary counter and changes the multiplexer address. Since the SHA1134's aperture time is small with respect to the multiplexer switching time, it will have switched to the hold mode before the MPX-8A actually changes channels. The multiplexer switching transients will settle out long before the SHA returns to "sample" at the end of conversion. The timing sequence described above is illustrated in Figure 7.

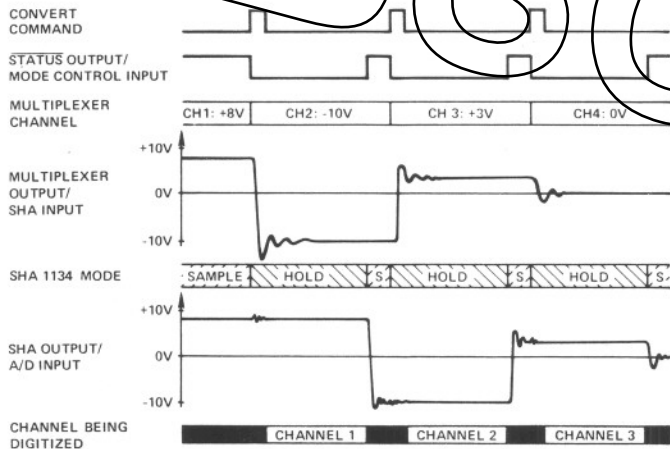


Figure 7. A/D, SHA, and MPX Timing

This method of sequencing the multiplexer may be altered to permit random addressing or addressing in a preset pattern. The timing of multiplexer address changes may also be altered but consideration should be given to the effects of feedthrough in the SHA1134. Feedthrough is the coupling of analog input signals to the output terminal while the SHA is in "hold". For the SHA1134, a 20V p-p input signal will typically produce a 1mV signal at the output. If large multiplexer switching transients occur while the A/D conversion is in progress, errors can be introduced.

THROUGHPUT RATE

The rate at which the systems of Figures 3 and 6 can perform conversions will, of course, depend on the conversion time of the A/D converter used. The table below lists the minimum system throughput rates achievable with several of Analog Devices' 12-bit successive approximation A/D converters.

A/D CONVERTER	MINIMUM SYSTEM THROUGHPUT RATE
ADC12QZ	22.1kHz
ADC12QM	33.1kHz
ADC12QU	49.6kHz
ADC1102	74.0kHz
ADC1103-003	115.6kHz

POWER SUPPLY AND GROUNDING CONNECTIONS

The proper power supply and grounding connections are shown below in Figure 8.

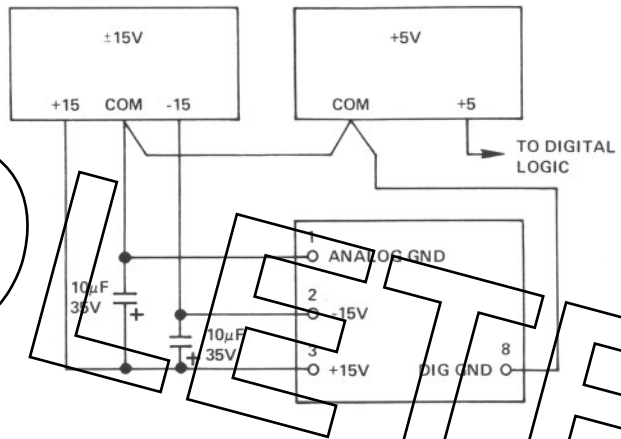


Figure 8. Power Supply and Grounding Connections

The ±15V power supplies must be externally bypassed as shown. The capacitors should be tantalum types and should be installed as close to the module pins as possible. The analog and digital ground lines should be run separately to their respective power supply commons to prevent coupling of digital switching noise to the sensitive analog circuit section.