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### Evaluating the SSM4567 Digital 2.5 W, 5.1 V, Boost Class-D Audio Amplifier

#### **FEATURES**

I<sup>2</sup>S/PDM/TDM/optical digital audio input Full featured evaluation board for the SSM4567 PCB footprint for optional EMI filter Includes the EVAL-ADUSB2EBZ USB hardware interface for plug-and-play operation Microsoft Windows-based evaluation software with simple graphical user interface

#### EQUIPMENT REQUIRED

Audio source with optical fiber or 10-pin 0.100" digital audio header Power supply (5.0 V, 2.0 A recommended) EVAL-SSM4567Z evaluation board USB-to-I<sup>2</sup>C adapter dongle, EVAL-ADUSB2EBZ PC running Windows XP or later; USB 2.0 port required Speaker or other load

#### **DOCUMENTS REQUIRED**

SSM4567 data sheet

#### **OPTIONAL SOFTWARE**

SigmaStudio software

#### **GENERAL DESCRIPTION**

The SSM4567 evaluation board is a complete solution for driving loudspeakers with boosted battery power supply as well as sense output current, output voltage, and the VBAT supply voltage. It includes the SSM4567 amplifier IC and the additional components needed to connect the digital audio input and optical fiber.

The SSM4567 combines an audio digital-to-analog converter (DAC), a power amplifier, and PDM or PCM (I<sup>2</sup>S/TDM) digital audio interfaces on a single chip. Using the SSM4567, audio can be transmitted digitally to the audio amplifier, significantly reducing the effect of noise sources on the transmitted audio and eliminating the need for input coupling capacitors. The SSM4567 is capable of delivering 2.5 W of continuous output power with <1% THD + N driving a 4  $\Omega$  load from a 3.6 V supply.

The SSM4567 can be controlled by I<sup>2</sup>C, PDM pattern control, or TDM control. It can also operate in standalone mode without a control interface.

The SSM4567 includes circuitry to sense output current, output voltage, and the VBAT supply voltage. Current sense is performed using an on-chip sense resistor that is connected between an output pin and the load. Output current and voltage are sent to ADCs. The output of these ADCs are available on the digital serial output port. The VBAT supply voltage can be used with an automatic gain control circuit that is fully configurable. This AGC can limit the maximum output at low battery voltages to avoid current that is too high off the battery.

This user guide describes how to use the EVAL-SSM4567Z to test the features of the SSM4567 amplifier. It describes the hardware and software of the SSM4567 evaluation board, including detailed schematics and PCB layout artwork.

The SSM4567 data sheet provides detailed information about the specifications, internal block diagrams, and application guidance for the amplifier IC.

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6/14—Revision 0: Initial Version

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### **EVALUATION BOARD OVERVIEW**

The SSM4567 evaluation board provides all of the support circuitry required to operate the SSM4567 amplifier. Figure 1 shows an overview while Figure 2 shows the typical bench characterization setup used to evaluate the audio performance of the SSM4567. See the Evaluation Board Software Quick Start Procedures section to get started.



Figure 1. Evaluation Board Overview



Figure 2. Default Quick Start Setup

### EVALUATION BOARD HARDWARE POWER SUPPLIES

The SSM4567 requires two power supplies, VBAT and IOVDD. VBAT voltages can be between 2.5 V and 5.0 V. The IOVDD power supply must be 1.8 V. The EVAL-SSM4567Z has three external dc power supply connections: VBAT (J3), VDD\_REG (J2), and EXT\_IOVDD (J5). The EVAL-SSM4567Z has voltage regulators on the board that can be isolated or bypassed to allow for current measurements only for the SSM4567. Note that VBAT supply currents may exceed 2 A, depending on supply voltage and load impedance.

The VBAT input can be configured to supply all the voltages required for the evaluation board to function.

VDD\_REG is used to provide on-board 3.3 V and 1.8 V power supply by LDOs (ADP1711). It can share the input with VBAT by shorting J23, but VBAT must be higher than 3.5 V. If VBAT input is lower than 3.5 V, VDD\_REG should be provided independently and be between 3.5 V and 5.0 V. The 1.8 V output from the on-board LDO can supply IOVDD for the SSM4567 or the EXT\_IOVDD terminal, J5, can supply IOVDD. J8 is used to select between the internal LDO or the external terminal J5.

Note that the 3.3 V regulator is used to supply power to the SPDIF input circuitry. There are on-board level shifters to translate the signals to 1.8 V levels.



Figure 3. Power Input Terminals and Default Jumper Settings. VBAT Only Using Internal Regulators for IOVDD and 3.3 V.

#### **INPUT SIGNALS**

On the right side of the PCB are two 10-pin headers: J25 and J26. One header is used to connect the digital input audio signals to the amplifier and the other can be used to connect to other EVAL-SSM4567Z boards to enable the testing of multichip mode. The two connectors are wired together in parallel so that they can be used interchangeably (see Figure 4).



Figure 4. Jumper Configuration for Clock and Data Input from J25 and J26

For a direct connection from an external circuit using the I<sup>2</sup>S headers, J25 and J26, the logic level inputs are at 1.8 V. A level shifter is required at the sending circuit for these inputs to operate at a different level.

The EVAL-SSM4567Z board also supports I<sup>2</sup>S input from an optical fiber port using the SPDIF format. The jumpers on J16 select the digital input from either the internal SPDIF interface or the external I<sup>2</sup>S signals from J25/J26 (see Figure 5).



Figure 5. Jumper Configuration for Clock and Data Input from the SPDIF Receiver

#### AUDIO AMPLIFIER OUTPUT SIGNAL

The amplifier output is available at two 2-pin 0.100" headers: J10 and J11. The speaker is connected in bridge-tied load (BTL) configuration, and the output pins are labeled with their polarity. For example, OUTP indicates the noninverting terminal (see Figure 6).

Figure 6. Amplifier Output Connectors

In the standard filterless configuration, the two headers are connected with 0  $\Omega$  links on the pads marked FB5 and FB6. In this case, the two headers are tied together and can be used interchangeably as attachment points for the load and an audio analyzer. The EMI filtering is not populated on the EVAL-SSM4567Z evaluation board to allow proper measurement of key parameters, such as SNR and THD.

A ferrite bead-based EMI filter can be implemented using FB5 and FB6 with C26 and C27 footprints. If this filtering is used, only J11 connects at the proper location with respect to the filter components—the load must be connected to this header. Measurements of the unfiltered waveform can be taken at J10.

Note that measuring of Class-D amplifier outputs with standard audio test equipment does not yield proper results. Switching amplifier filters, such as the Audio Precision AUX-0025 or the AUX-0100, filters the amplifier output and allows the proper measurement of the amplifier.

#### SENSE OUTPUT SIGNALS

The SSM4567 can output voltage, current, and battery level sensing data of the Class-D amplifier via I<sup>2</sup>S/PDM/TDM format. The output data is available (SDATAO) on J25 and J26. The logic level outputs on J25 and J26 are at a 1.8 V level so a level shifter is required at the receiving circuit.

There is an on-board level shifting circuit for the SDATAO signal. The level can be 3.3 V originating from the internal 3.3 V regulator or an external source can feed the level translator. J19 selects the level between the internal 3.3 V or an external level can be injected using Pin 2 of J19. Note that Pin 3 of J19 is not connected to any signals on the board (NC).

The input of the level shifter is selected using J29. Installing a jumper on Pin 1 and Pin 2 connects the SDATAO signal to the level shifter. The output of the level shifter appears on J15. Pin 1 is the shifted SDATAO signal and Pin 2 is ground. When not using the level shifter, it is recommended that the input be grounded by inserting a jumper between Pin 2 and Pin 3 of J29 (see Figure 7).



Figure 7. SDATAO Jumpers and Connections Mode Selection Pins

The SSM4567 can operate in many different modes based on the state of several multifunction pins. The EVAL-SSM4567Z board has the capability to set the pins to different levels thereby changing the operating mode of the SSM4567.

#### Table 1. Mode Pin Header Descriptions

| Mode Pin Header | Description         |
|-----------------|---------------------|
| J12             | SEL Pin             |
| J9              | LR_SEL/ADDR Pin     |
| J20             | SCL Pin             |
| J21             | SDA Pin             |
| J13             | 47 kΩ bypass jumper |

The settings for these pins on the evaluation board are labeled as low or high where low = ground and high = IOVDD. The LR\_SEL/ADDR Pin has five functions so it needs to be able to be set at five different levels: ground, IOVDD, floating, pulled up to IOVDD, or pulled down to ground via a 47 K $\Omega$  resistor. This is where J13 can bypass the resistor to allow the pin to be pulled high or low. When J13 is removed, the pin is pulled up or down through R22.

Jumper J20 and Jumper J21 are on the SDA and SCL pins. To communicate with the SSM4567 via I<sup>2</sup>C, these jumpers must be removed. These jumpers are for options when operating the part in standalone modes where communication with the part is not required.

The following sections detail the use of these jumpers. See Figure 8 for the jumper locations.



Figure 8. Mode Selection Jumper Locations

#### PDM CONTROL MODE

The SSM4567 can boot up in PDM control mode. Powering up, or resetting, the part while the SEL pin, J12, is tied low places the part in PDM audio and pattern control mode. In this mode, several functions are controlled via PDM pattern control. I<sup>2</sup>C remains available, but registers that are controlled via PDM do not respond to I<sup>2</sup>C control and the proper state of the part is not reflected when the registers are read. For full I<sup>2</sup>C control, SEL, J12, must be tied high, then placed into PDM mode using I<sup>2</sup>C writes. Refer to the SSM4567 data sheet for more details.

#### PDM CHANNEL SELECTION

The SSM4567 includes a left/right input select pin, LR\_SEL/ADDR, J9 is used to determine which of the timemultiplexed input streams is routed to the amplifier when using PDM pattern control mode. The connection to this pin is via the jumpers labeled ADDR on the EVAL-SSM4567Z board. To select the left input channel, connect LR\_SEL/ADDR low. To select the right channel data, connect LR\_SEL/ADDR to high. At any point during amplifier operation, the logic level applied to LR\_SEL/ADDR may be changed and the output switches between input streams without audible artifacts. Aside from your logic level selection, no muting, watermarking pattern, or synchronizing are necessary to achieve a click/pop free LR\_SEL/ADDR transition.

#### Table 2. LR\_SEL/ADDR Function Descriptions

| Device Setting       | LR_SEL/ADDR Pin Configuration |
|----------------------|-------------------------------|
| Right Channel Select | High (IOVDD)                  |
| Left Channel Select  | Low (GND)                     |

#### Table 3. PCM Mode Pin Setup

#### PCM MODE PIN SETUP AND CONTROL

When the SEL pin is tied to IOVDD, the SSM4567 is set for PCM mode operation. In this mode, the SSM4567 supports standalone operation, I<sup>2</sup>C control, or control using commands sent over the input serial audio/TDM interface. See Figure 9 for the location of J14, the serial port, and the jumpers associated with the port. Note that the J20 and J21 jumpers must be removed when I<sup>2</sup>C communication to the part is desired.



Figure 9. Serial Port and Jumper Location

When the LR\_SEL/ADDR pin is pulled up via a 47 k $\Omega$  resister (J9 set high and J13 removed), the IC operates in a standalone mode with most registers set to their default states.

The state of these several pins can change the functionality of other pins. The LR\_SEL/ADDR pin determines the I<sup>2</sup>C device address. In standalone and TDM control modes, the SCL and SDA pins are used to determine the TDM slot used (J20 and J21). For details, see the data sheet or refer to Table 3.

| LR_SEL/ADDR | SCL                              | SDA                   | Control Mode                            | I <sup>2</sup> C Control Address | TDM Slot |
|-------------|----------------------------------|-----------------------|---|----------------------------------|----------|
| STANDALONE  | SCL                              | SDA                   | I <sup>2</sup> C                        | 0                                | 1        |
| IOVDD       | SCL                              | SDA                   | I <sup>2</sup> C                        | 1                                | 2        |
| Open        | SCL                              | SDA                   | I <sup>2</sup> C                        | 2                                | 3        |
| Pull-Up     | 0                                | 0                     | Standalone (TDM interface)              | NA                               | 1        |
| Pull-Up     | 0                                | 1                     | Standalone (TDM interface)              | NA                               | 2        |
| Pull-Up     | 1                                | 0                     | Standalone (TDM interface)              | NA                               | 3        |
| Pull-Up     | 1                                | 1                     | Standalone (TDM interface)              | NA                               | 4        |
| Pull-Up     | Boost power down<br>(active low) | Shutdown (active low) | Standalone (l <sup>2</sup> S interface) | NA                               | NA       |
| Pull-Down   | 0                                | 0                     | TDM                                     | NA                               | 1        |
| Pull-Down   | 0                                | 1                     | TDM                                     | NA                               | 2        |
| Pull-Down   | 1                                | 0                     | TDM                                     | NA                               | 3        |
| Pull-Down   | 1                                | 1                     | TDM                                     | NA                               | 4        |

# EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

#### HARDWARE ONLY QUICK START

The evaluation board comes configured for single 3.5 V to 5 V dc input, 48 kHz optical SPDIF input, and standalone operation mode of the SSM4567. To operate the board with this quick start configuration

- 1. Connect power to J3 and J4.
- 2. Connect the speaker load to J11.
- 3. Connect the optical SPDIF cable to the optical jack.
- 4. Apply power to the evaluation board.
- 5. Start the SPDIF digital audio stream.
- 6. Press the SPDIF reset switch, S1.

See Figure 2 for the jumper settings.

#### SSM4567 CONTROL SOFTWARE SETUP

Do not connect the USBi (EVAL-ADUSB2EBZ) to the computer until the software is installed. The SSM4567 software interface (SigmaStudio<sup>™</sup>) requires Microsoft<sup>®</sup> .NET Framework (Version 2.0 or later). The installer automatically downloads it if .NET Version 2.0 is not previously installed.

A graphical user interface for the SSM4567 has been created in the Analog Devices, Inc., SigmaStudio environment. SigmaStudio must first be downloaded and installed on your PC.

#### SSM4567 USB DRIVER INSTALLATION

Before connecting the USBi (EVAL-ADUSB2EBZ) evaluation board to a PC or notebook, the following procedure may need to be completed. (This procedure only needs to be executed once on each computer that uses the SSM4567 software. Skip this procedure if you previously installed any SigmaStudio or USBi related drivers from Analog Devices.)

Ensure that the Cypress (CYUSB) USB driver is installed during the SigmaStudio installation. If you need to verify installation, you can find the driver on your computer in this location:

#### C:\Program Files\Analog Devices\SigmaStudio x.x\USB drivers\x86 (or x64)\dpinst.exe

Note that the parentheses indicate alternate folder names depending on your hardware. In addition, x.x refers to the version of SigmaStudio installed.



Figure 10. Device Driver Installation Wizard

#### INITIAL SSM4567 HARDWARE SETUP

To allow the SSM4567 software to control the SSM4567 evaluation board, make a few simple jumper connections as follows:

- Connect the SEL to HIGH (J12) and ADDR to LOW (J9), and short R22 (install J13). The purpose of this is to set the SSM4567 to work under I<sup>2</sup>C control mode.
- 2. Remove any jumpers on J20 and J21.
- 3. Install jumpers on J16 to select the digital audio input to the SSM4567 from either an external source or the SPDIF input. The SPDIF input signals are labeled as INT (internal). See Figure 4 or Figure 5 for details.

#### SOFTWARE INSTRUCTIONS

Complete the following instructions after SigmaStudio and the USBi driver installation.

- 1. Connect the EVAL-ADUSB2EBZ to your PC using the USB cable.
- 2. Launch SigmaStudio on the PC.
- 3. Click **File>New Project** to start a new GUI project file, and then find **USBi** under **Communication Channels**.



4. Drag and drop **USBi** to the **Hardware Configuration**.



Figure 12. Project with the USBi GUI Inserted

If SigmaStudio cannot detect the USBi on the USB port of the computer, then the background of the USB label is red. This may happen when the USBi is not connected or when the drivers are incorrectly installed.

| US | SB            |   |   |
|----|---------------|---|---|
|    |               | Ŧ | • |
|    |               | - | • |
|    |               | Ŧ | • |
|    |               | Ŧ | • |
|    |               | Ŧ | • |
|    | USB Interface |   | _ |

Figure 13. USBi GUI when USBi Hardware is Not Found

If SigmaStudio detects the USBi on the USB port of the computer, the background of the USB label changes to orange.

| US | B             |   | ٦ |
|----|---------------|---|---|
|    |               | - | • |
|    |               | - | • |
|    |               | - | • |
|    |               | Ŧ | • |
|    |               | - | • |
|    | USB Interface |   | 1 |

Figure 14. USBi GUI when USBi Hardware is Located

- 5. After launching SigmaStudio, follow this sequence to initiate the SSM4567 GUI:
  - a. Copy the SSM4567.dll to C:\Program Files\Analog Devices\SigmaStudio 3.7.
  - b. From the main SigmaStudio window, click Tools>Add-Ins Browser...>Add Dll and browse to locate the SSM4567.dll you copied to in Step 5a and then click Save. This loads the SSM4567 as a processor in SigmaStudio.

| 🖳 AddIns             |                   |   |
|----------------------|-------------------|---|
| File                 | Click here to add |   |
|                      | SSM4567.dll       |   |
| V . ADICtris.dli     |                   | - |
| Sigma100.dll         |                   | 1 |
| Sigma200.dll         |                   |   |
| VADAV451.dll         |                   |   |
| VADAV4xxx.dll        |                   |   |
| VADAU176X.dll        |                   |   |
| VADAU136X.dll        | E                 | 1 |
| ✓ .\SigmaLP2.dll     |                   |   |
| WindNoise.dll        |                   |   |
| VDSC.dll             |                   |   |
| SubHarmonic.dll      |                   |   |
| VAVC.dll             |                   | 1 |
| .\NoiseReduction.dll |                   |   |
| SuperBass.dll        |                   |   |
| V.SSM2518.dll        |                   |   |
| VADAU1772.dll        |                   | r |
|                      |                   |   |

Figure 15. Adding a Processor DLL Using the AddIns Tool

c. From the main SigmaStudio window, click **File>New Project** to start a new GUI project file.

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d. Drag **USBi** and <u>SSM4567</u> from the tree toolbox to the **Hardware Configuration** window, and connect one blue pin of USBi to the green pin of the <u>SSM4567</u> by clicking and dragging a wire as shown in Figure 16.



Figure 16. USBi to SSM4567 Communications Connection

e. Click the **IC 1–SSM4567 v1.8** tab from the **Hardware Configuration** tab to open the SSM4567 GUI.

2378-013

| Analog Devices - SigmaStudio - [*Design 1]       |                           |                |                             |            |  |   |
|--|---------------------------|----------------|-----------------------------|------------|--|---|
| 🖉 File Edit View Tools Format Action Window Help |                           |                |                             |            |  |   |
| 👒 🔗 🏉 🔜 🕺 🖕 🖄 💁 🖉 🖉                              |                           | êr i 🦧 🦓 😽     | } _4 <sup>2</sup> i  fs- 48 | kHz 💌 🥳    |  |   |
| 2월 음 마 음 읍 ጥ 🗤 💂 🔝 💷 💷                           | + -                       | × .            |                             |            |  |   |
| Hardware Configuration                           |                           |                |                             |            |  |   |
| Write All Read All Import Expo                   | xt                        |                |                             |            |  |   |
| Chip Control SAI PDM DAC/Boost/Volume/AMP        | Limiter Set Fault/Status  |                |                             |            |  | _ |
| Power Control (0x00)                             | Status (0x10 - 0x11)      |                |                             |            |  |   |
| Master Software Powerdown O Normal Operation     | Boost:                    | Normal         |                             | Soft Reset |  |   |
| Software Powerdown                               | Amplifer Over Current:    | False          |                             |            |  |   |
| Amplifer and DAC Enabled                         | Over Temperature:         | False          |                             |            |  |   |
| Boost Enabled                                    | Over Temperature Warning: | False          |                             |            |  |   |
| Voltage Sense AD C Enabled                       | Under Voltage:            | False          |                             |            |  |   |
| Current Sense ADC                                | Clip:                     | False          |                             |            |  |   |
| Battery Voltage Sense ADC Enabled                | Limiter:                  | Normal         |                             |            |  |   |
| Auto Powerdown Enable Enabled                    | Battery Vokage:           | Above VBAT_INF |                             |            |  |   |
| Class D Power Switch (0x00)                      |                           |                |                             |            |  |   |
| VBAT and PVDD                                    | Rea                       | ad Status      |                             |            |  |   |
| ○ VBAT   |                           |                |                             |            |  |   |
|  |                           |                |                             | 2          |  |   |
| Config IC 1 - 55M4567 v1.8.0                     |                           |                |                             |            |  |   |

Figure 17. SSM4567 Evaluation Software GUI

### **PASSIVE COMPONENT SELECTION**

Although the evaluation board is preloaded with the passive components required for a basic configuration, the same circuit can be evaluated with different component values or filter designs. Selecting the proper components is the key to achieving the performance required at the budgeted cost.

#### **OUTPUT FERRITE BEADS (FB5 TO FB6)**

The output beads, FB5 to FB6, are suggested components for filtering out the EMI caused at the switching output nodes. The penalty for using ferrite beads for EMI filtering is slightly worse noise and distortion performance at the system level due to the nonlinearity of the beads. Ensure that these beads have enough current conducting capability while providing sufficient EMI attenuation. The current rating needed for an 8  $\Omega$  load is approximately 420 mA, and impedance at 100 MHz must be  $\geq$ 120  $\Omega$ . In addition, the lower the dc resistance (DCR) of these beads, the better for minimizing their power consumption. Table 4 describes suggested beads.

#### Table 4. Suggested Output Beads

| Part No.       | Manufacturer | Ζ (Ω) | I <sub>MAX</sub> (mA) | DCR (Ω) | Size (mm)               |
|----------------|--------------|-------|-----------------------|---------|-------------------------|
| BLM18PG121SN1D | Murata       | 120   | 2000                  | 0.05    | 1.6 	imes 0.8 	imes 0.8 |
| MPZ1608S101A   | TDK          | 100   | 3000                  | 0.03    | 1.6 	imes 0.8 	imes 0.8 |
| MPZ1608S221A   | TDK          | 220   | 2000                  | 0.05    | 1.6 	imes 0.8 	imes 0.8 |
| BLM18EG221SN1D | Murata       | 220   | 2000                  | 0.05    | 1.6 	imes 0.8 	imes 0.8 |

#### **OUTPUT SHUNTING CAPACITORS (C26 AND C27)**

There are two output shunt capacitors, C26 and C27, that work with the FB5 to FB6 ferrite beads, if they are used. Use small size (0603 or 0402), multilayer ceramic capacitors that are made of X7R or C0G (NP0) materials. Note that the capacitors can be used in pairs: a capacitor with small capacitance (up to 100 pF) plus a capacitor with a larger capacitance (less than 1 nF). This configuration provides thorough EMI reduction for the entire frequency spectrum. Alternatively, a single capacitor of approximately 470 pF can be used if reducing the bill of materials is a priority.

### **EVALUATION BOARD SCHEMATICS AND ARTWORK**











Figure 20. SSM4567 Evaluation Board Schematic (Continued)





12378-023







Figure 23. Evaluation Board Layout, Ground Plane (Layer 2)



Figure 24. Evaluation Board Layout, Power Plane (Layer 3)







Figure 26. Evaluation Board Layout, Top Silkscreen



Figure 27. Evaluation Board Layout, Bottom Silkscreen

### **ORDERING INFORMATION**

#### **BILL OF MATERIALS**

#### Table 5.

| ltem | Qty | Reference Designator  | Description                                  | Manufacturer                | Mfg Part Number      |
|------|-----|---|--|-----------------------------|----------------------|
| 1    | 2   | C17, C24  | Multilayer ceramic 10 V X5R 22 µF 0805       | Taiyo Yuden                 | LMK212BJ226MG-T      |
|      |     |   |  |                             |                      |
| 2    | 4   | C1, C13, C16, C20   | Multilayer ceramic 10 V X5R 10 µF 0805       | Taiyo Yuden                 | LMK212BJ106KG-T      |
| 3    | 17  | C2, C3, C4, C6, C23, C28, C29, C31,<br>C32, C34, C35, C36, C37, C38, C39,<br>C40, C41           | Multilayer ceramic 16 V X7R 0.1 μF<br>0603   | Murata                      | GRM188R71C104KA01D   |
| 4    | 7   | C11, C12, C15, C18, C21, C22, C25   | Multilayer ceramic 16 V X7R 1.0 μF<br>0603   | Taiyo Yuden                 | ЕМК107В7105КА-Т      |
| 5    | 4   | C5, C7, C14, C19  | Multilayer ceramic 50 V X7R 0.01 μF<br>0603  | Murata                      | GRM188R71H103KA01D   |
| 6    | 1   | С9  | Multilayer ceramic 50 V X7R 0.022 μF<br>0603 | Murata                      | GRM188R71H223KA01D   |
| 7    | 2   | C30, C33  | Multilayer ceramic 50 V NP0 10 pF 0603       | TDK Corporation             | C1608C0G1H100D       |
| 8    | 2   | C26, C27  | Multilayer ceramic 50 V NP0 510 pF<br>0603   | Murata                      | GRM1885C1H511JA01D   |
| 9    | 1   | C8  | Multilayer ceramic 50 V X7R 1 nF 0603        | Murata                      | GRM188R71H102KA01D   |
| 10   | 1   | C10   | Cap alum 100 μF 50 V 20% radial              | Panasonic EC                | ECA-1HM101B          |
| 11   | 1   | D1  | LED 610 NM orn wtr clr 0805 SMD              | Rohm<br>Semiconductor       | SML-210DTT86         |
| 12   | 10  | J1, J8, J9, J12, J19, J20, J21, J27,<br>J28, J29  | Conn header .100" sngl str                   | Sullins Electronics<br>Corp | PRPC040SAAN-RC       |
| 13   | 10  | J6, J10, J11, J22, J23, J7, J24, J13,<br>J15, J17   | Conn header .100" sngl str                   | Sullins Electronics<br>Corp | PRPC040SAAN-RC       |
| 14   | 4   | J2, J3, J4, J5  | Post binding grounded type nickel            | Johnson/Emerson             | 111-2223-001         |
| 15   | 3   | J14, J25, J26   | Conn header 2.54 mm 10 POS gold              | Sullins Electronics<br>Corp | SBH11-PBPC-D05-ST-BK |
| 16   | 1   | J16   | Conn header .100" dual str                   | Sullins Electronics<br>Corp | PRPC040DAAN-RC       |
| 17   | 1   | L1  | 2.2 μH, 1.85 A, 20%                          | Vishay Dale                 | IFSC1008ABER2R2M01   |
| 18   | 4   | FB1, FB2, FB3, FB4  | Ferrite bead 600 $\Omega$ 0805               | Taiyo Yuden                 | BK2125HM601-T        |
| 19   | 2   | FB5, FB6  | RES 0.0 Ω 1/8 W 0805 SMD                     | Panasonic EC                | ERJ-6GEY0R00V        |
| 20   | 19  | R2, R3, R4, R6, R20, R25, R26, R27,<br>R28, R29, R31, R32, R33, R34, R35,<br>R36, R38, R40, R41 | RES 33.0 Ω 1/10 W 1% 0603 SMD                | Panasonic EC                | ERJ-3GEYJ330V        |
| 21   | 1   | R21   | RES 470 Ω 1/10 W 1% 0603 SMD                 | Panasonic EC                | ERJ-3EKF4750V        |
| 22   | 1   | R1  | RES 10.0 K $\Omega$ 1/10 W 1% 0603 SMD       | Panasonic EC                | ERJ-3EKF1002V        |
| 23   | 1   | R5  | RES 0.0 Ω 1/10 W 0603 SMD                    | Panasonic EC                | ERJ-3GEY0R00V        |
| 24   | 1   | R7  | RES 3.01 Ω 1/10 W 1% 0603 SMD                | Panasonic EC                | ERJ-3EKF3011V        |
| 25   | 13  | R8, R9, R10, R11, R12, R13, R14,<br>R15, R16, R17, R18, R19, R22                                | RES 47.0 K Ω 1/10 W 1% 0603 SMD              | Panasonic EC                | ERJ-3EKF4702V        |
| 26   | 2   | R30, R37  | RES 51.0 Ω 1/10 W 1% 0603 SMD                | Panasonic EC                | ERJ-3EKF51R0V        |
| 27   | 1   | R39   | RES 100 K Ω 1/10 W 1% 0603 SMD               | Panasonic EC                | ERJ-3EKF1003V        |
| 28   | 2   | R23, R24  | RES 2.20 K $\Omega$ 1/10 W 1% 0603 SMD       | Panasonic EC                | ERJ-3EKF2201V        |
| 29   | 1   | S1  | Switch tactile SPST-NO 0.05A 12 V            | Tyco/Alcoswitch             | FSM6JSMA             |
| 30   | 7   | TP1, TP2, TP3, TP4, TP5, TP6, TP7   | Test point PC mini .040"D black              | Keystone<br>Electronics     | 5001                 |
| 31   | 3   | TP12, TP13, TP14  | Test point PC mini .040"D red                | Keystone<br>Electronics     | 5000                 |
| 32   | 1   | U2  | Receiver module fiber optic                  | Toshiba                     | TORX147(F, T)        |
| 33   | 6   | U7, U8, U9, U10, U11, U12   | Translator 1-bit unidirect SC70-5            | Fairchild<br>Semiconductor  | FXLP34P5X            |

| ltem | Qty | Reference Designator | Description                                 | Manufacturer   | Mfg Part Number    |
|------|-----|----------------------|---|----------------|--------------------|
| 34   | 1   | U5                   | Adjustable low dropout voltage regulator    | Analog Devices | ADP1711AUJZ-1.8-R7 |
| 35   | 1   | U1                   | 192 kHz AES3/SPDIF receiver                 | Cirrus Logic   | CS8416-CZZ         |
| 36   | 1   | U4                   | Adjustable low dropout voltage<br>regulator | Analog Devices | ADP1711AUJZ-3.3-R7 |
| 37   | 1   | U3                   | Oscillator 12.288 MHz 3.3 V SMD             | Abracon Corp   | ASEP-BLANK         |
| 38   | 1   | U6                   | SSM4567 WLCSP                               | Analog Devices | SSM4567CBZ-RL      |
|      |     |                      |   |                |                    |

### NOTES

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I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).



#### ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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