AMD Geode™ LX DB800 Development Board Mini-ITX-Baseboard Schematic

NOTES:

1) THIS SCHEMATIC IS TARGETED AT AN AMD GEODE™ LX PROCESSOR AND CS5535/CS5536 COMPANION DEVICE BASED DESIGN.

IMPORTANT NOTICE:

1. THIS DOCUMENT MAY NOT REFLECT THE MOST RECENT CHANGES IN BOARD DEVELOPMENT AND DEBUG. ANY DEVELOPER INTENDING TO USE THIS SCHEMATIC AS A REFERNCE SHOULD CONTACT THEIR LOCAL FIELD APPLICATIONS ENGINEER, REGIONAL SALES OFFICE, OR PROGRAM MANAGER FOR SCHEMATIC UPDATES, DESIGN RECOMMENDATIONS AND PCB LAYOUT GUIDELINES. AMD ALSO RECOMMENDS A DESIGN REVIEW OF BOTH THE SCHEMATIC DIAGRAM AND PCB LAYOUT BEFORE CONSIDERING PRODUCTION.

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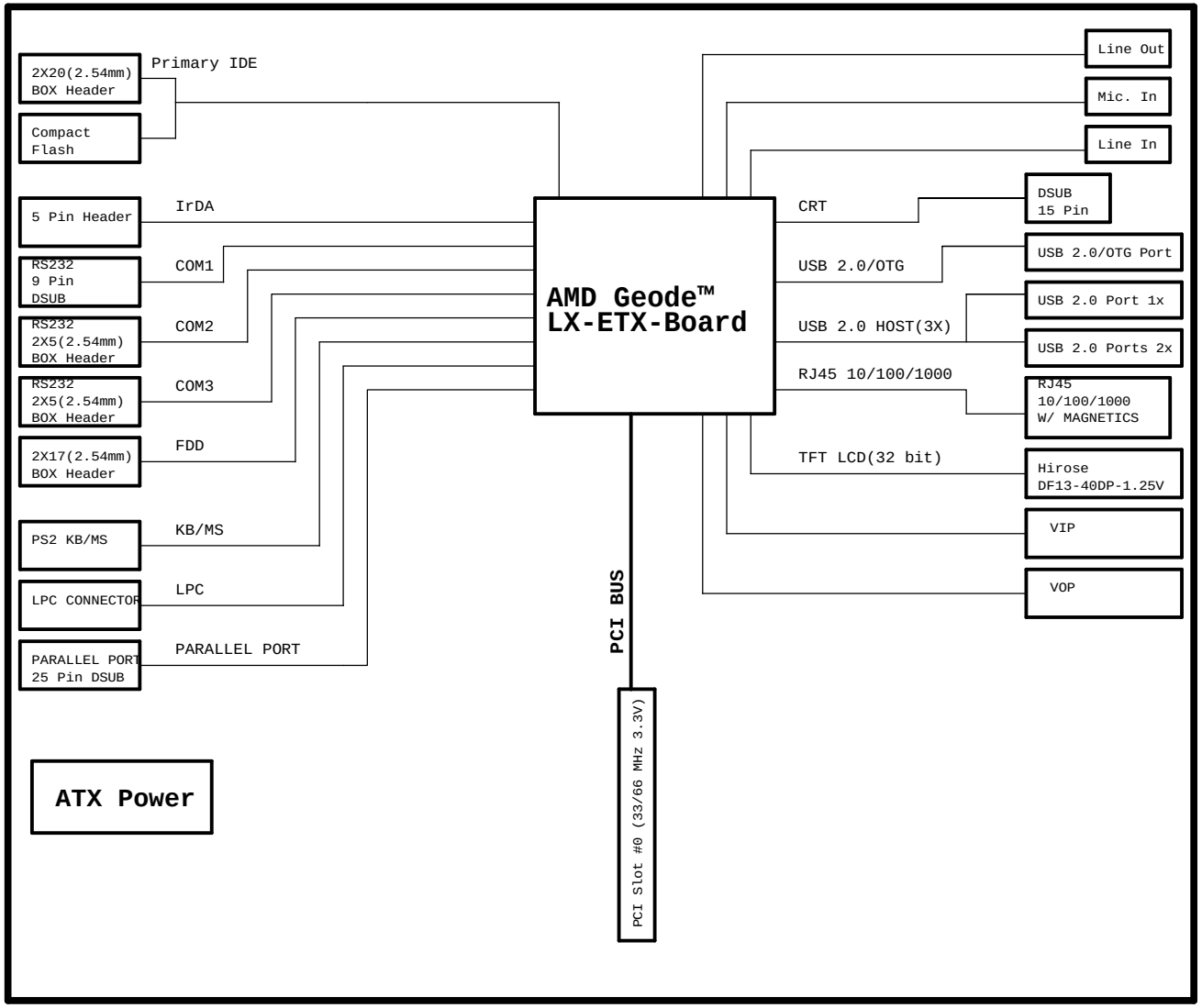
Mini-ITX-Baseboard Block Diagram



PCI0
IDSEL: AD24
INT: C D A
B

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PROJECT:	AMD Geode™ LX-Mini-ITX-Baseboard Schematic
PART NUMBER:	1000369
ASSEMBLY NAME:	SDK-AMD
SCHEMATICS:	ECR

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

3) DESIGN NOTES in red are critical, and must be understood and followed.

REVISIONS 5->6

1. REMOVED ALL 4PT CONNECTIONS, AND REMOVED THE DUPLICATE PAGE CONTAINING THE 31PIN CONNECTOR.
2. REMOVED THE SECOND USB 2.0 HOST CONTROLLER PAGE AND ALL ASSOCIATED COMPONENTS.

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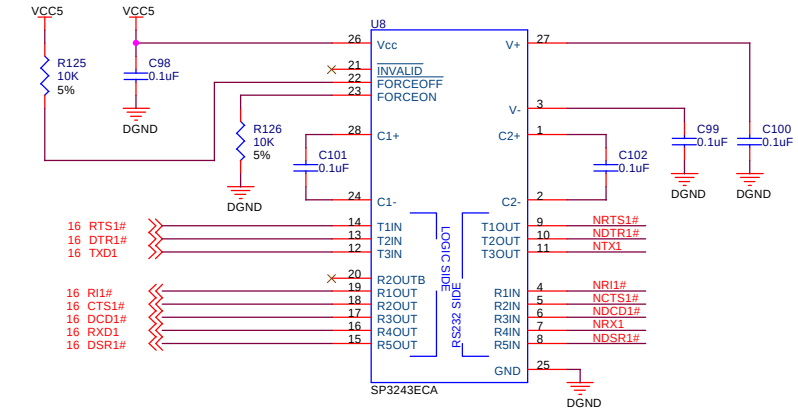

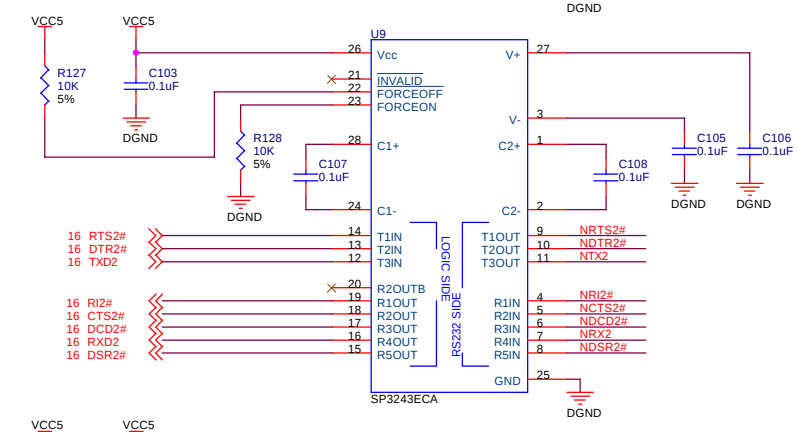

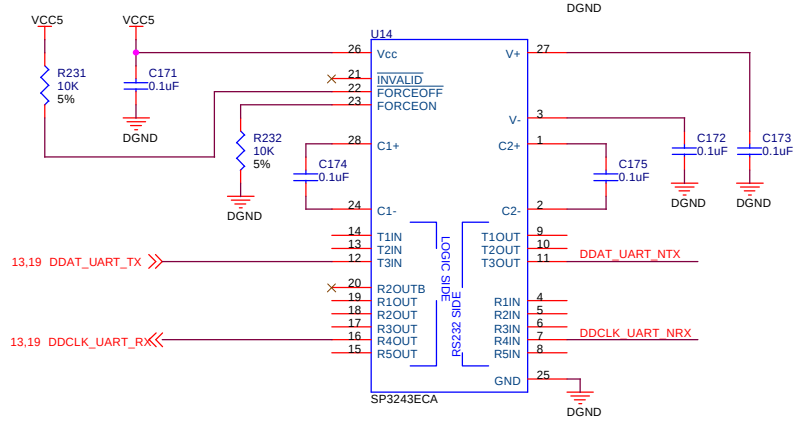

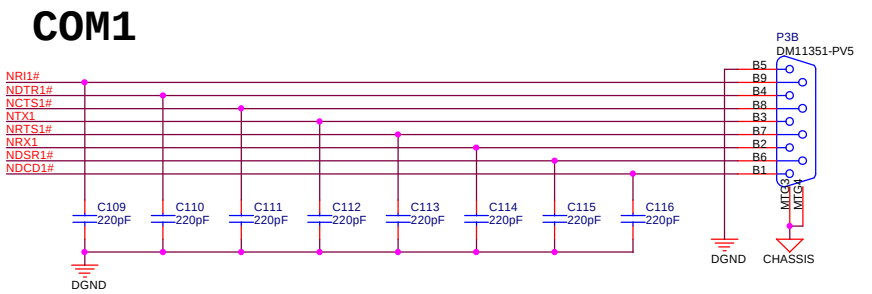

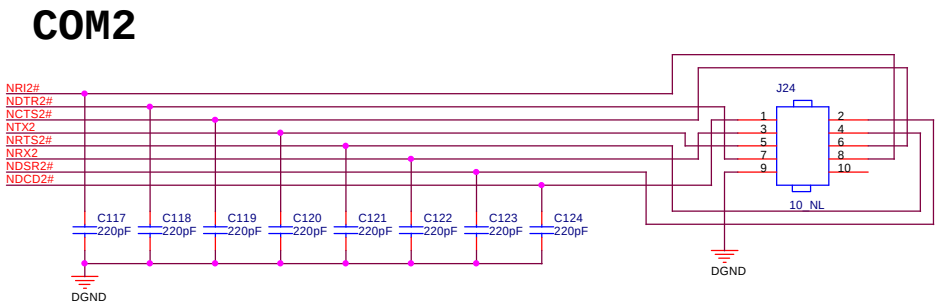

REVISIONS 6->7

1. ADDED THIRD RS232 LEVEL SHIFTER FOR THE THIRD COM PORT

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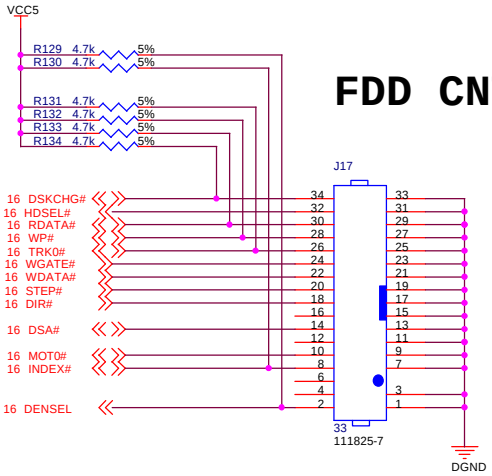
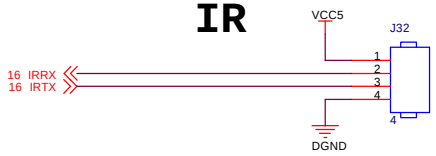
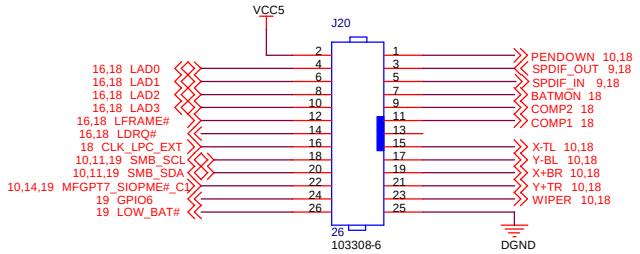
FDD CNT



IR



DEBUG HEADER



REVISIONS 9->10

1. CHANGED FDD CONNECTOR TO PRE-KEY'D TYPE

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ETHERNET/USB CONNECTOR

DESIGN NOTE: PLACE HEADER NEAR THE ETHERNET CONNECTOR

VCC5 J8 14,19 RESET# DGND

VCC_VDAC C27 0.1uF C28 10000pF AGND_ENET

J9 JW0-0006

CTAP_CAP_VCC
19 ENETTX+_BIDA+ MDI0_DH
19 ENETTX-_BIDA- MDI0_DL
19 ENETRX+_BIDB+ MDI1_DH
19 ENETRX-_BIDB- MDI1_DL
19 BIDC+ MDI2_DH
19 BIDC- MDI2_DL
19 BIDD+ MDI3_DH
19 BIDD- MDI3_DL
CTAP_CAP_GND
VCC_USB0 AGND_ENET
VCC1 DNEG1 DPOS1 GND1
VCC_USB1
VCC2 DNEG2 DPOS2 GND2
G_LED_C G_LED_A
Y_LED_A/G_LED_C Y_LED_C/G_LED_A
MH_E MH_USB

VCC5VSB R39 0 5% R40 0 5%

D10 BAT54TA LED0_FULL 19 LED1_L100M 19
D11 BAT54TA LED2_L10M 19
LED3_L1G 19

L1 DLW21SN900SQ2 18 USB0- 18 USB0+
L2 DLW21SN900SQ2 18 USB1- 18 USB1+

D16 SRV05-4 (D1 PWR, D2, D3, D4 GND) VCC5 DGND

FB10 HI1206N101R-00 FB11 HI1206N101R-00 DGND

CHASSIS

DESIGN NOTE: Place ESD protection components as close to the USB/Ethernet connector as possible.

USB CONNECTORS

DESIGN NOTE: Route USB_DM and USB_DP signals as differential pairs.

D8 SRV05-4 (D1 PWR, D2, D3, D4 GND) VCC5 DGND

L3 DLW21SN900SQ2 18 USB2- 18 USB2+
L4 DLW21SN900SQ2 18 USB3- 18 USB3+

VCC_USB2 VCC_USB3

J10 USB Type A 89485-0000 (PWR, D-, D+, GND, M1–M4) CHASSIS

J11 USB Mini AB 54819-0578 (VBUS, D-, D+, ID, GND, M1–M4) CHASSIS

19 USB_ID

C43 220pF FB21 BLM21BD601SN1D DGND CHASSIS

FB17 HI1206N101R-00 FB18 HI1206N101R-00 DGND

REVISIONS 6->7

1. REMOVED R169, R171, R173, R175, R177, R179, R181, R183.
2. VERIFIED THAT THERE IS NOT TERMINATION BUILT INTO THE ENET/USB CONNECTOR.

REVISIONS 5->6

1. REMOVED COMPONENTS THAT SUPPORTED DUAL ETHERNET SOLUTIONS.
2. VERIFIED WITH SEMTECS APP NOTE THAT SUPPLYING THE SRV05-4 PARTS WITH 5V IS OK.
3. CHANGED NOMINCLATURE FOR THE USB CONNECTORS TO USE "TYPE A, TYPE B ETC"

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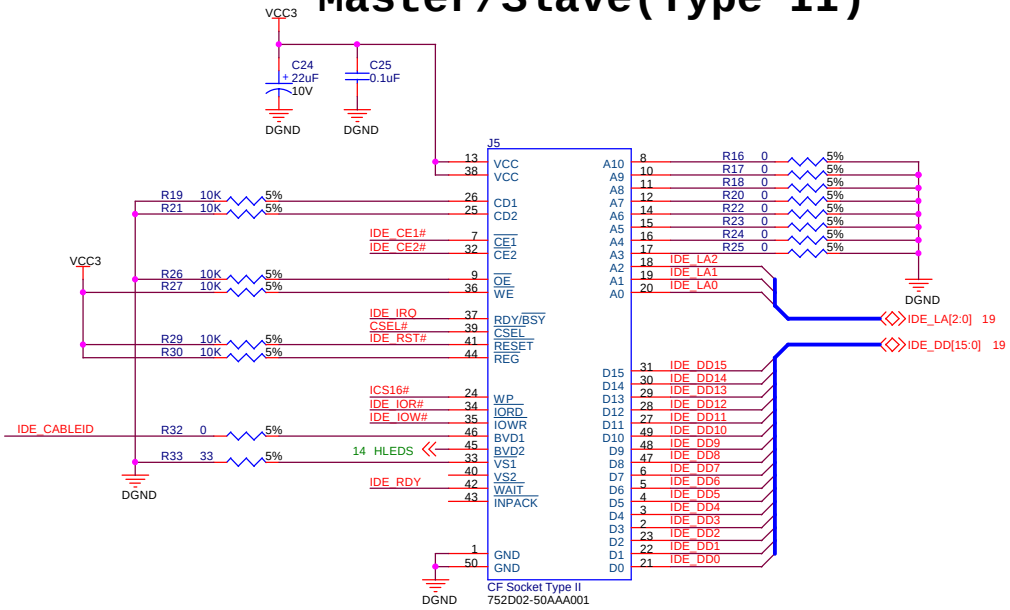
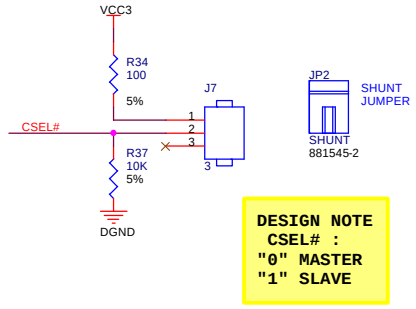
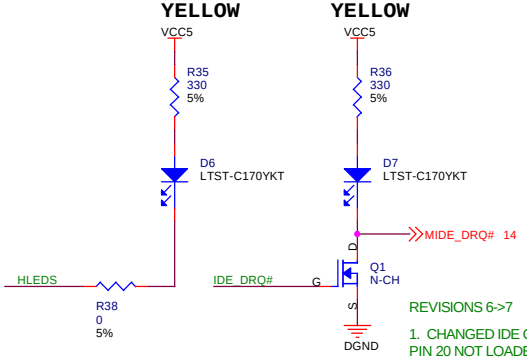
COMPACT FLASH CONNECTOR
Master/Slave(Type II)

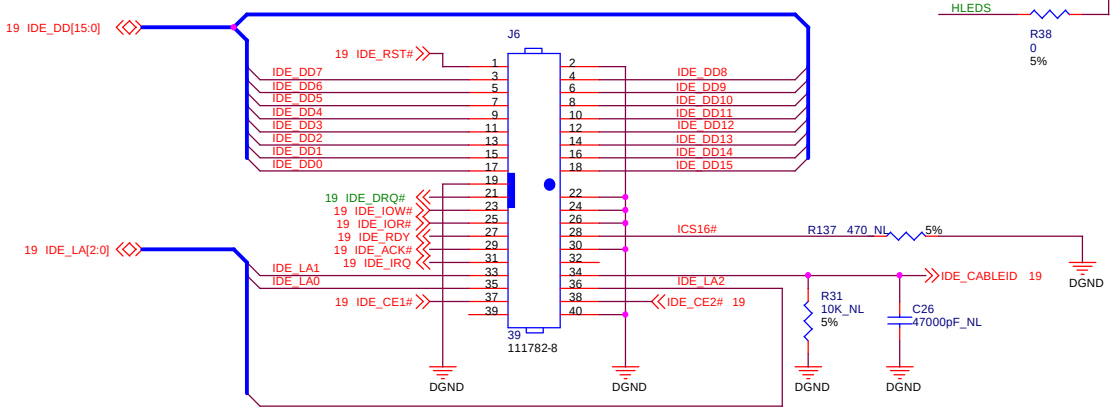




DESIGN NOTE
CSEL# :
"0" MASTER
"1" SLAVE



IDE CONNECTOR



REVISIONS 6->7

1. CHANGED IDE CONNECTOR TO BE A PART THAT IS SHIPPED WITH PIN 20 NOT LOADED. REMOVED J39 AND JP16 AS THEY ARE NO LONGER NEEDED TO SWITCH BTWN THE VOLTAGE SUPPLIED TO J6.20

REVISIONS 5->6

1. CHANGED SUPPLY VOLTAGE OF THE CF SLOT TO 3.3V SINCE 5V CARDS ARE REQUIRED TO RUN AT 3.3V AS WELL.
2. ADDED CONFIG RESISTOR TO J6.20 ALLOWING THE OPTION TO SWITCH BTWN 3.3V AND 5V.
3. REMOVED R28 AND R224 AND REPLACED WITH A 3PIN JUMPER SUCH THAT THE VOLTAGE SUPPLIED TO THE IDE SLOT IS CONFIGURABLE AND ONE CANNOT SHORT VCC5 TO VCC3.

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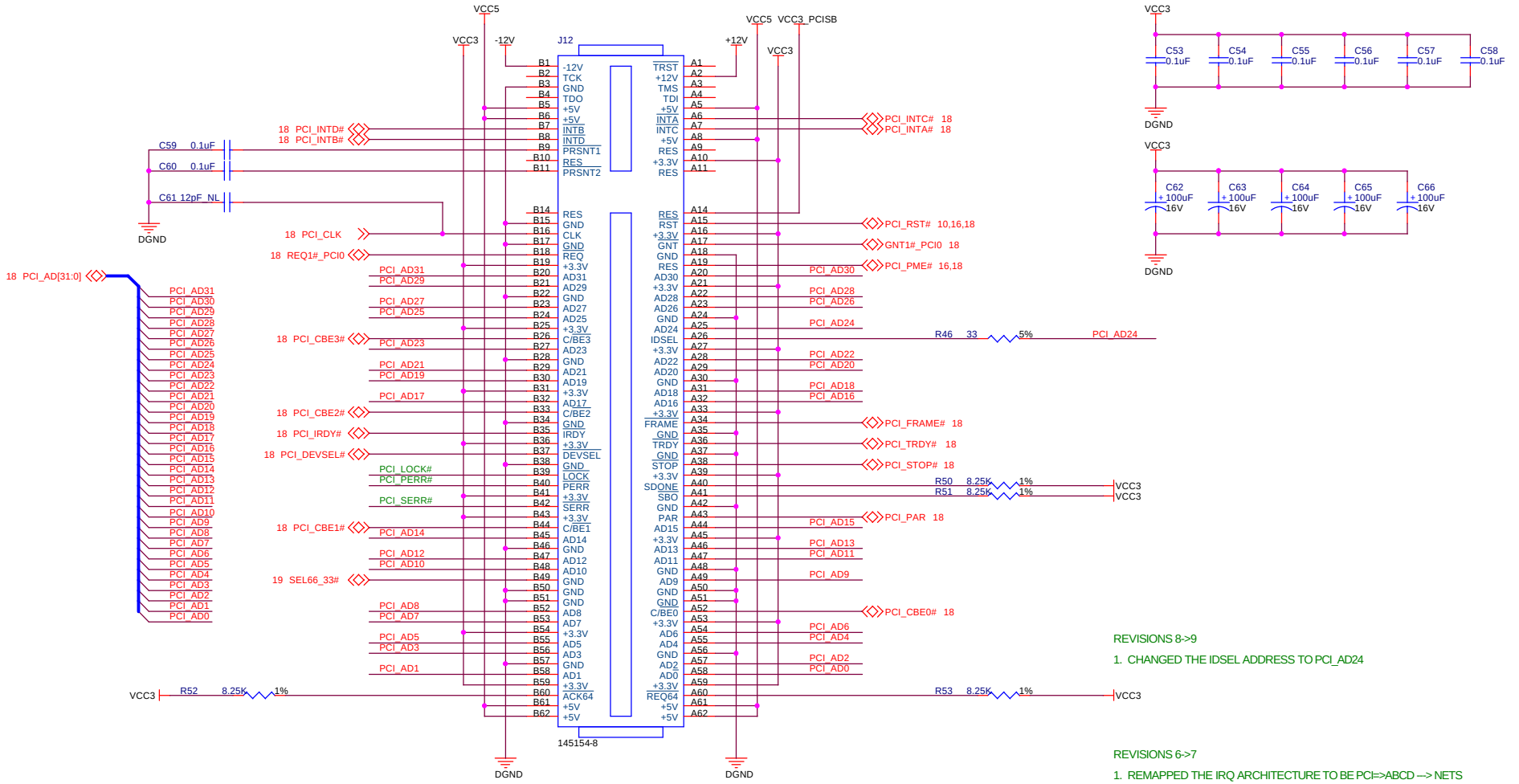

PCI 33 or 66 MHz (3.3V Slot)

REVISIONS 8->9

1. CHANGED THE IDSEL ADDRESS TO PCI_AD24

REVISIONS 6->7

1. REMAPPED THE IRQ ARCHITECTURE TO BE PCI=>ABCD --> NETS CDAB, REMOVED C52 (100uF ON -12V)

REVISIONS 6->7

1. REMAPPED THE IRQ ARCHITECTURE TO BE PCI=>ABCD --> NETS CDAB, REMOVED C52 (100uF ON -12V)

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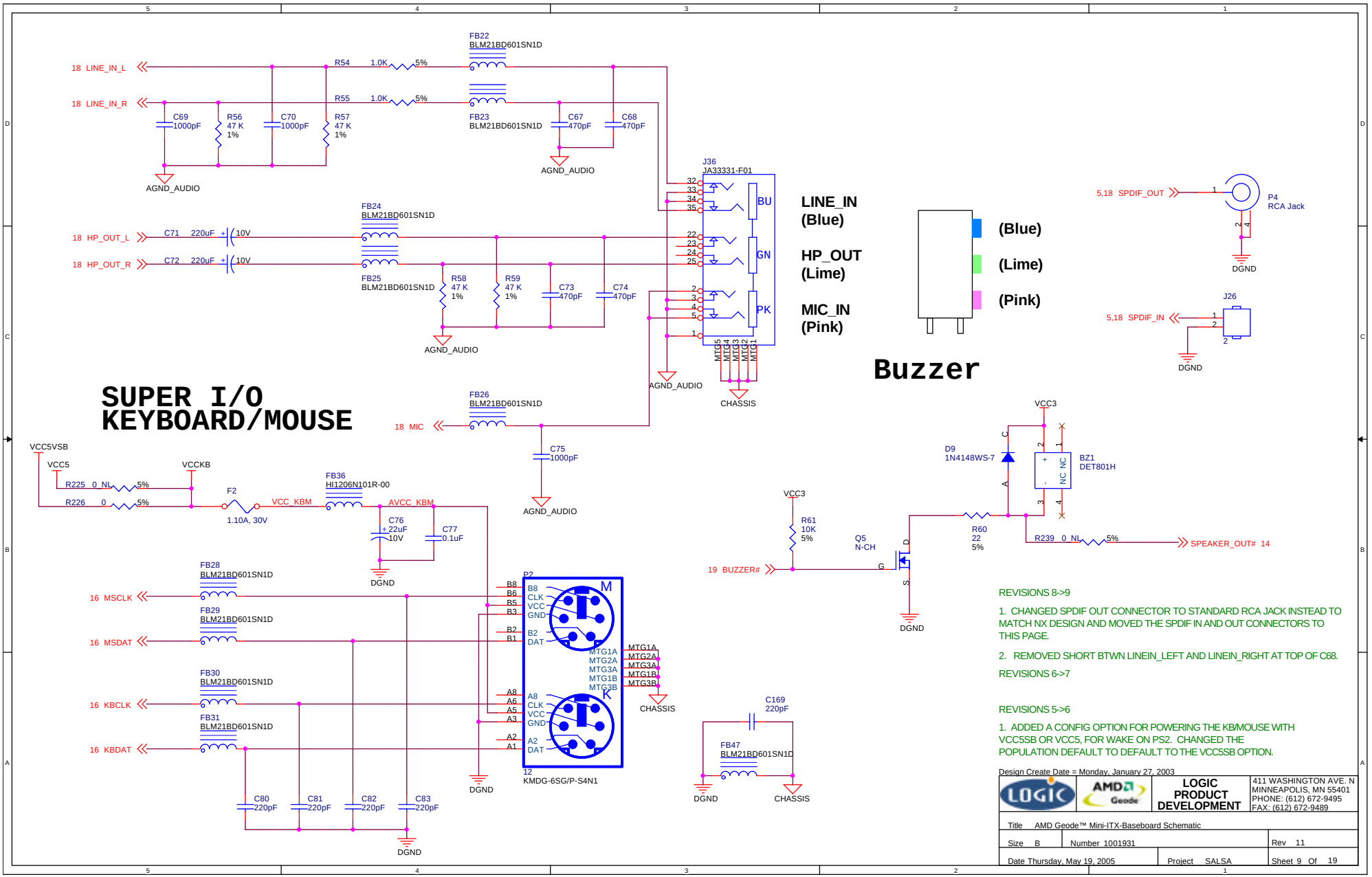
18 LINE_IN_L
18 LINE_IN_R
R54 1.0K 5%
R55 1.0K 5%
FB22 BLM21BD601SN1D
FB23 BLM21BD601SN1D
C69 1000pF
R56 47 K 1%
C70 1000pF
R57 47 K 1%
C67 470pF
C68 470pF
AGND_AUDIO
J36 JA33331-F01
BU
GN
PK
MTG5
MTG4
MTG3
MTG2
MTG1
CHASSIS
18 HP_OUT_L
18 HP_OUT_R
C71 220uF 10V
C72 220uF 10V
FB24 BLM21BD601SN1D
FB25 BLM21BD601SN1D
R58 47 K 1%
R59 47 K 1%
C73 470pF
C74 470pF
LINE_IN (Blue)
HP_OUT (Lime)
MIC_IN (Pink)
(Blue)
(Lime)
(Pink)
Buzzer
5,18 SPDIF_OUT
P4 RCA Jack
DGND
5,18 SPDIF_IN
J26
SUPER I/O KEYBOARD/MOUSE
18 MIC
FB26 BLM21BD601SN1D
C75 1000pF
VCC5VSB
VCC5
VCCKB
R225 0_NL 5%
R226 0 5%
F2
1.10A, 30V
VCC_KBM
FB36 HI1206N101R-00
AVCC_KBM
C76 22uF 10V
C77 0.1uF
VCC3
D9 1N4148WS-7
BZ1 DET801H
NC NC
R61 10K 5%
19 BUZZER#
Q5 N-CH
R60 22 5%
R239 0_NL 5%
SPEAKER_OUT# 14
FB28 BLM21BD601SN1D
16 MSCLK
FB29 BLM21BD601SN1D
16 MSDAT
FB30 BLM21BD601SN1D
16 KBCLK
FB31 BLM21BD601SN1D
16 KBDAT
P2
B8 CLK VCC GND B2 DAT
A8 CLK VCC GND A2 DAT
MTG1A MTG2A MTG3A MTG1B MTG3B
12 KMDG-6SG/P-S4N1
C80 220pF
C81 220pF
C82 220pF
C83 220pF
C169 220pF
FB47 BLM21BD601SN1D
REVISIONS 8->9
1. CHANGED SPDIF OUT CONNECTOR TO STANDARD RCA JACK INSTEAD TO MATCH NX DESIGN AND MOVED THE SPDIF IN AND OUT CONNECTORS TO THIS PAGE.
2. REMOVED SHORT BTWN LINEIN_LEFT AND LINEIN_RIGHT AT TOP OF C68.
REVISIONS 6->7
REVISIONS 5->6
1. ADDED A CONFIG OPTION FOR POWERING THE KB/MOUSE WITH VCC5SB OR VCC5, FOR WAKE ON PS2. CHANGED THE POPULATION DEFAULT TO DEFAULT TO THE VCC5SB OPTION.
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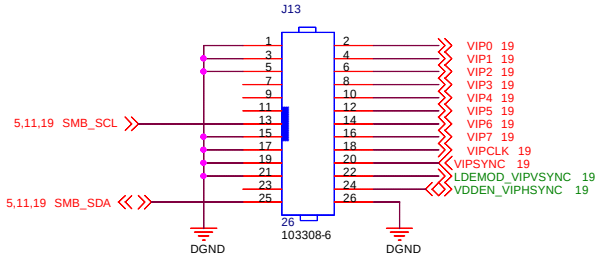
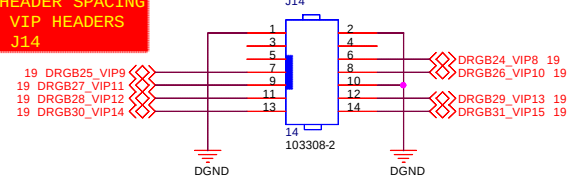
VIP 8-BIT HEADER



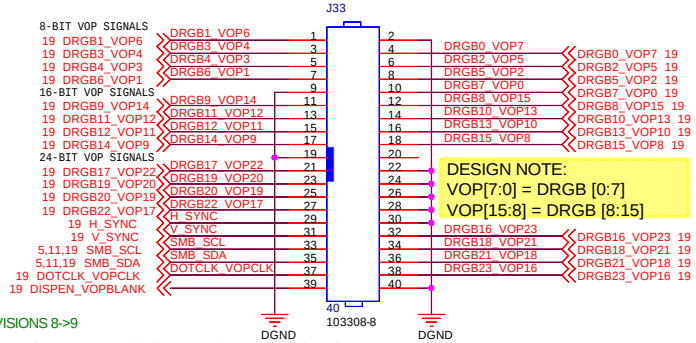
LEAVE 10-PIN HEADER SPACING BETWEEN VIP HEADERS

VIP 16-BIT HEADER

LAYOUT NOTE: LEAVE 10-PIN HEADER SPACING BETWEEN VIP HEADERS J13 AND J14



VOP 8-BIT, 16-BIT & 24-BIT HEADER



DESIGN NOTE:
VOP[7:0] = DRGB [0:7]
VOP[15:8] = DRGB [8:15]

REVISIONS 8->9

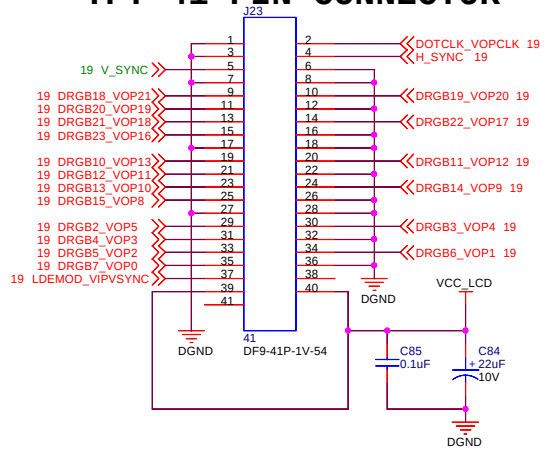
1. CHANGED NET NAMES FOR LDEMOD_VIPHSYNC WAS RENAMED TO LDEMOD_VIPVSYNC VDDEN_VIPVSYNC WAS RENAMED TO VDDEN_VIPHSYNC

REVISIONS 6->7

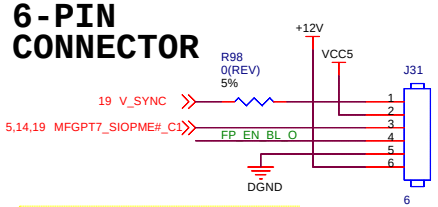
1. CHANGED J33 TO BE A 40PIN IDE STYLE CONNECTOR THAT IS PINNED OUT WITH THE SAME GNDS AS A STANDARD IDE CABLE, THIS CONNECTOR IS NOT SHROUDED.

DISPLAY MODULE

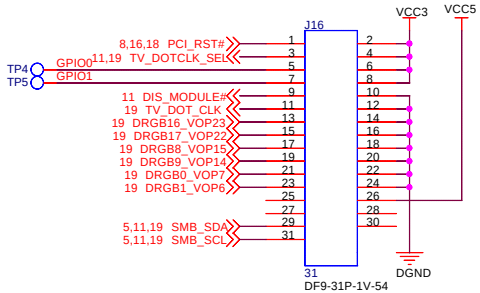
TFT 41-PIN CONNECTOR



6-PIN CONNECTOR

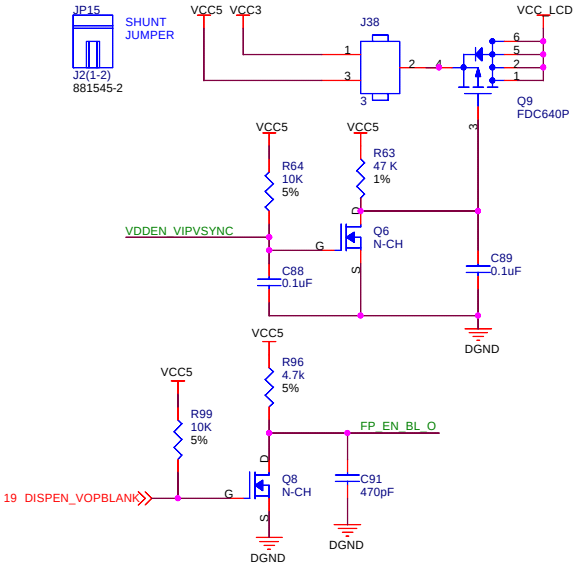


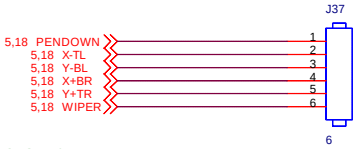
DESIGN NOTE: DOTCLK_SEL to Geode LX processor
0 = TV_DOT_CLK
1 = 48MHz Clock from 5536



31-PIN CONNECTOR

LAYOUT NOTE: ADD SILKSCREEN THAT SAYS: PANEL VCC SELCTION





TSW-106-23-T-S

REVISIONS 5->6

1. ADDED NET VIPSYNC TO J13.20, REMOVED NETS LDEMOD_VIPSYNC AND VDDEN_VIPSYNC FROM J23.4,5 AND REPLACED WITH H_SYNC AND V_SYNC.
2. J23 WAS REPINNED TO PROPERLY MATCH THE FOOTPRINT.
3. REPLACED J35 WITH A THREE PIN HEADER SUCH THAT A USER IS UNABLE TO SHORT THE 5V TO 3V PLANE WITH THE SHUNT. ADDED A BUNCH OF SIGNALS TO THE 31PIN CONNECTOR J16.

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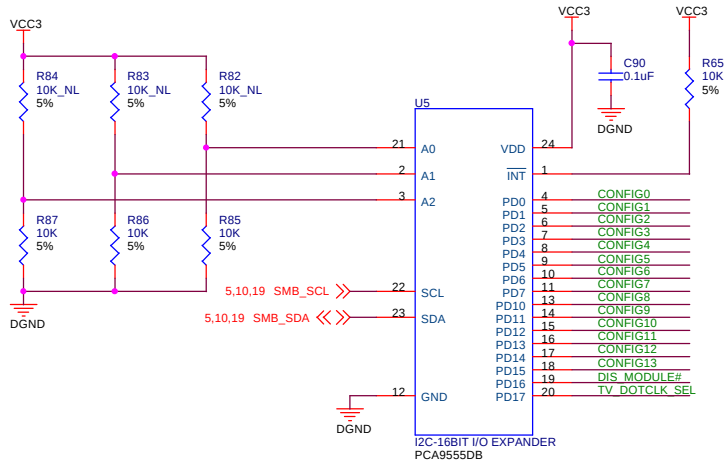
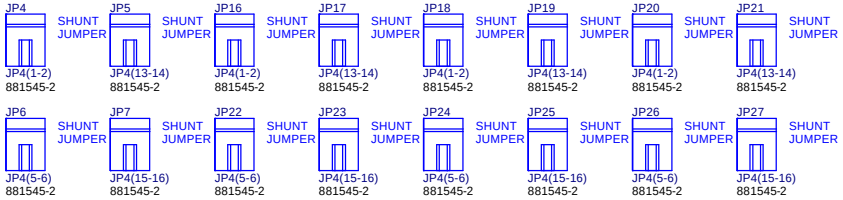
DESIGN NOTE: I2C address select

0	0	0	=	40h
0	0	1	=	42h
0	1	0	=	44h
0	1	1	=	46h
1	0	0	=	48h
1	0	1	=	4Ah
1	1	0	=	4Ch
1	1	1	=	4Eh

DEFAULT



DESIGN NOTE: Configuration header defined on next page



REVISIONS 8->9

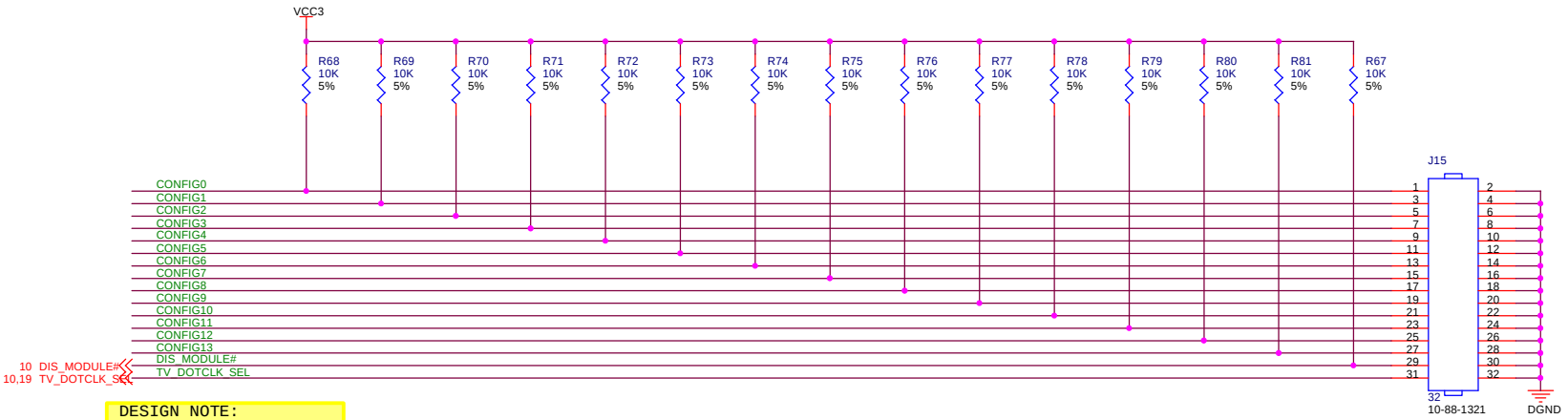
1. CHANGE THE PORT ADDRESS TABLE FOR U5 TO 40,42,44,46,48,4A,4C, AND 4E.
2. CHANGED THE DEFAULT PORT ADDRESS OF U5 TO 40h TO MATCH NORWICH.

REVISIONS 6->7

1. PUT DEFAULT I2C GPIO ADDRESS INTO TABLE, CHANGED NET NAME OF DOTCLK_SEL TO TV_DOTCLK_SEL

REVISIONS 5->6

1. CHANGED NAME OF PAGE, CHANGED ADDRESS OF I2C DEVICE, ADDED NEW NET DIS_MODULE# TO THE JUMPER SET.
2. VERIFIED THE PINOUT OF THE REQUESTED REPLACEMENT PART FOR THE IO EXPANDER => PCA9555 PART. IT IS A DROP IN.



DESIGN NOTE: DOTCLK_SEL IS PULLED UP ON THE ETX SOM, THE DEFAULT WILL DISABLE THE TV DOTCLK REFERENCE

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Header Pins	Meaning for Flat Panel output	Pin Pair#
28-27	Reserved	13
26-25	Reserved	12
24-23 MSB	Panel refresh rate	11:9
22-21	000 - 60Hz	
20-19 LSB	001 - 70Hz	
	010 - 72Hz	
	011 - 75Hz	
	100 - 85Hz	
	101 - 90Hz	
	110 - 100Hz	
	101 - 111 Reserved	
18-17	VSync polarity	8
	0 - Active low	
	1 - Active high	
16-15	HSync polarity	7
	0 - Active low	
	1 - Active high	
14-13	Reserved	6
12-11	Data bus width and data type	5
	0 - 9, 12, 18, 24 bit data bus, 1 pixel per clock	
	1 - 18, 24 bit data bus, 2 pixels per clock	
10-9 MSB	Panel resolution	4:2
8-7	000 - 320x240	
6-5 LSB	001 - 640x480	
	010 - 800x600	
	011 - 1024x768	
	100 - 1152x864	
	101 - 1280x1024	
	110 - 1600x1280	
	111 - Reserved	
4-3	Panel Type	1
	0 - TFT	
	1 - LVDS	

Header Pins	Meaning for TV output	Pin Pair#
28-27	Extended SAV/EAV codes	13
	0 - Not used	
	1 - Added to stream	
26-25 MSB	4:4:4 to 4:2:2 Conversion scheme	12:11
24-23 LSB	00 - 4:2:2 Co-sited	
	01 - 4:2:2 Interspersed, respective co-samples	
	10 - 4:2:2 Interspersed, alternating successive samples	
	11 - Reserved	
22-21	VIP 2.0 support level	10
	0 - 8-bit, level I	
	1 - 16-bit, level II	
20-19 MSB	Output stream type	9:8
18-17 LSB	00 - VIP 1.1	
	01 - VIP 2.0	
	10 - CCIR-656	
	11 - Reserved	
16-15 MSB	Refresh rate	7:6
14-13 LSB	00 - 50Hz	
	01 - 59.94Hz	
	10 - 60Hz	
	11 - Reserved	
12-11	Interlace	5
	0 - Interlaced	
	1 - Non-interlaced (progressive)	
10-9 MSB	TV resolution	4:2
8-7	000 - Reserved	
6-5	001 - 640x480	
	010 - 720x480	
	011 - 720x576	
	100 - 1280x720	
	101 - 1920x1080	
	111 - Reserved	
4-3	Output path	1
	0 - TFT path	
	1 - Video Output port	
2-1	Panel or TV mappings select	0
	0 - Flat panel output	
	1 - TV output	

REVISIONS 8->9

1. REMOVED THE 2-1 PANEL OR TV MAPPINGS SELECT PORTION OF THE TABLE (WAS REDUNDANT WITH MAIN TABLE.

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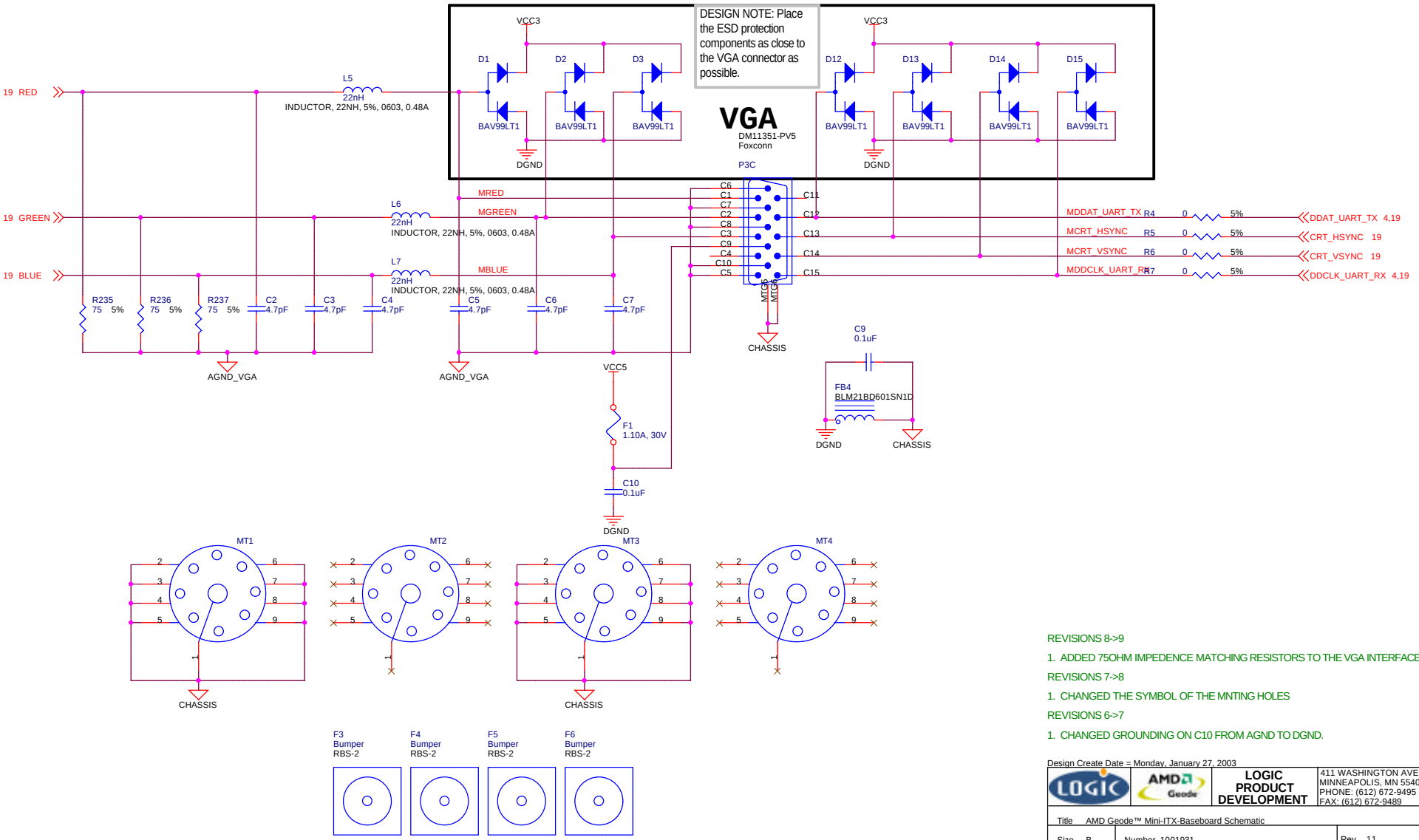

REVISIONS 8->9

1. ADDED 75OHM IMPEDENCE MATCHING RESISTORS TO THE VGA INTERFACE.

REVISIONS 7->8

1. CHANGED THE SYMBOL OF THE MNTING HOLES

REVISIONS 6->7

1. CHANGED GROUNDING ON C10 FROM AGND TO DGND.

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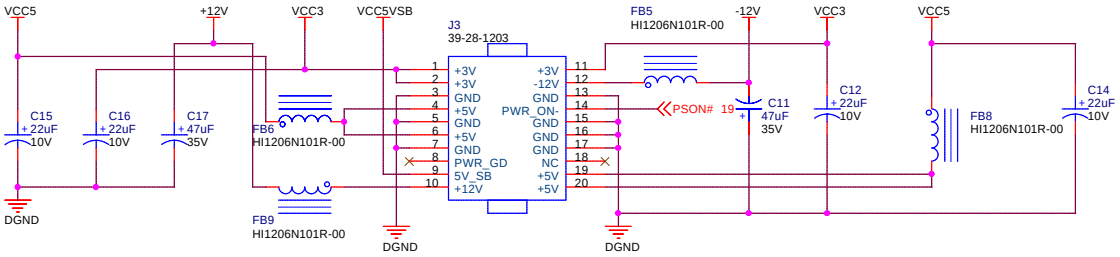
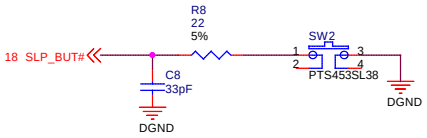
ATX Power

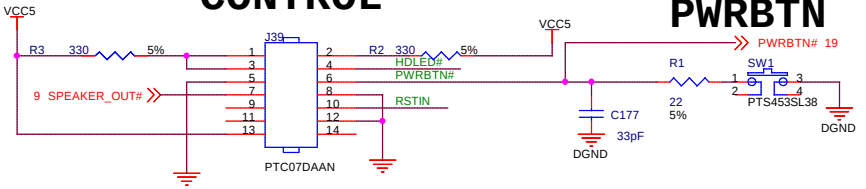


SLPBTN

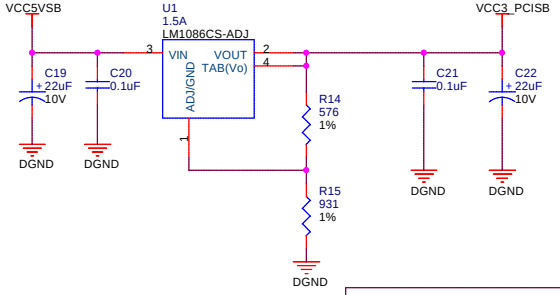


CHASSIS CONTROL

PWRBTN

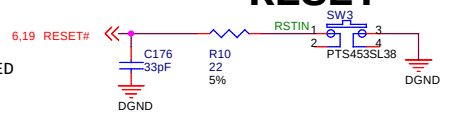


DESIGN NOTE: To ensure proper operation, 2nd generation (or later) ATX power supplies are required. Supply must supply at least 500mA on 5VSB.

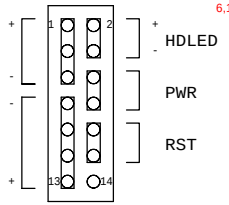


LAYOUT NOTE: LABEL ON SILKSCREEN WHAT THE LED'S ARE

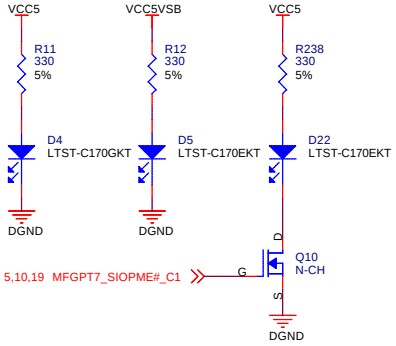
RESET

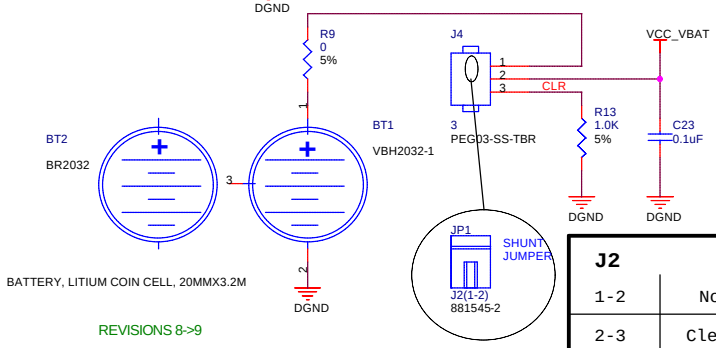


CONNECTION DIAGRAM

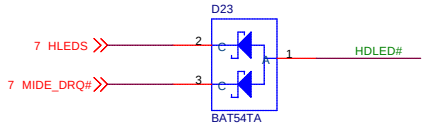


POWER GREEN **5VSB RED** **PWR MANAGEMENT RED**





J2	
1-2	Normal
2-3	Clear CMOS



REVISIONS 6->7

1. REMOVED C13, FB7 AND REMOVED THE NET -5V FROM J3.18, WE DON'T USE -5V THEREFORE NO BYPASSING IS NECESSARY.
2. CHANGED DEBOUNCE CKT ON PWRBTN AND EXTERNAL RESET BUTTON

REVISIONS 8->9

1. CHANGED OUT THE SWITCHES TO MATCH THE NX DESIGN
2. CHANGED OUT THE LEDS TO MATCH THE NX DESIGN
3. CHANGED OUT THE THE BATTERY HOLDER TO MATCH NX.
4. ADDED LED DRIVEN BY NET MFGPT7_SIOPME#_C1 FOR A PWR MANAGEMENT INDICATOR.
5. CHANGED EXTERNAL LED'S/SWITCHES HEADER TO MATCH NX, ADDED OR GATE FOR HD LIGHT TO SHOW EITHER CF CARD OR IDE SLOT ACTIVITY. REMOVED SIGNAL PSON# FROM HEADER. AND ADDED SPEAKER INPUT TO HEADER.

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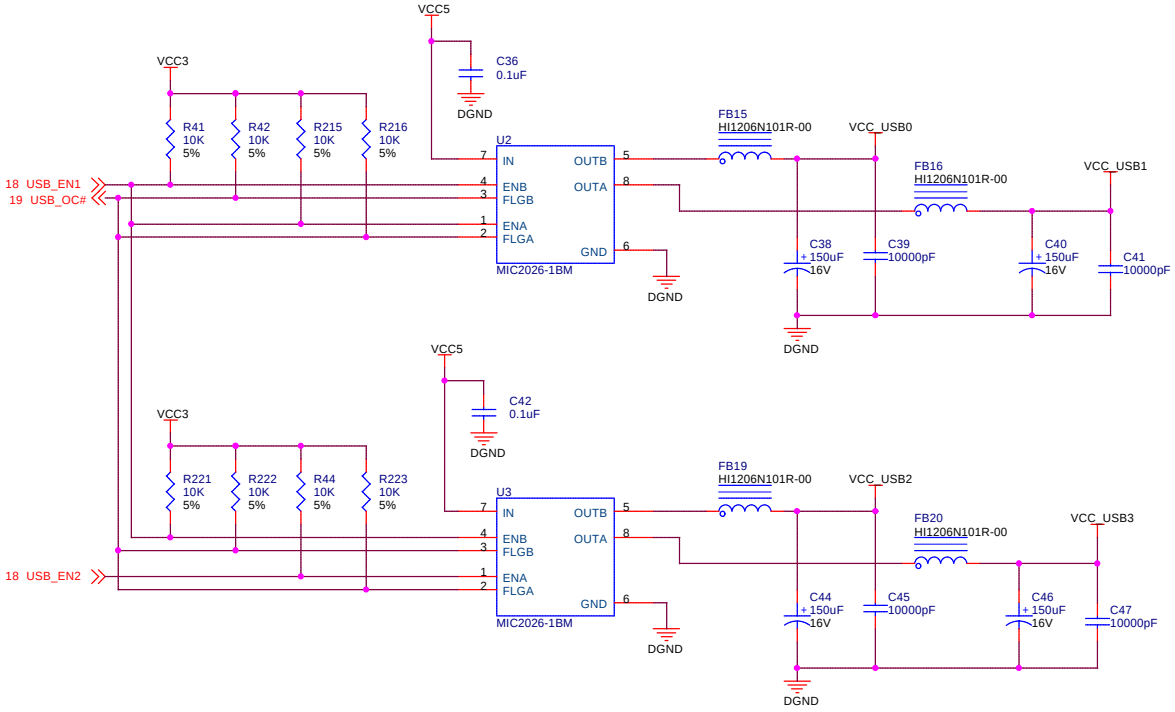

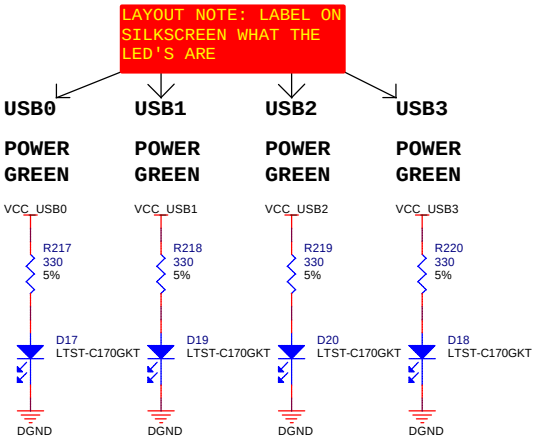

REVISIONS 9->10

1. FIXED MISTAKE ON U2, U3 THAT HAD THE ENABLES AND FLAGS SWAPPED ON CHANNEL A

REVISIONS 8->9

1. FIXED MISTAKE ON U2 THAT HAD ENABLEB AND FLGB CROSSED.
2. CHANGED USB_EN1#/EN2# TO USB_EN1 AND USB_EN2 BECAUSE THEY ARE ACTIVE HIGH SIGNALS.
3. CHANGED OUT THE MICREL USB POWER SWITCHES FROM THE MIC2076-2BM TO THE MIC2026-1BM WHICH IS ACTIVE HIGH INPUTS.

REVISIONS 6->7

1. FIXED DANGLING NET ON FB16.

REVISIONS 5->6

1. REMOVED THE UNECESSARY CAPS ON VCC_USB0, VCC_USB1, VCC_USB2, VCC_USB3. REMOVED THE FUSES ON THE OUTPUTS OF THE POWER SWITCHES, THEY ARE REDUNDANT. REPOISTIONED THE FERRITES.

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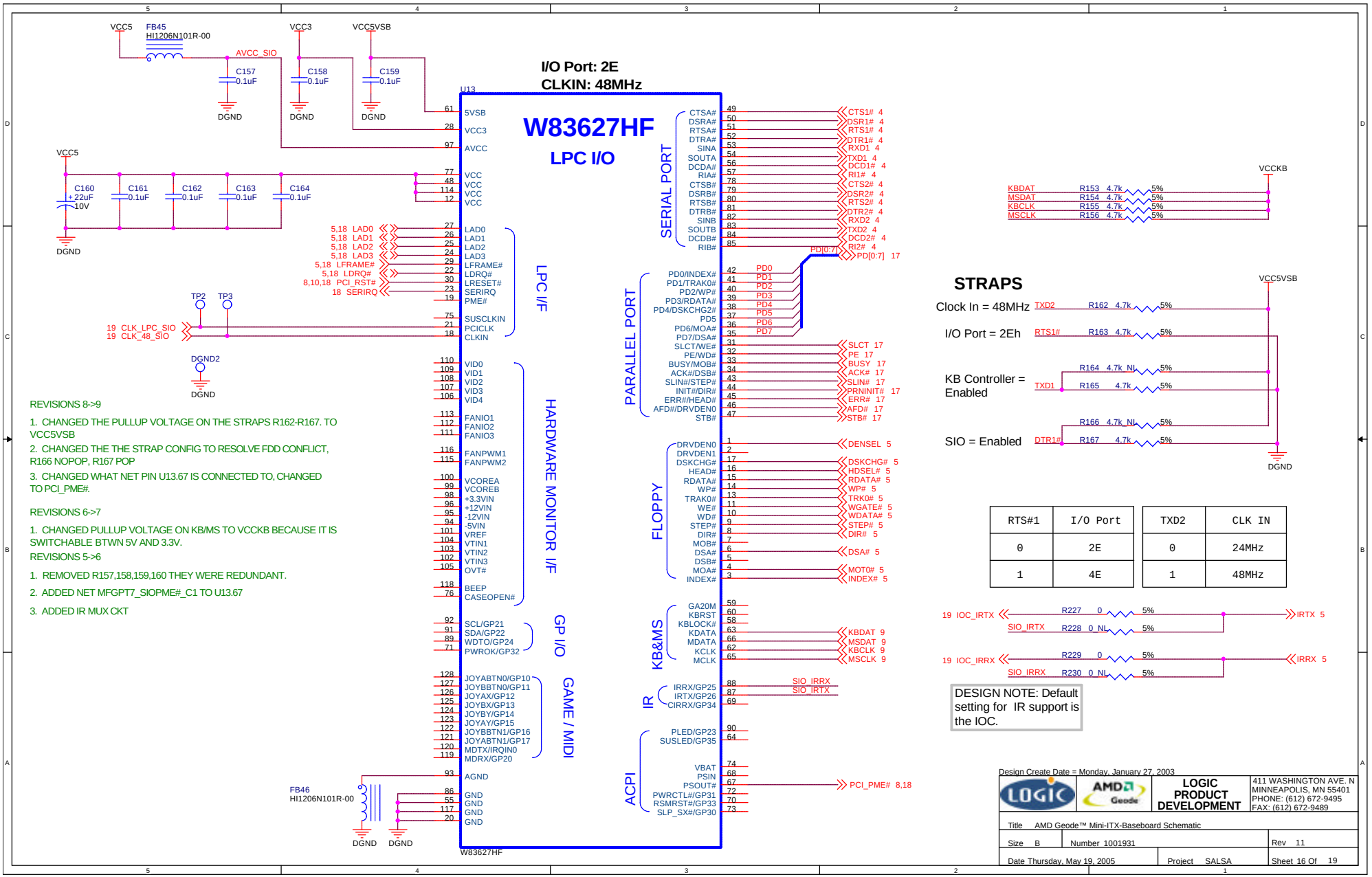

RTS#1	I/O Port	TXD2	CLK IN
0	2E	0	24MHz
1	4E	1	48MHz

REVISIONS 8->9

1. CHANGED THE PULLUP VOLTAGE ON THE STRAPS R162-R167. TO VCC5VSB
2. CHANGED THE THE STRAP CONFIG TO RESOLVE FDD CONFLICT, R166 NOPOP, R167 POP
3. CHANGED WHAT NET PIN U13.67 IS CONNECTED TO, CHANGED TO PCI_PME#.

REVISIONS 6->7

1. CHANGED PULLUP VOLTAGE ON KB/MS TO VCCKB BECAUSE IT IS SWITCHABLE BTWN 5V AND 3.3V.

REVISIONS 5->6

1. REMOVED R157,158,159,160 THEY WERE REDUNDANT.
2. ADDED NET MFGPT7_SIOPME#_C1 TO U13.67
3. ADDED IR MUX CKT

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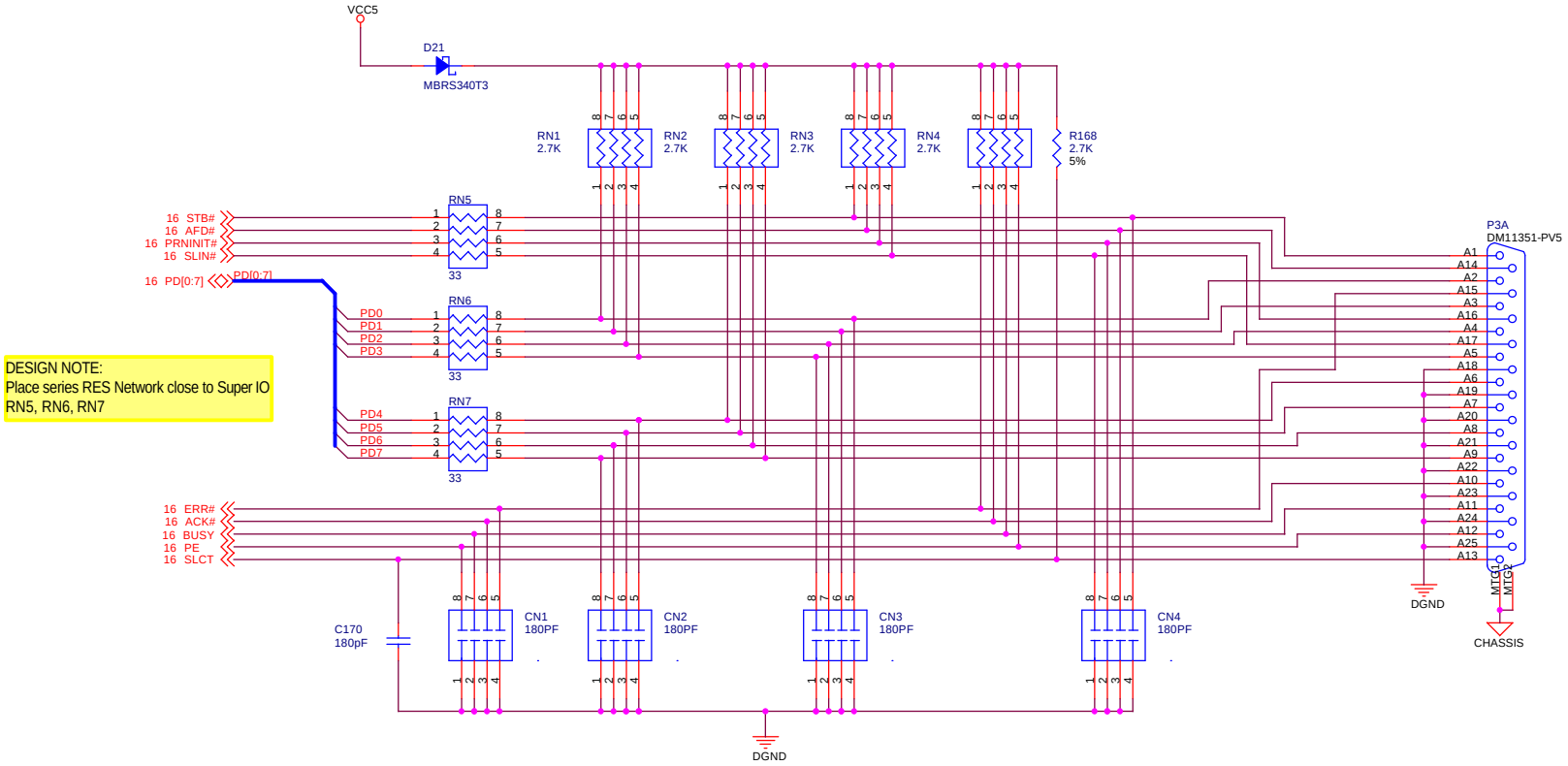

DESIGN NOTE:
Place series RES Network close to Super IO
RN5, RN6, RN7

REVISIONS 5->6

1. ADDED A SERIES DIODE BETWEEN THE PULLUP RESISTORS AND THE VCC5 PLANE.

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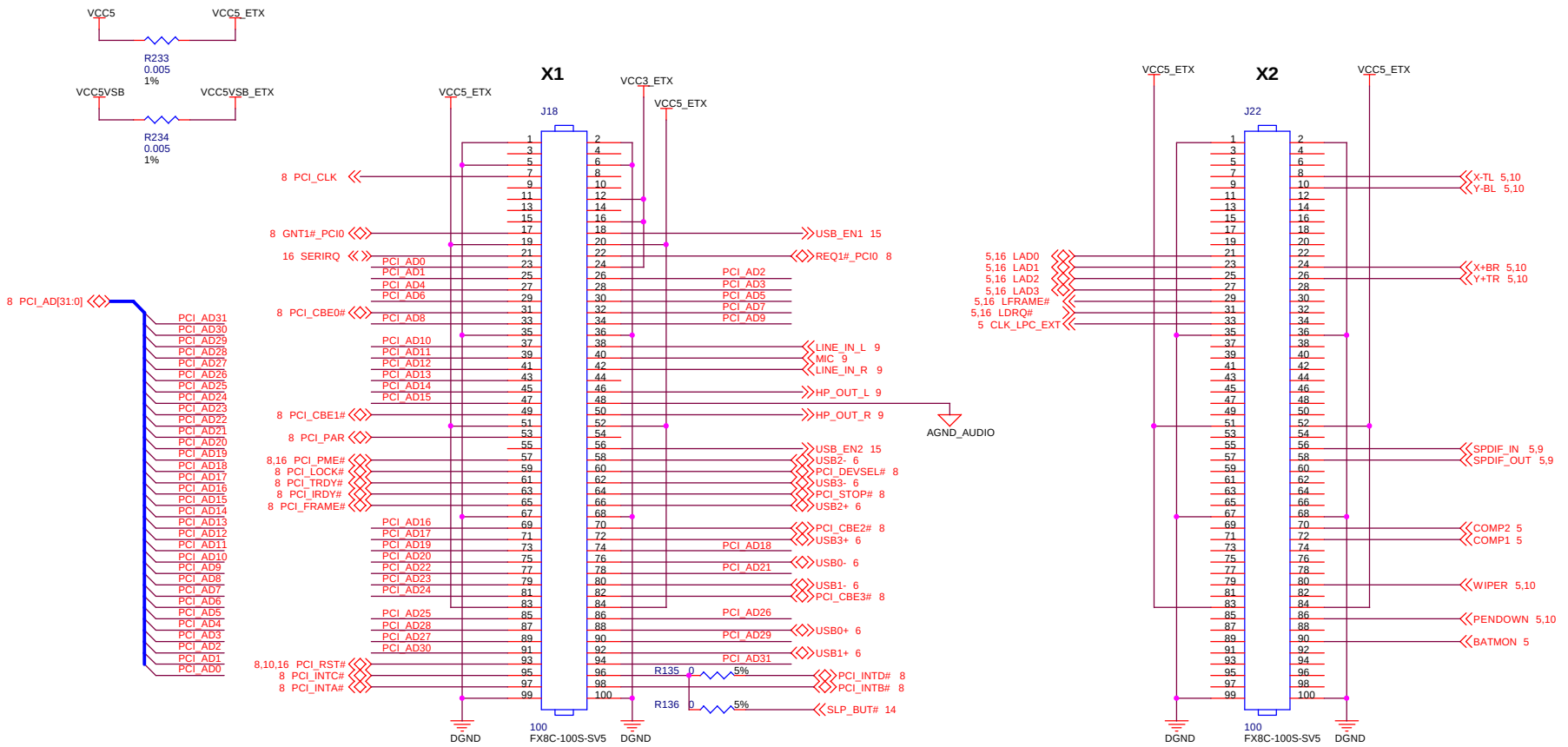

REVISIONS 8->9

1. CHANGED INPUT VOLTAGE TO R234 TO BE VCC5VSB
2. CHANGED USB_EN1#/EN2# TO USB_EN1 AND USB_EN2 BECAUSE THEY ARE ACTIVE HIGH SIGNALS.

REVISIONS 6->7

1. ADDED 2 SENSE RESISTORS FOR MEASURING CURRENT OF THE SOM

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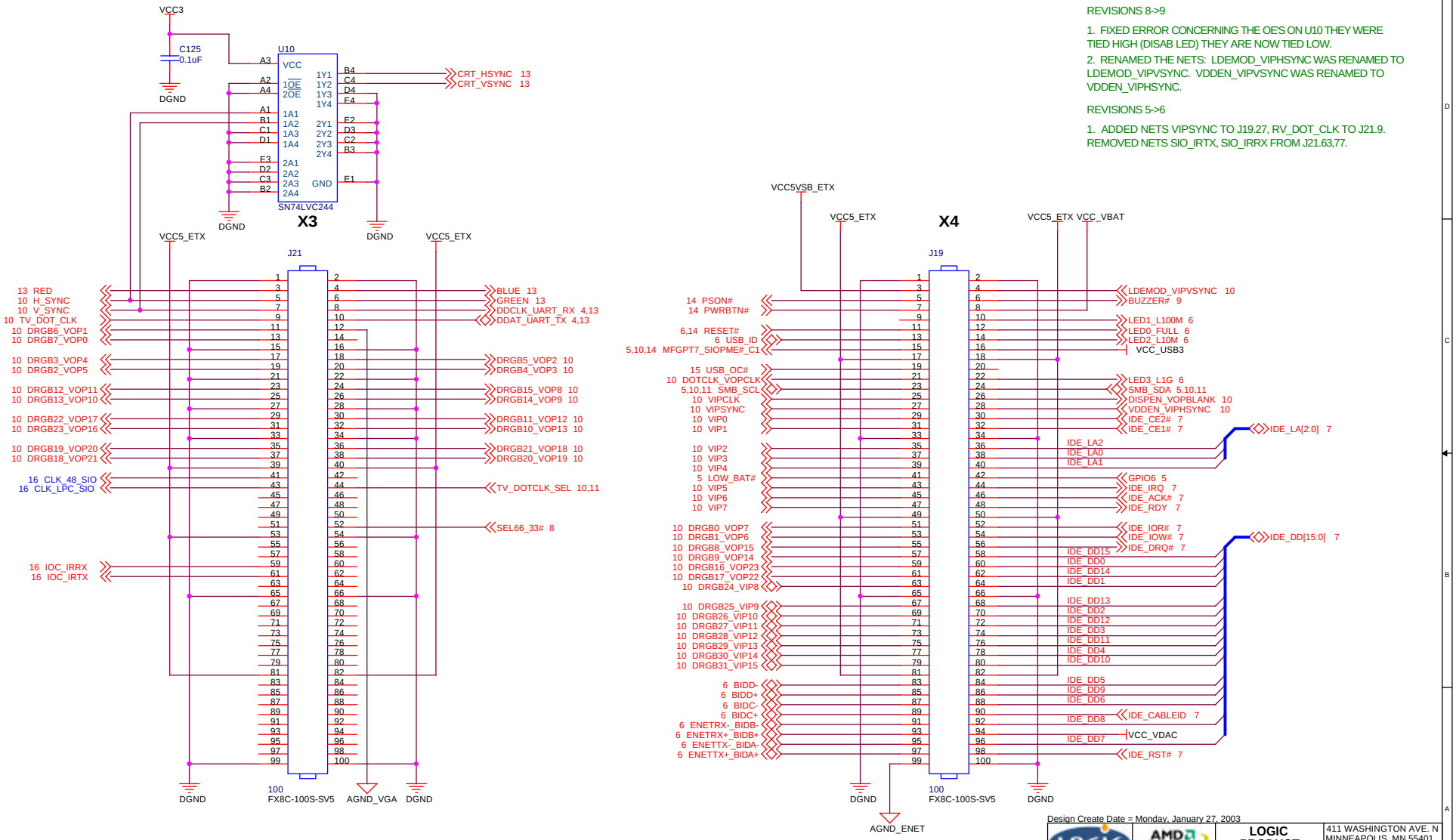

REVISIONS 8->9

1. FIXED ERROR CONCERNING THE OE'S ON U10 THEY WERE TIED HIGH (DISAB LED) THEY ARE NOW TIED LOW.
2. RENAMED THE NETS: LDEMOD_VIPHSYNC WAS RENAMED TO LDEMOD_VIPVSYNC. VDDEN_VIPVSYNC WAS RENAMED TO VDDEN_VIPHSYNC.

REVISIONS 5->6

1. ADDED NETS VIPSYNC TO J19.27, RV_DOT_CLK TO J21.9. REMOVED NETS SIO_IRTX, SIO_IRRX FROM J21.63,77.

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Reference Designator to Schematic Cross List

Format: REFDES PAGE:X.Y VALUE

BT

BT1	14:4.B	CR2032 HOLD‡
BT2	14:4.B	BR2032

BZ

BZ1	9:2.B	DET801H

C

C2	13:5.C	4.7PF
C3	13:4.C	4.7PF
C4	13:4.C	4.7PF
C5	13:4.C	4.7PF
C6	13:4.C	4.7PF
C7	13:3.C	4.7PF
C8	14:1.C	33PF
C9	13:2.C	0.1UF
C10	13:3.B	0.1UF
C11	14:3.D	47UF
C12	14:3.D	22UF
C14	14:3.D	22UF
C15	14:5.D	22UF
C16	14:5.D	22UF
C17	14:5.D	47UF
C19	14:4.C	22UF
C20	14:4.C	0.1UF
C21	14:3.C	0.1UF
C22	14:3.C	22UF
C23	14:3.B	0.1UF
C24	7:5.D	22UF
C25	7:4.D	0.1UF
C26	7:3.A	47000pF
C27	6:3.D	0.1UF
C28	6:3.D	10000PF
C36	15:4.D	0.1UF
C38	15:3.C	150UF
C39	15:3.C	10000PF
C40	15:3.C	150UF
C41	15:2.C	10000PF
C42	15:4.C	0.1UF
C43	6:2.A	220PF
C44	15:3.B	150UF
C45	15:3.B	10000PF
C46	15:3.B	150UF
C47	15:3.B	10000PF
C53	8:2.D	0.1UF
C54	8:2.D	0.1UF
C55	8:1.D	0.1UF
C56	8:1.D	0.1UF
C57	8:1.D	0.1UF
C58	8:1.D	0.1UF
C59	8:5.D	0.1UF
C60	8:5.D	0.1UF
C61	8:5.D	12pF
C62	8:2.D	100UF
C63	8:2.D	100UF
C64	8:1.D	100UF
C65	8:1.D	100UF
C66	8:1.D	100UF
C67	9:4.D	470PF
C68	9:3.D	470PF
C69	9:5.D	1000PF
C70	9:5.D	1000PF
C71	9:5.C	220UF
C72	9:5.C	220UF
C73	9:4.C	470PF
C74	9:3.C	470PF
C75	9:4.B	1000PF
C76	9:4.B	22UF
C77	9:4.B	0.1UF
C80	9:5.A	220PF
C81	9:4.A	220PF
C82	9:4.A	220PF
C83	9:4.A	220PF
C84	10:2.C	22UF
C85	10:3.C	0.1UF
C88	10:1.C	0.1UF
C89	10:1.C	0.1UF
C90	11:3.D	0.1UF
C91	10:1.C	470PF
C98	4:5.D	0.1UF
C99	4:4.D	0.1UF
C100	4:4.D	0.1UF
C101	4:5.D	0.1UF
C102	4:4.D	0.1UF
C103	4:5.C	0.1UF
C105	4:4.C	0.1UF
C106	4:4.C	0.1UF
C107	4:5.C	0.1UF
C108	4:4.C	0.1UF
C109	4:3.D	220PF
C110	4:3.D	220PF
C111	4:3.D	220PF
C112	4:2.D	220PF
C113	4:2.D	220PF
C114	4:2.D	220PF
C115	4:2.D	220PF
C116	4:2.D	220PF
C117	4:3.C	220PF
C118	4:3.C	220PF
C119	4:3.C	220PF
C120	4:2.C	220PF
C121	4:2.C	220PF
C122	4:2.C	220PF
C123	4:2.C	220PF
C124	4:2.C	220PF
C125	19:5.D	0.1UF
C126	4:3.B	220PF
C127	4:3.B	220PF
C157	16:5.D	0.1UF
C158	16:4.D	0.1UF
C159	16:4.D	0.1UF
C160	16:5.D	22UF
C161	16:5.D	0.1UF
C162	16:5.D	0.1UF
C163	16:5.D	0.1UF
C164	16:5.D	0.1UF
C169	9:3.A	220PF
C170	17:4.B	180pF
C171	4:5.B	0.1UF
C172	4:4.A	0.1UF
C173	4:4.A	0.1UF
C174	4:5.A	0.1UF
C175	4:4.A	0.1UF
C176	14:1.B	33PF
C177	14:1.C	33PF

CN

CN1	17:4.B	180PF
CN2	17:4.B	180PF
CN3	17:3.B	180PF
CN4	17:2.B	180PF

D

D1	13:4.D	BAV99LT1
D2	13:4.D	BAV99LT1
D3	13:3.D	BAV99LT1
D4	14:5.B	CMD17-21VGC‡
D5	14:5.B	CMD17-21VRD‡
D6	7:2.B	CMD17-21VYD‡
D7	7:2.B	CMD17-21VYD‡
D8	6:3.B	SRV05-4
D9	9:2.B	1N4148WS-7
D10	6:2.D	BAT54TA
D11	6:2.C	BAT54TA
D12	13:3.D	BAV99LT1
D13	13:2.D	BAV99LT1
D14	13:2.D	BAV99LT1
D15	13:2.D	BAV99LT1
D16	6:4.C	SRV05-4
D17	15:2.C	CMD17-21VGC‡
D18	15:1.C	CMD17-21VGC‡
D19	15:2.C	CMD17-21VGC‡
D20	15:1.C	CMD17-21VGC‡
D21	17:4.D	MBRS340T3
D22	14:5.B	CMD17-21VRD‡
D23	14:1.B	BAT54TA

DGND

DGND2	16:5.C	T_POINT

F

F1	13:3.B	1.10A, 30V
F2	9:5.B	1.10A, 30V
F3	13:4.A	BUMPER
F4	13:4.A	BUMPER
F5	13:4.A	BUMPER
F6	13:4.A	BUMPER

FB

FB4	13:3.C	FERRITE BEAD
FB5	14:4.D	FB
FB6	14:5.D	FB
FB8	14:3.D	FB
FB9	14:5.D	FB
FB10	6:3.C	FB
FB11	6:3.C	FB
FB15	15:3.D	FB
FB16	15:3.D	FB
FB17	6:3.A	FB
FB18	6:3.A	FB
FB19	15:3.C	FB
FB20	15:3.C	FB
FB21	6:2.A	FERRITE BEAD
FB22	9:4.D	FERRITE BEAD
FB23	9:4.D	FERRITE BEAD
FB24	9:4.D	FERRITE BEAD
FB25	9:4.C	FERRITE BEAD
FB26	9:4.C	FERRITE BEAD
FB28	9:5.B	FERRITE BEAD
FB29	9:5.B	FERRITE BEAD
FB30	9:5.A	FERRITE BEAD
FB31	9:5.A	FERRITE BEAD
FB36	9:4.B	FB
FB45	16:5.D	FB
FB46	16:4.A	FB
FB47	9:3.A	FERRITE BEAD

J

J3	14:4.D	20
J4	14:3.B	3
J5	7:4.D	CF Socket T‡
J6	7:4.B	39
J7	7:2.D	3
J8	6:5.D	4
J9	6:3.D	USB DUAL TY‡
J10	6:2.B	USB Type A
J11	6:2.A	USB Mini AB
J12	8:4.D	120
J13	10:5.D	26
J14	10:5.C	14
J15	11:2.B	32
J16	10:3.B	31
J17	5:4.C	33
J18	18:4.D	100
J19	19:2.C	100
J20	5:2.C	26
J21	19:4.C	100
J22	18:2.D	100
J23	10:3.D	41
J24	4:1.C	10
J26	9:1.C	2
J29	4:1.B	10
J31	10:3.B	6
J32	5:2.C	4
J33	10:5.B	40
J36	9:3.D	15
J37	10:1.B	6
J38	10:1.D	3
J39	14:2.C	7X2

JP

JP1	14:3.B	J2(1-2)
JP2	7:2.D	SHUNT
JP4	11:3.D	JP4(1-2)
JP5	11:3.D	JP4(13-14)
JP6	11:3.D	JP4(5-6)
JP7	11:3.D	JP4(15-16)
JP15	10:2.D	J2(1-2)
JP16	11:2.D	JP4(1-2)
JP17	11:2.D	JP4(13-14)
JP18	11:2.D	JP4(1-2)
JP19	11:1.D	JP4(13-14)
JP20	11:1.D	JP4(1-2)
JP21	11:1.D	JP4(13-14)
JP22	11:2.D	JP4(5-6)
JP23	11:2.D	JP4(15-16)
JP24	11:2.D	JP4(5-6)
JP25	11:1.D	JP4(15-16)
JP26	11:1.D	JP4(5-6)
JP27	11:1.D	JP4(15-16)

L

L1	6:4.C	90 OHMS/350‡
L2	6:4.C	90 OHMS/350‡
L3	6:4.B	90 OHMS/350‡
L4	6:4.A	90 OHMS/350‡
L5	13:4.D	22NH
L6	13:4.C	22NH
L7	13:4.C	22NH

MT

MT1	13:5.B	0.125
MT2	13:4.B	0.125
MT3	13:4.B	0.125
MT4	13:3.B	0.125

P

P2	9:4.B	12
P3A	17:1.C	DB-9/DB-15/‡
P3B	4:1.D	DB-9/DB-15/‡
P3C	13:3.D	DB-9/DB-15/‡
P4	9:1.D	RCA Jack

Q

Q1	7:2.B	N-CH
Q5	9:2.B	N-CH
Q6	10:1.C	N-CH
Q8	10:1.C	N-CH
Q9	10:1.D	FDC640P
Q10	14:5.A	N-CH

R

R1	14:1.C	22
R2	14:2.C	330
R3	14:3.C	330
R4	13:1.C	0
R5	13:1.C	0
R6	13:1.C	0
R7	13:1.C	0
R8	14:1.D	22
R9	14:4.B	0
R10	14:1.B	22
R11	14:5.B	330
R12	14:5.B	330
R13	14:3.B	1.0K
R14	14:4.C	576
R15	14:4.C	931
R16	7:3.D	0
R17	7:3.D	0
R18	7:3.D	0
R19	7:5.D	10K
R20	7:3.D	0
R21	7:5.D	10K
R22	7:3.D	0
R23	7:3.D	0
R24	7:3.C	0
R25	7:3.C	0
R26	7:5.C	10K
R27	7:5.C	10K
R29	7:5.C	10K
R30	7:5.C	10K
R31	7:3.A	10K
R32	7:5.C	0
R33	7:5.C	33
R34	7:2.D	100
R35	7:2.C	330
R36	7:2.C	330
R37	7:2.C	10K
R38	7:3.B	0
R39	6:2.D	0
R40	6:2.C	0
R41	15:5.D	10K
R42	15:5.D	10K
R44	15:5.C	10K
R46	8:2.C	33
R47	8:4.A	10K
R48	8:4.A	10K
R49	8:4.A	10K
R50	8:2.C	8.25K
R51	8:2.C	8.25K
R52	8:5.B	8.25K
R53	8:2.B	8.25K
R54	9:4.D	1.0K
R55	9:4.D	1.0K
R56	9:5.D	47 K
R57	9:4.D	47 K
R58	9:4.C	47 K
R59	9:4.C	47 K
R60	9:2.B	22
R61	9:3.B	10K
R63	10:1.D	47 K
R64	10:1.D	10K
R65	11:3.D	10K
R67	11:2.B	10K
R68	11:5.B	10K
R69	11:4.B	10K
R70	11:4.B	10K
R71	11:4.B	10K
R72	11:4.B	10K
R73	11:4.B	10K
R74	11:4.B	10K
R75	11:3.B	10K
R76	11:3.B	10K
R77	11:3.B	10K
R78	11:3.B	10K
R79	11:2.B	10K
R80	11:2.B	10K
R81	11:2.B	10K
R82	11:4.D	10K
R83	11:5.D	10K
R84	11:5.D	10K
R85	11:4.D	10K
R86	11:5.D	10K
R87	11:5.D	10K
R96	10:1.C	4.7K
R98	10:3.B	0(REV)
R99	10:2.C	10K
R125	4:5.D	10K
R126	4:5.D	10K
R127	4:5.C	10K
R128	4:5.C	10K
R129	5:4.D	4.7K
R130	5:4.D	4.7K
R131	5:4.D	4.7K
R132	5:4.C	4.7K
R133	5:4.C	4.7K
R134	5:4.C	4.7K
R135	18:3.B	0
R136	18:3.B	0
R137	7:3.A	470
R153	16:1.D	4.7K
R154	16:1.D	4.7K
R155	16:1.D	4.7K
R156	16:1.D	4.7K
R162	16:1.C	4.7K
R163	16:1.C	4.7K
R164	16:1.C	4.7K
R165	16:1.C	4.7K
R166	16:1.C	4.7K
R167	16:1.C	4.7K
R168	17:2.D	2.7K
R215	15:5.D	10K
R216	15:4.D	10K
R217	15:2.C	330
R218	15:2.C	330
R219	15:1.C	330
R220	15:1.C	330
R221	15:5.C	10K
R222	15:5.C	10K
R223	15:4.C	10K
R225	9:5.B	0
R226	9:5.B	0
R227	16:1.B	0
R228	16:1.B	0
R229	16:1.B	0
R230	16:1.A	0
R231	4:5.B	10K
R232	4:5.A	10K
R233	18:5.D	0.005
R234	18:5.D	0.005
R235	13:5.C	75
R236	13:5.C	75
R237	13:5.C	75
R238	14:5.B	330
R239	9:2.B	0

RN

RN1	17:4.D	2.7K
RN2	17:3.D	2.7K
RN3	17:3.D	2.7K
RN4	17:3.D	2.7K
RN5	17:4.C	33
RN6	17:4.C	33
RN7	17:4.C	33

SW

SW1	14:1.C	SPST
SW2	14:1.D	SPST
SW3	14:1.B	SPST

TP

TP2	16:5.C	T_POINT
TP3	16:5.C	T_POINT
TP4	10:3.B	T_POINT
TP5	10:3.B	T_POINT

U

U1	14:4.C	1.5A
U2	15:4.D	MIC2026-1BM
U3	15:4.C	MIC2026-1BM
U5	11:4.D	I2C-16BIT I‡
U8	4:4.D	SP3243E
U9	4:4.C	SP3243E
U10	19:4.D	SN74LVC244
U13	16:4.D	W83627HF