AMD

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Mobile AMD Athlon™ and Mobile AMD Duron™ Processor

Power Module Design Guide

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Revision History

Date	Rev	Description
October 2000	B	Added three deliverables to Deliverables on page 3. Updated Figure 1 on page 4 to include mounting hole size and locations. Added the specification for the standoffs. In Table 2, "General Electrical Requirements," on page 7 changed the MIN specification for VCC transient tolerance at the regulator from –50 mV to –100 mV and the Current Slew Rate from 1000 A/µS to 30 A/µS. Added upper and lower thresholds from Power Good Output (PWRGD) on page 8 and voltage thresholds from ENABLE (Shutdown) REQUIRED on page 10 into Table 2. Added section on Over Voltage Protection on page 12. Added 30 W VRM information.
August 2000	A	Initial Release

Mobile AMD Athlon™ and Mobile AMD Duron™ Processor Power Module Design Guide

Overview

This document defines the guidelines for designing the DC to DC power converter CPU core power supply for the AMD "Thresher" Mobile Customer Development Platform (M–CDP). The intention is to have an interchangeable power supply module that supports both the Mobile AMD Athlon™ processor and the Mobile AMD Duron™ processor. This module must meet the power requirements for the Mobile AMD processors and support AMD PowerNow!™ Technology. For actual notebook system designs, the power supply module is likely to be integrated on the planar. This power supply module design is only intended for use with the AMD M–CDP.

Goals

The primary goal for this development is to provide AMD's OEM partners with a fully functional design that can be directly imported into a production form–factor notebook computer. This goal can be broken down as follows:

- Designs must use low profile surface mount parts suitable for a mobile computer
- Schematics and layout should be suitable for a mobile computer
- Designs should be suitable for mass production by a mobile computer equipment manufacturer
- Designs must minimize board area (maximize component density)
- Designs should utilize parts that are readily available in Taiwan/China

This design is intended for use on the AMD M–CDP designed for the Mobile AMD Athlon and Mobile AMD Duron processor product families. ODMs working on an AMD mobile solution should have the option of either copying the power module directly into their motherboard layout design or directly using the power module by placing the mating header on their design. Hence, the documents called out in the Deliverables section on page 3 are essential for minimizing ODM time–to–market.

Deliverables

The following items are considered an integral part of the total design solution and should be delivered in electronic format in addition to the actual power modules :

- Schematics and Netlist
- CAD Database
- Gerber files
- Bill of Materials complete with $100 k/month pricing
- All part specifications in PDF format
- Layout and Design Guidelines document
- Power Supply Vendor contact information
- Manufacturer contact information
- Minimum of five working modules for evaluation
- Design calculations and component stresses
- Thermal calculations or test data
- Simulations, if done

Mechanical Specifications

Dimensions

Outline dimensions should be equal to or less than 3.1–inch x 1.5–inch. Per the Goals section, this module should be made as compact as possible using commonly available parts traditionally used in notebook designs (i.e., low profile, surface mount). This module mounts horizontal (parallel) to the motherboard with a low-profile 0.05–inch pitch, 2x40 header socket. Maximum component height on the connector side of the board should be 6.0 mm. Maximum component height on the bottom side of the board should be 2.0 mm.

Corner mounting holes are recommended to accommodate the option of directly using the module in a production mobile solution. Use standoff Keystone Electronic Corporation catalog# 8816 to mount board.

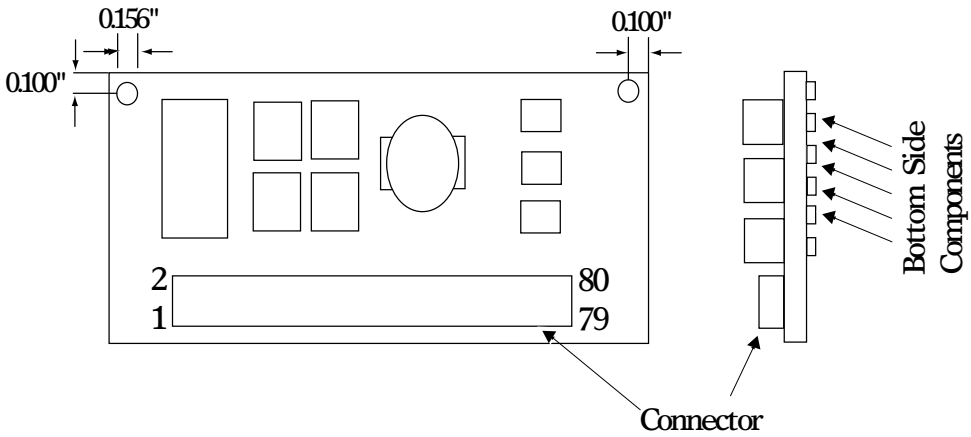

Figure 1. Sample Layout

Interconnect

Interconnect should consist of a 80 pin interface (low profile 0.05–inch, surface mount, 2x40), Berg part number 87023–640. The pin electrical interface should be as given in Table 1 on page 5.

Table 1. Module Pinout

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	COREFB*	21	V_{IN}	41	GND	61	V_{CC_OUT}
2	COREFB#*	22	V_{IN}	42	GND	62	V_{CC_OUT}
3	GND	23	V_{IN}	43	GND	63	V_{CC_OUT}
4	GND	24	V_{IN}	44	GND	64	V_{CC_OUT}
5	PWRGD	25	V_{IN}	45	GND	65	V_{CC_OUT}
6	ENABLE	26	V_{IN}	46	GND	66	V_{CC_OUT}
7	VID0	27	5 V_{IN}	47	GND	67	V_{CC_OUT}
8	VID1	28	5 V_{IN}	48	GND	68	V_{CC_OUT}
9	VID2	29	5 V_{IN}	49	GND	69	V_{CC_OUT}
10	VID3	30	5 V_{IN}	50	GND	70	V_{CC_OUT}
11	VID4	31	5 V_{IN}	51	GND	71	V_{CC_OUT}
12	GND	32	5 V_{IN}	52	GND	72	V_{CC_OUT}
13	GND	33	5 V_{IN}	53	GND	73	V_{CC_OUT}
14	GND	34	3 V_{IN}	54	GND	74	V_{CC_OUT}
15	GND	35	3 V_{IN}	55	GND	75	V_{CC_OUT}
16	GND	36	3 V_{IN}	56	GND	76	V_{CC_OUT}
17	GND	37	3 V_{IN}	57	GND	77	V_{CC_OUT}
18	GND	38	3 V_{IN}	58	GND	78	V_{CC_OUT}
19	GND	39	3 V_{IN}	59	V_{CC_OUT}	79	V_{CC_OUT}
20	GND	40	3 V_{IN}	60	V_{CC_OUT}	80	V_{CC_OUT}

Note:
** COREFB is the remote sense (+) and COREFB# is the remote sense (–)*

Mating Header on Motherboard

The motherboard header is an 80–pin, 40x2, shrouded header with 0.05–inch centers, reference Berg part number 90098–140 or equivalent.

Weight

Package weight should be no more than 3.0 ounces.

Electrical Specifications

The following conditions apply to the specifications:

- Icc is measured at nominal Vcc under maximum signal loading conditions.
- Note that these values are for reference only. Refer to the processor data sheet for updated values.

Recommended references:

- *AMD Athlon™ Processor Voltage Regulator Design Application Note*, order# 22651
- *AMD Athlon™ Processor Data Sheet*, order# 21016
- *Mobile AMD Duron™ and Mobile AMD Duron™ Processor System Requirements*, order# 24106
- *Mobile AMD Duron™ Processor Model 3 Data Sheet*, order# 23979
- *Mobile AMD Athlon™ Processor Model 6 Data Sheet*, order# 24319
- *Mobile AMD Duron™ Processor Model 7 Data Sheet*, order# 24068

General Converter Requirements

A DC to DC power converter design that can be used with a Mobile AMD Athlon or Mobile AMD Duron processor–based notebook will meet all of the requirements specified in this section. A general block diagram of the inputs and outputs of this converter is given in Figure 2.

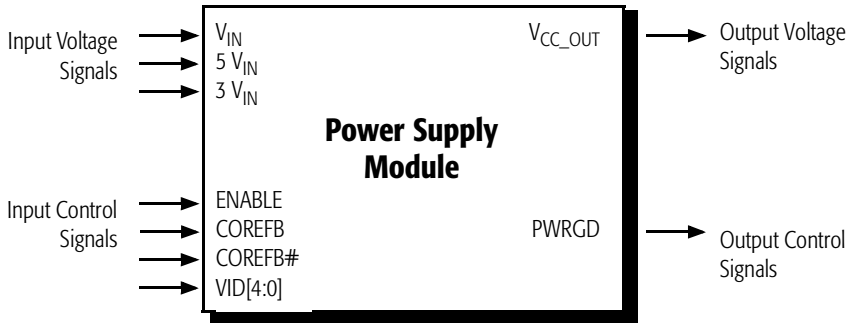

Figure 2. Logic Symbol Diagram

The power supply module must provide the maximum specified value of continuous current for the voltage range specified in Table 2. The power module should be optimized for this operating voltage range, but should still support the full voltage range shown in Table 2. A two phase solution is recommended for driving this current level while maintaining the desired efficiency using standard mobile components.

Table 2. General Electrical Requirements

	Description	Min	Typical	Max	Comments
V_{CC}	V_{CC_OUT} for the Mobile AMD Athlon and Mobile AMD Duron processors	1.0 V	1.4 V	1.5 V	Note 1
	Vcc static tolerance at the regulator	–0.050 V		+0.050 V	
	Vcc transient tolerance at the regulator	–0.100 V		+0.100 V	
I_{CC}	Icc for the processor @ 24 W	0.25 A		18.14 A	Note 2
I_{CC}	Icc for the processor @ 30 W	0.25 A		23.8 A	Note 2
$dI_{CC/dt}$	Current Slew rate			30 A/µs	
V_{In}	Input Voltage	6.0 V	12.0 V	24.0 V	
Eff_{min}	Efficiency of the regulator at minimum load	80%			
Eff_{max}	Efficiency of the regulator at maximum load	90%			
Temp	Operating temperature range	0° C		70° C	
PWRGD	Output voltage good signal threshold	0.800 V	0.850 V	0.900 V	Note 3
ENABLE	Power supply enable signal threshold	0.8 V		2.0 V	

Notes:

1. *The nominal core voltage, Vcc, for processors with frequencies of 1 GHz or greater is TBD.*
2. *The DC to DC converter supplies the Mobile AMD Athlon and Mobile AMD Duron processor core voltage and the AMD System Bus interface driver voltage on the Northbridge. Thus, the Northbridge current consumption is factored into the maximum current specification.*
3. *This signal must not assert until after the output voltage passes the threshold and stays above that threshold for a minimum of 10 ms.*

Table 3 is a description of the output signals.

Table 3. Output Voltage Signals

Signal	Description
V_{CC_OUT}	Variable voltage out (powers CPU)
PWRGD	Power good indicator

Static Voltage Regulation

The output voltage must be within the static range specified in Table 2 on page 7 when measured at the processor pins except during initial power–on and final power–off. Static voltage regulation includes the following:

- DC output initial voltage set point adjust
- Output ripple and noise
- Output load ranges specified in tables above
- Temperature range specified including warm up time

Transient Voltage Regulation

The output voltage must be within the transient range specified in Table 2 on page 7 when measured at the processor pins except during initial power-on and final power-off. This tolerance must include the variation due to static voltage regulation plus the effects of the output load transient at the module output pins. The module must remain within the transient range specified during VID transitions.

Turn–On Response Time

The output voltage should be within its specified range within 10 ms of the input reaching 95% of its nominal voltage.

Overshoot at Power-On and Power-Off

Overshoot upon the application or removal of the input must be less than 10% above the initial set output voltage. No negative voltage may be present on any output during power-on or power-off.

Output Control Signals

Power Good Output (PWRGD)

The Power Good output, PWRGD, is required and implemented at the system level, not on the module. The "Thresher" motherboard provides its own PWRGD circuit for the processor core voltage, therefore the PWRGD output from the power supply module is not used on the Thresher motherboard. A PWRGD indication for the processor core voltage is required at the system level for Mobile AMD Athlon and Mobile AMD Duron processor–based systems.

If the DC to DC power converter does not provide this directly, the motherboard designer must provide a PWRGD circuit for the processor core voltage external to the DC to DC power converter. The following description of the PWRGD signal is provided for the reference of the DC to DC power converter manufacturer in case they desire to integrate the processor core

voltage PWRGD functionality required for Mobile AMD Athlon and Mobile AMD Duron processor–based systems:

PWRGD is an open collector signal consistent with TTL DC specifications. This signal provides the Power Good indication for the core voltage. Refer to Table 2, "General Electrical Requirements," on page 7 for the recommended threshold voltage levels used to determine the Power Good status of the core voltage. If the core voltage is stabilized above the threshold voltage defined for the PWRGD signal, the PWRGD signal is asserted (open state). If the core voltage falls below the specified threshold voltage, the PWRGD signal is deasserted (low impedance to GND).

The PWRGD signal will assert only after the following two conditions are met:

1. The output voltage must rise above the threshold given in Table 2, "General Electrical Requirements," on page 7.
2. The output voltage must stay above this threshold for a minimum of 10 ms, which allows the output to reach the VID-defined voltage before PWRGD is asserted.

The PWRGD signal must not deassert based on VID[4:0] forced voltage transitions. Using a PWRGD output that deasserts during VID[4:0] forced voltage transitions will cause a system reset.

Input Voltage

The input voltage to the module is typically 12.0 V ±5% from a standard ATX power supply or a variable voltage (i.e., from a notebook brick supply or battery). However the input voltage may traverse the range of 6 V up to 22 V. The DC plug source voltage for the OEM systems has not been defined, so it is important that the power supply module support variable input voltages within this specified range. The power supply module must also maintain the specified output voltage degree of regulation during a step change in input voltage. A step change in input voltage can occur, for instance, when the AC adapter is inserted into a notebook that is running on a low battery.

Alternatively, the power module may derive the CPU voltage from the regulated 5 V and 3.3 V system supplies.

Table 4. Input Voltage Signals

Signal	Description	Min	Typical	Max
V_{IN}	Variable voltage in (ATX 12 V, BATT, or DC plug)	6 V	12 V	22 V
5 V_{IN}	Regulated 5 V input		5 V	
3 V_{IN}	Regulated 3.3 V input		3.3 V	

Input Control Signals

ENABLE (Shutdown) REQUIRED

The module should accept an active high input which turns the supply on and off. A logical high state should turn the supply on.

COREFB/COREFB# Sense REQUIRED

Full–differential sense is required in the power supply module design. The power supply module feedback that is connected to the COREFB/COREFB# signals can be used to ensure that the core voltage supplied to the processor is within the specified limits.

VID Inputs REQUIRED

A five bit signal, VID[4:0] should determine the output voltage of the module. These signals have an open–ground pattern. The module may use pull–up resistors to pull these signals up to TTL levels. Pull–up resistors should have a resistance ≥10 kohm. Table 5 on page 11 lists the appropriate output voltage for each valid VID combination. The module must support dynamic VID

switching. The Vcc output must reach the new voltage within 100 µs when VID[4:0] inputs dictate a voltage transition from a lower voltage to a higher voltage. For example, a transition from 1.0 V to 1.5 V must complete within 100 µs from the time VID[4:0] inputs transitioned to select 1.5 V. Transitions from higher voltages to lower voltages do not have this requirement because the processor can be operating at a lower frequency before the voltage drops to the new level.

Any overshoot or undershoot on the Vcc output during a VID change should be within the Vcc transient tolerance defined in Table 2 on page 7. VID codes are defined in Table 5.

Table 5. Voltage Identification (VID) Code

VID[4:0]	VCC_CORE (V)	VID[4:0]	VCC_CORE (V)
00000	2.000	10000	1.275
00001	1.950	10001	1.250
00010	1.900	10010	1.225
00011	1.850	10011	1.200
00100	1.800	10100	1.175
00101	1.750	10101	1.150
00110	1.700	10110	1.125
00111	1.650	10111	1.100
01000	1.600	11000	1.075
01001	1.550	11001	1.050
01010	1.500	11010	1.025
01011	1.450	11011	1.000
01100	1.400	11100	0.975
01101	1.350	11101	0.950
01110	1.300	11110	0.925
01111	Shutdown	11111	Shutdown

Notes:

These are nominal voltages, not maximums or minimums. The actual expected voltage range expected is given in Table 2, "General Electrical Requirements," on page 7. However, the power supply must be able to support this range of outputs at full load.

0 = Low, GND

1 = High, Vcc

Remote Sensing

The COREFB/COREFB# signals will be routed differentially and connected directly to the processor's FB+/FB– pins. The COREFB/COREFB# signals can be used to ensure that the core voltage supplied to the processor is within the specified limits.

Protection

The features outlined in this section should be built into the power module to prevent damage to the module itself or the motherboard.

Over Current Protection

The power supply module should measure the CPU current draw and should shut down if the current exceeds 27 A for a period of greater than 1 ms. This current limit set point must be adjustable.

The over current protection must not activate during a VID[4:0] forced voltage transition.

Over Voltage Protection

In the event the output voltage exceeds a value of 2.35 V, the upper FET will be switched off and the lower FET will be switched on to pull down the output.

Short Circuit Protection

The module should be capable of withstanding a short circuit condition without causing damage to the unit or the motherboard, and remain off until input power is cycled.

Protective Shutdown

If the power supply module shuts down due to one of the above fault conditions, it should remain latched off until the power is cycled off and on. The power supply module should not automatically return to normal operation after a fault condition.

Electromagnetic

Design, including materials, should be consistent with the manufacture of units that comply with the limits of FCC Class B and VDE 243 Level B for radiated emissions, given the existence of an external package around the module with 20 dB of shielding.

Safety

Design, including materials, should be consistent with the manufacture of units that meet the standards of UL flammability specifications per 94V–0.