AMD Socket AM2 with AMD M690T Chipset Reference Schematic

NOTES:

1) This schematic supports the AMD Socket AM2 CPU devices.
2) These are "Reference Schematics" and as such they have not been verified by an actual board build.
3) This reference schematic supports AMD M960T revision A12 or later. If A12 or later revision is not used, please see your customer support representative for the necessary application notes for workarounds.
4) This reference schematic supports SB600 revision A21 or later. If A21 or later revision is not used, please see your customer support representative for the necessary application notes for workarounds.
5) Unless otherwise specified, resistors have 5% tolerance.
6) Unless otherwise specified, capacitors have 20% tolerance.

IMPORTANT NOTICE:

1. THIS DOCUMENT MAY NOT REFLECT THE MOST RECENT CHANGES IN BOARD DEVELOPMENT AND DEBUG. ANY DEVELOPER INTENDING TO USE THIS SCHEMATIC AS A REFERNCE SHOULD CONTACT THEIR LOCAL FIELD APPLICATIONS ENGINEER, REGIONAL SALES OFFICE, OR PROGRAM MANAGER FOR SCHEMATIC UPDATES, DESIGN RECOMMENDATIONS AND PCB LAYOUT GUIDELINES. AMD ALSO RECOMMENDS A DESIGN REVIEW OF BOTH THE SCHEMATIC DIAGRAM AND PCB LAYOUT BEFORE CONSIDERING PRODUCTION.

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DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

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Cover page

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REVISION HISTORY:

REV	DATE	NOTES
0.5	04/20/2007	Preliminary release

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Revision History

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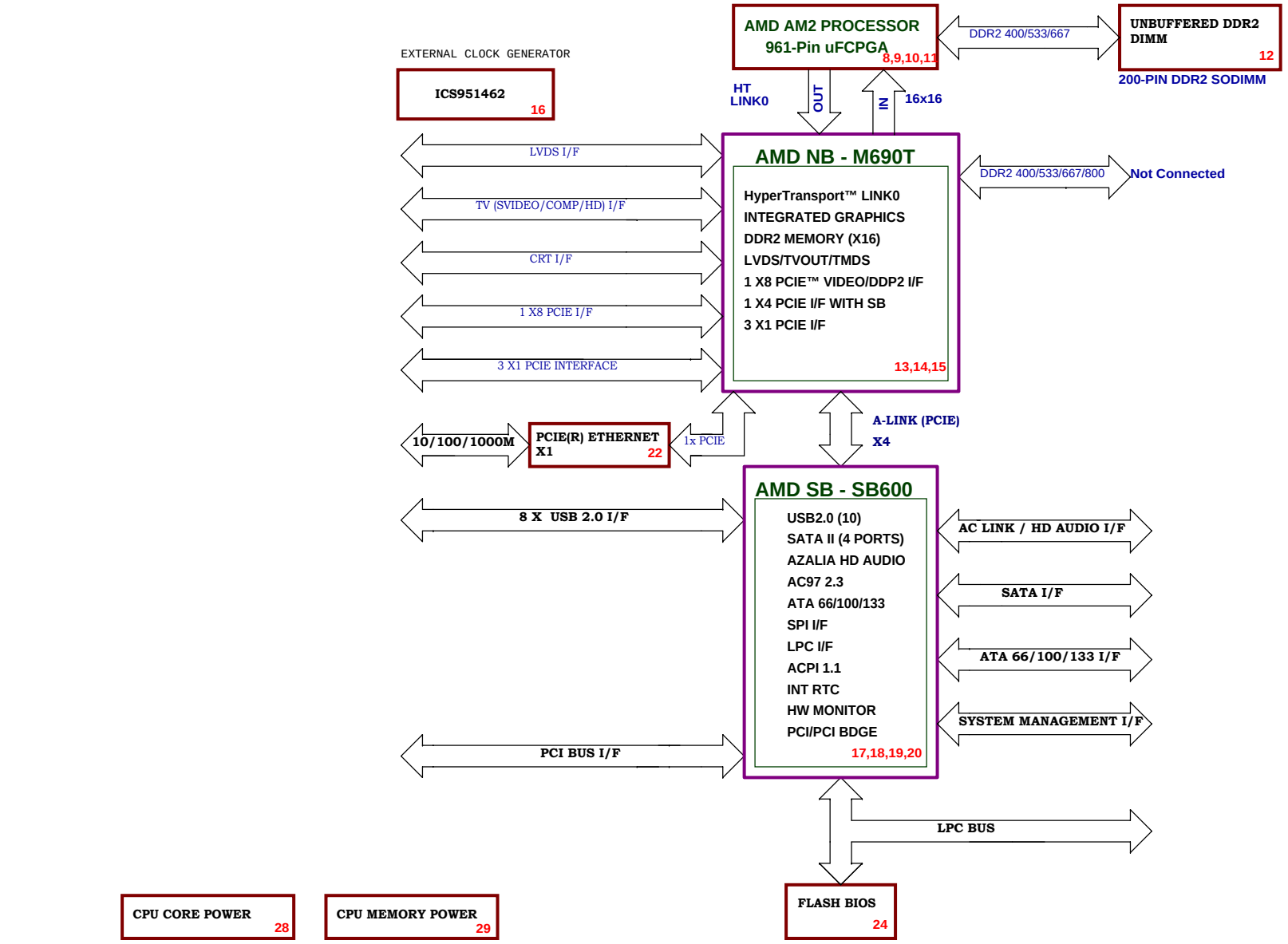
REFERENCE DESIGN FOR SOCKET S1 / M690T / SB600



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Block Diagram

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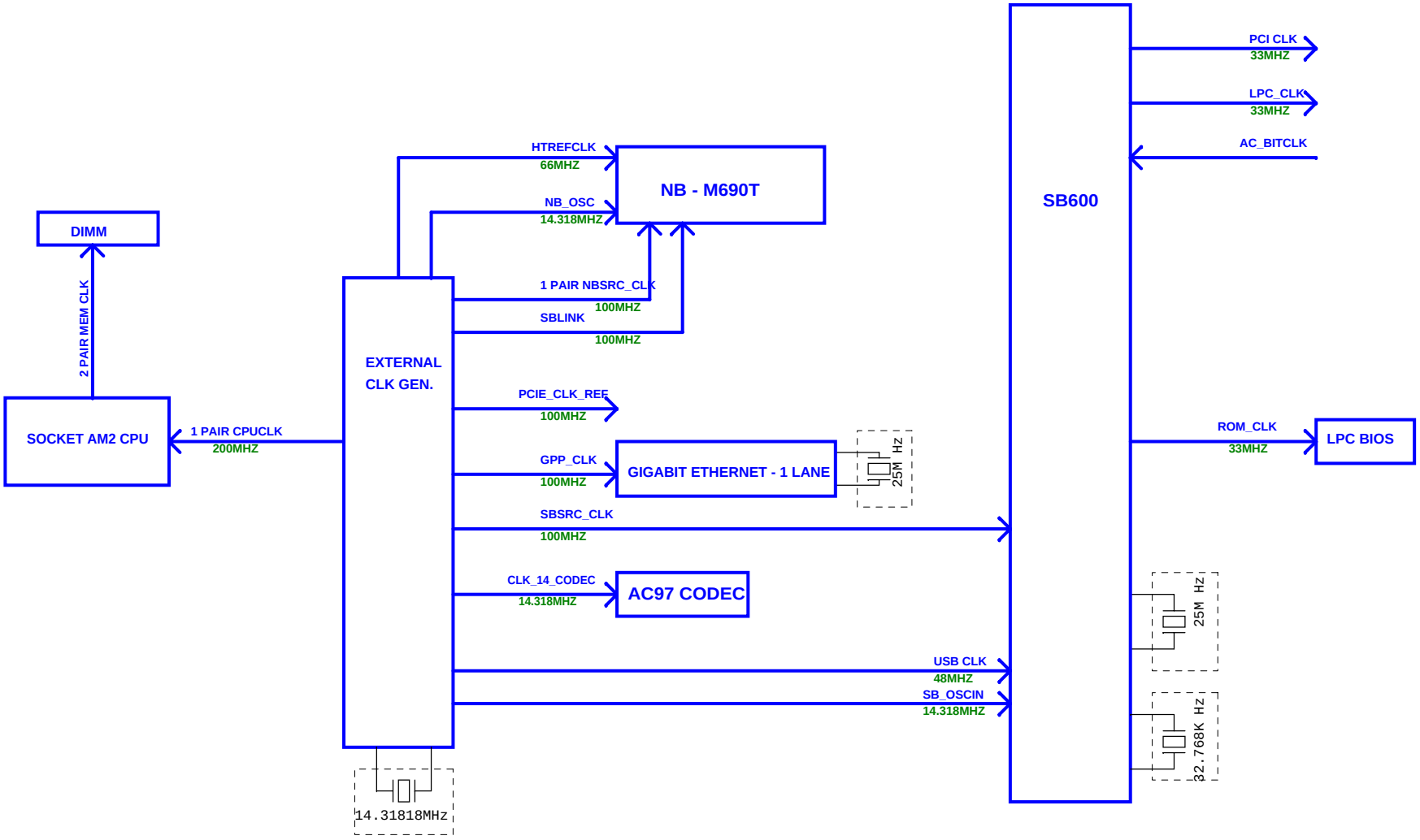

Clock Structure

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	POWER RAIL SOURCE NET	V (NET NAME)	S0	S1	S3	S4	S5
INPUT VOLTAGE	VCC_12V	+12V	ON	ON	OFF	OFF	OFF
SYSTEM POWER	VCC3P3V_ALW	+3.3V	ON	ON	ON	ON	ON
	VCC1P2V_ALW	+1.2V	ON	ON	ON	ON	ON
	VCC3P3V_DUAL	+3.3V	ON	ON	ON	ON	ON
	VCC5V	+5V	ON	ON	OFF	OFF	OFF
	VCC3P3V	+3.3V	ON	ON	OFF	OFF	OFF
CPU	CPU_VDD_RUN	VID[5:0]	ON	ON	OFF	OFF	OFF
	VCC1P2V	+1.2V	ON	ON	OFF	OFF	OFF
	CPU_VDDA_RUN	+2.5V	ON	ON	OFF	OFF	OFF
CPU & MEMORY	CPU_VDDIO_SUS	+1.8V	ON	ON	ON	OFF	OFF
	CPU_M_VREF_SUS	+0.9V	ON	ON	ON	OFF	OFF
	MEM_M_VREF_SUS	+0.9V	ON	ON	ON	OFF	OFF
	CPU_VTT_SUS	+0.9V	ON	ON	ON	OFF	OFF
RS690T	VCC1P2V_NB	+1.2V (VDDC)	ON	ON	OFF	OFF	OFF
	VCC1P2V	+1.2V (VDDA_12)	ON	ON	OFF	OFF	OFF
	VCC1P2V	+1.2V (VDD_HT)	ON	ON	OFF	OFF	OFF
	VCC1P2V	+1.2V (VDDPLL)	ON	ON	OFF	OFF	OFF
	VCC1P2V	+1.2V (PLLVDD12)	ON	ON	OFF	OFF	OFF

	POWER RAIL SOURCE NET	V (NET NAME)	S0	S1	S3	S4	S5
RS690T	VCC1P8V	+1.8V (PLLVDD18)	ON	ON	OFF	OFF	OFF
	VCC1P8V	+1.8V (LVDDR18,LPVDD)	ON	ON	OFF	OFF	OFF
	VCC1P8V	+1.8V (VDD_18)	ON	ON	OFF	OFF	OFF
	VCC1P8V	+1.8V (HTPVDD)	ON	ON	OFF	OFF	OFF
	VCC1P8V	+1.8V (AVDDI)	ON	ON	OFF	OFF	OFF
	VCC1P8V	+1.8V (AVDDQ)	ON	ON	OFF	OFF	OFF
	VCC3P3V	+3.3V (VDDR3,LVDDR33)	ON	ON	OFF	OFF	OFF
	VCC3P3V	+3.3V (AVDD)	ON	ON	OFF	OFF	OFF
SB600	VCC1P2V_SB	+1.2V (VDD)	ON	ON	OFF	OFF	OFF
	VCC1P2V_SB	+1.2V(PCIE_PVDD)	ON	ON	OFF	OFF	OFF
	VCC1P2V_SB	+1.2V(PCIE_VDDR)	ON	ON	OFF	OFF	OFF
	VCC1P2V_SB	+1.2V(PLLVDD_SATA)	ON	ON	OFF	OFF	OFF
	VCC1P2V_SB	+1.2V(AVDD_SATA)	ON	ON	OFF	OFF	OFF
	VCC1P2V_SB	+1.2V (AVDDCK_1.2V)	ON	ON	OFF	OFF	OFF
	VCC1P2V_ALW	+1.2V (S5_1.2V)	ON	ON	ON	ON	ON
	VCC1P2V_ALW	+1.2V(USN_PHY_1.2V)	ON	ON	ON	ON	ON
	VCC3P3V_DUAL	+3.3V (AVDDC)	ON	ON	ON	ON	ON
	VCC3P3V	+3.3V(XTLVDD_SATA)	ON	ON	OFF	OFF	OFF
	VCC3P3V	+3.3V (VDDQ)	ON	ON	OFF	OFF	OFF
	VCC3P3V	+3.3V (AVDD)	ON	ON	OFF	OFF	OFF
	VCC3.3V_ALW	+3.3V (S5_3.3V)	ON	ON	ON	ON	ON
	VCC3P3V_DUAL	+3.3V (AVDDTX_RX)	ON	ON	ON	ON	ON
	VCC3P3V	+3.3V (AVDDCK_3.3V)	ON	ON	OFF	OFF	OFF
	VCC1P8V	+1.8V (CPU_PWR)	ON	ON	OFF	OFF	OFF
	VCC5V	+5V (V5_VREF)	ON	ON	OFF	OFF	OFF

POWER ON SEQUENCING REQUIREMENT BY PARTS

CPU

PIN(BALL): VDDIO & VTT & VDDA -> VDD -> VLDT

NET NAME: CPU_VDDIO_SUS & CPU_VTT_SUS & CPU_VDDA_RUN -> CPU_VDD_RUN -> VCC1P2V

RS690T

PIN(BALL): 3.3V (VDDR3, LVDDR33, AVDD) -> 1.8V DISIPLAY AND PLL(PLLVDD18, IOPLLVDD18, LVDDR18D, LPVDD, AVDDI, AVDDQ, HTPVDD, VDD_18) --> 1.8V MEMORY(VDD_MEM) -> 1.2V PLL (PLLVDD12, IOPLLVDD12) -> 1.2V VDD

NET NAME: VCC3P3V (VDDR3, LVDDR33, AVDD) -> VCC1P8V (PLLVDD18D, IOPLLVDD18, LVDDR18D, LPVDD, AVDDDI, AVDDQ, HTPVDD, VDD_18) --> MEM_VDDQ (VDD_MEM) -> VCC1P2V (PLLVDD12, IOPLLVDD12) -> VCC1P2V_NB

THERE ARE NO SPECIFIC REQUIREMENTS FOR THE FOLLOWING 1.2V RAILS: VDD_HT, VDDA_12, AND VDD_PLL

SB600

THERE ARE NO SPECIFIC POWER SEQUENCING REQUIREMENTS OTHER THAN 5V VREF AND VDDQ. VDDQ(3.3V) MUST NOT EXCEED V5_VREF BY MORE THAN 0.6V AT ANY TIME DURING RAMP UP, STEADY STATE, OR RAMP DOWN.

NET NAME: VCC5V, VCC3P3V -> VCC1P2V_SB

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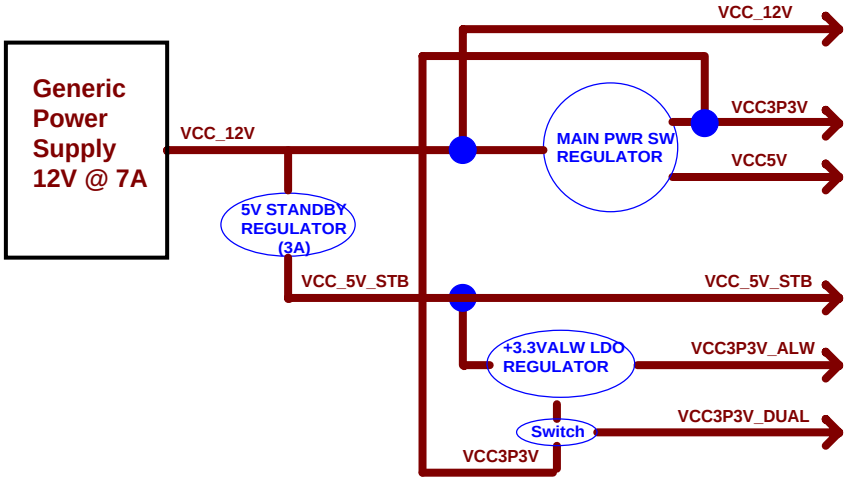
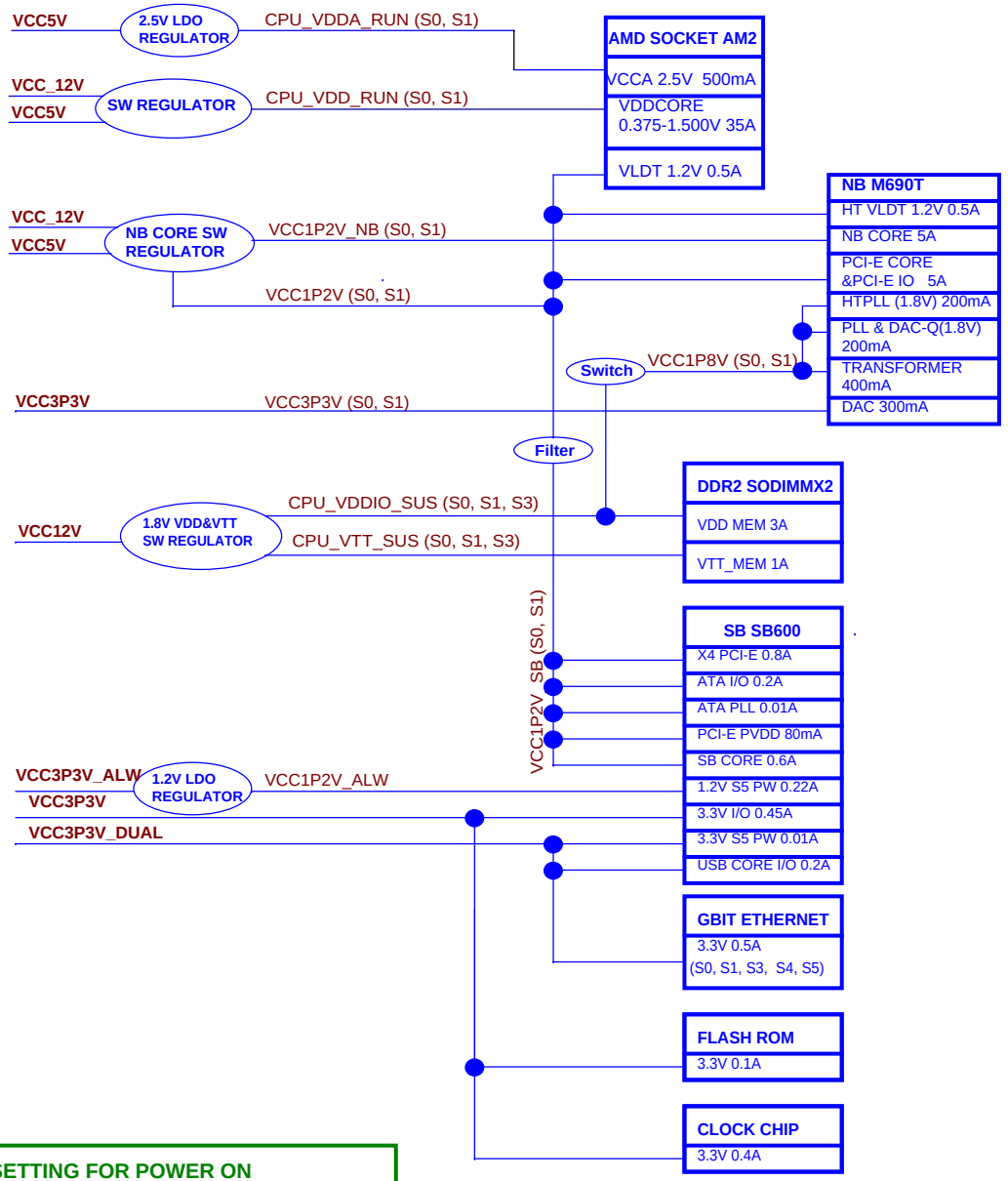
Power Configuration (1)





PCI DEVICES IRQ TABLE

DEVICE	IDSEL#	REQ/GNT#	PCI INT	CLOCK
M690T VGA	N/A	N/A	A	
SB600	AD31(INT)	N/A	N/A	
ATA	AD31	N/A	A	INT
AC97/HD	AD31	N/A	B	INT
USB	AD30	N/A	D	INT

SMBUS TABLE

SOURCE	BALL(PIN) NAME	LINKED DEVICES
M690T	DACSCL/DACSDA	CRT
	I2C_CLK/I2C_DATA	LVDS
SB600	SCL0/SDA0	SO-DIMM / CLK_GEN / THERM_SENSOR
	SCL1/SDA1	GBIT ETHERNET

DEFAULT JUMPER SETTING FOR POWER ON

JUMPER	DEF.	FUNCTION
JU5	1-2	CMOS NORMAL MODE OR CLEAR CMOS
JU7	1-2	SPI BIOS PROGRAMMING SELECTION

Power Configuration (2)

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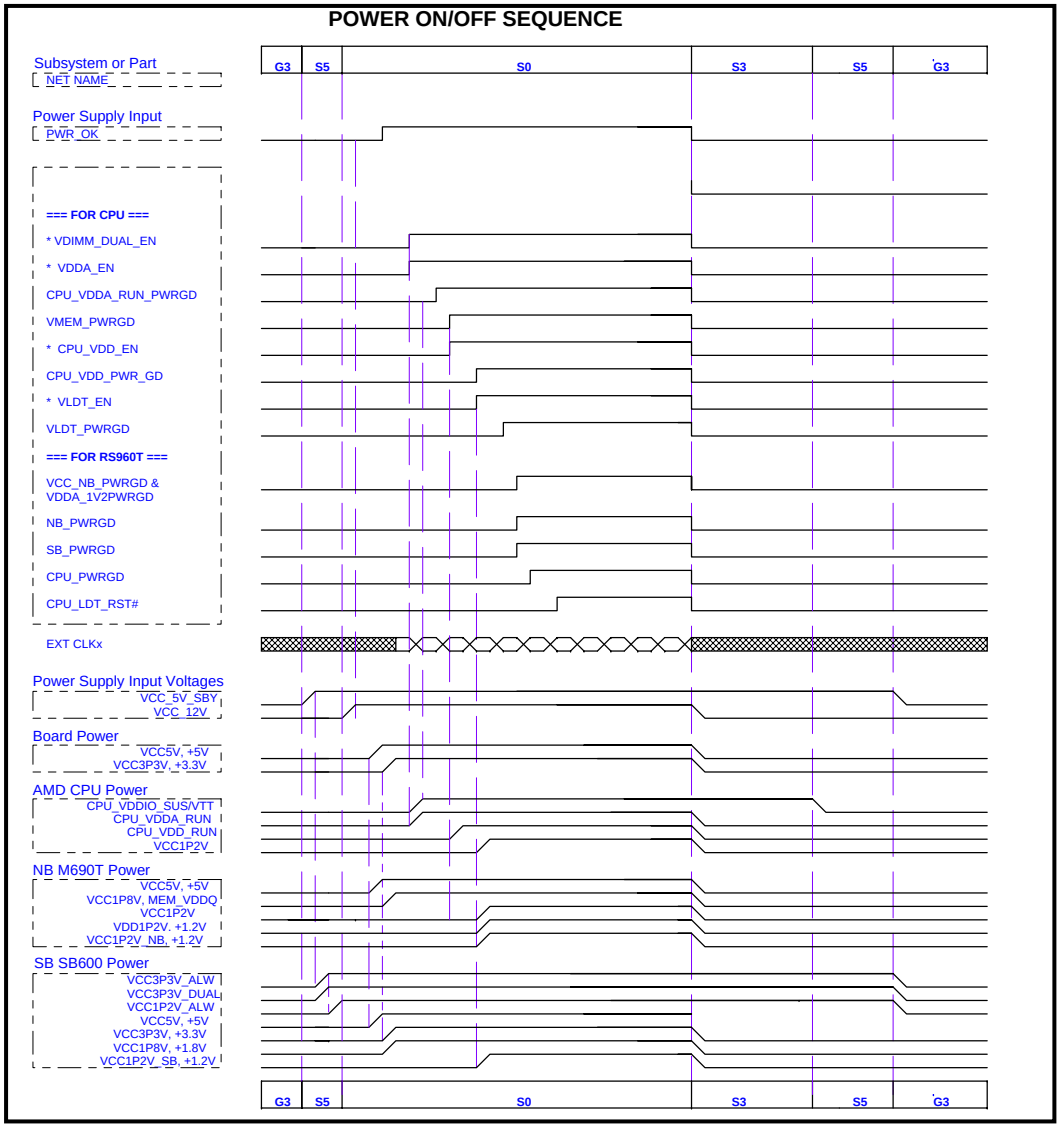
POWER ON/OFF SEQUENCE



Reset and Voltage Sequence

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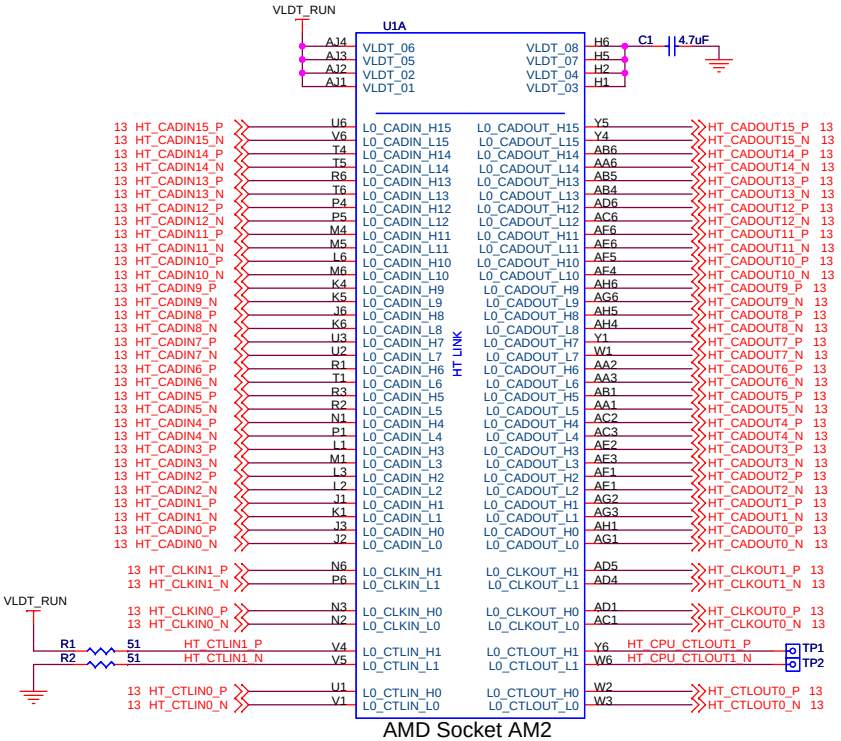
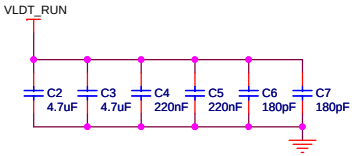
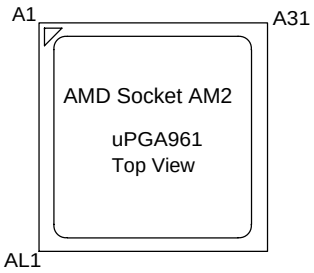
DESIGN NOTE: VLDT_Ax or VLDT_Bx can be connected to VCC1P2V. Layout considerations should decide which group is connected to VCC1P2V. If VLDT_Ax pins are connected to VCC1P2Vthen VLDT_Bx pins should be connected to a single 4.7uF CAP. Conversely, if VLDT_Bx pins are connected to VCC1P2Vthen VLDT_Ax pins should be connected to a single 4.7uF CAP.







Socket AM2 HyperTransport™ Interface

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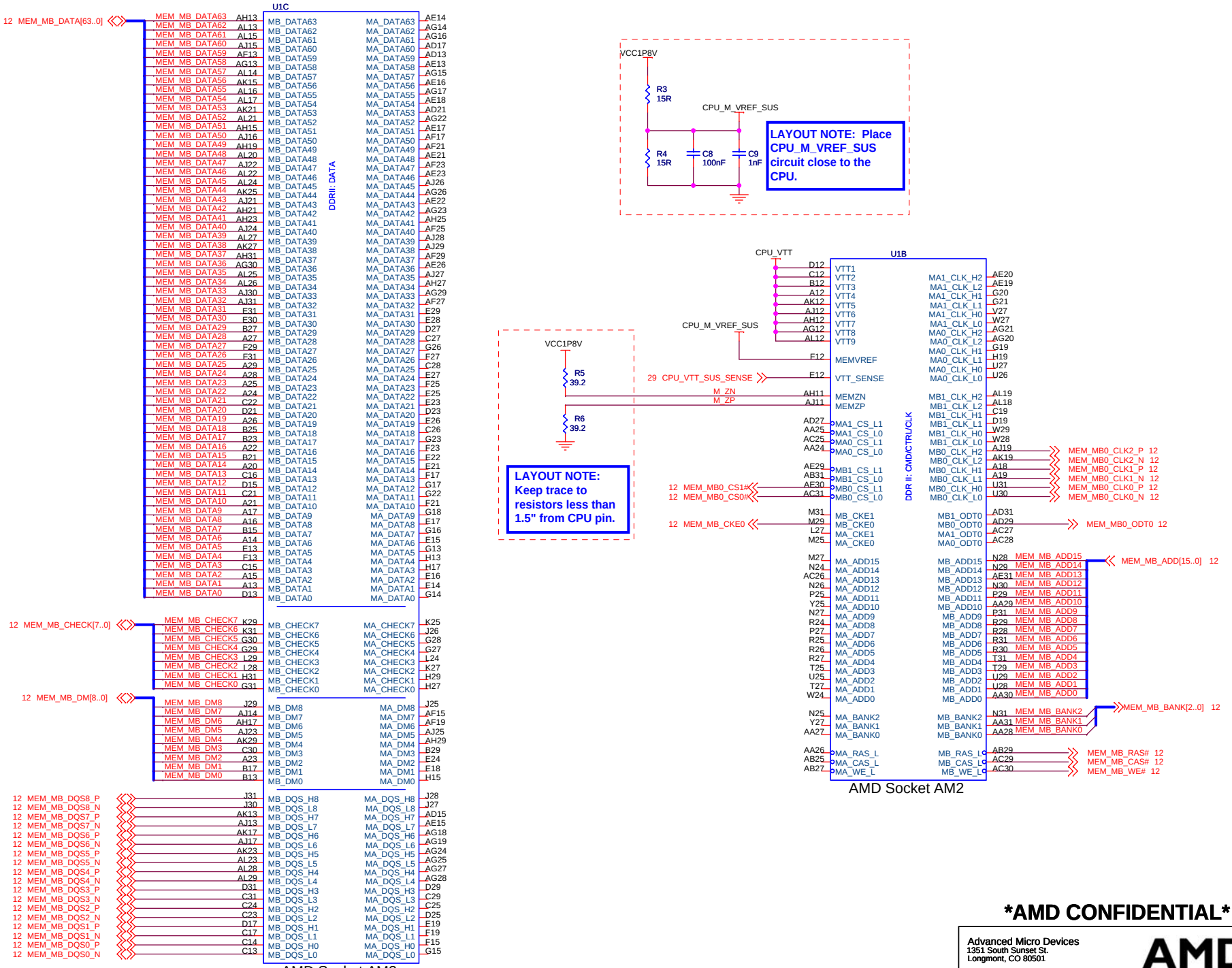

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Socket AM2 DDRII Memory Interface

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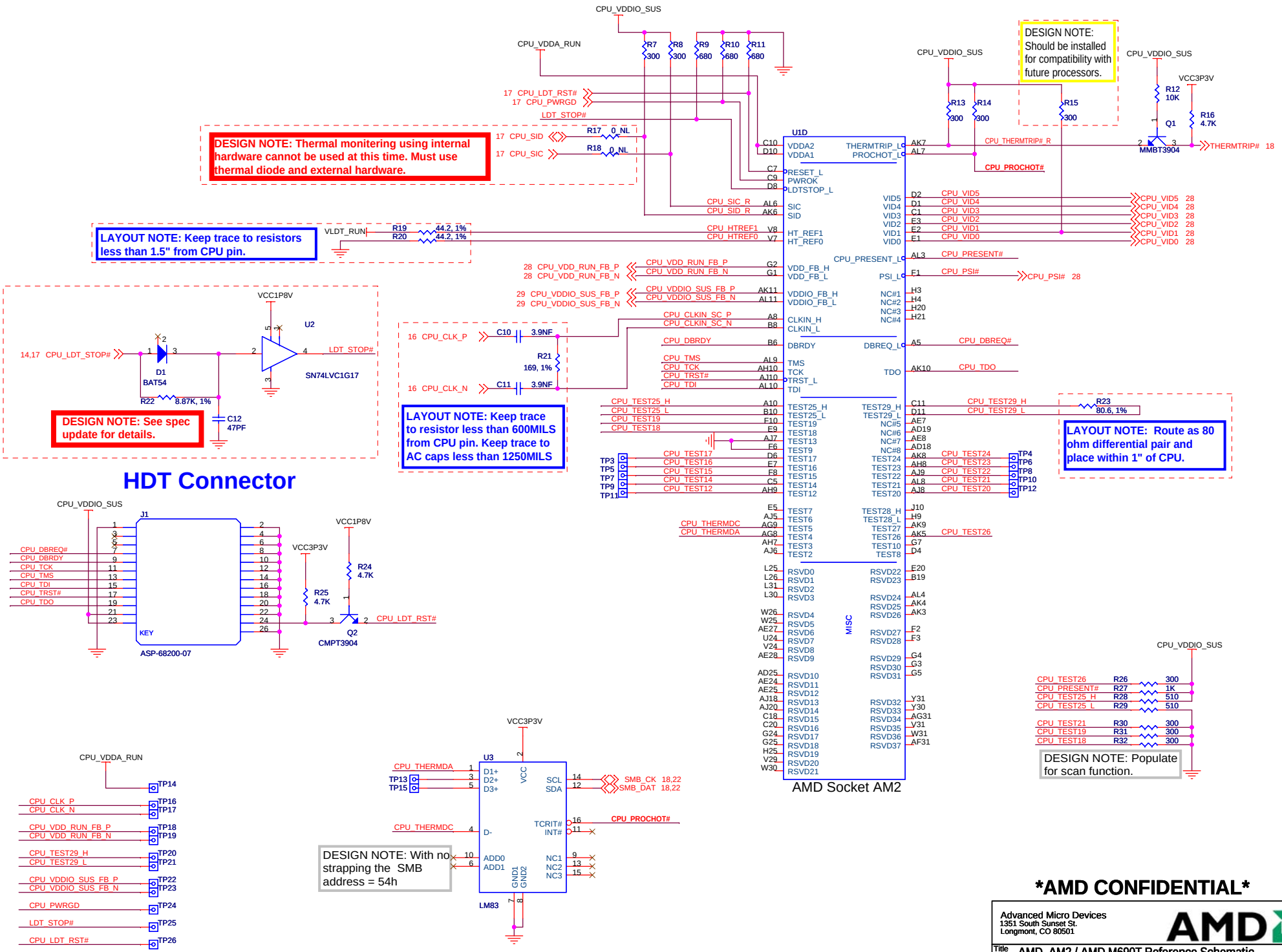
CPU_VDDIO_SUS
CPU_VDDA_RUN
R7 300
R8 300
R9 680
R10 680
R11 680
17 CPU_LDT_RST#
17 CPU_PWRGD
LDT_STOP#
17 CPU_SID
17 CPU_SIC
R17 0_NL
R18 0_NL
DESIGN NOTE: Thermal monitering using internal hardware cannot be used at this time. Must use thermal diode and external hardware.
U1D
VDDA2
VDDA1
RESET_L
PWROK
LDTSTOP_L
SIC
SID
HT_REF1
HT_REF0
THERMTRIP_L
PROCHOT_L
CPU_THERMTRIP# R
CPU_PROCHOT#
CPU_SIC_R
CPU_SID_R
CPU_HTREF1
CPU_HTREF0
VID5
VID4
VID3
VID2
VID1
VID0
CPU_VID5
CPU_VID4
CPU_VID3
CPU_VID2
CPU_VID1
CPU_VID0
CPU_PRESENT_L
CPU_PRESENT#
CPU_PSI#
CPU_PSI# 28
DESIGN NOTE: Should be installed for compatibility with future processors.
R13 300
R14 300
R15 300
VCC3P3V
R12 10K
R16 4.7K
Q1
MMBT3904
THERMTRIP# 18
LAYOUT NOTE: Keep trace to resistors less than 1.5" from CPU pin.
VLDT_RUN
R19 44.2, 1%
R20 44.2, 1%
28 CPU_VDD_RUN_FB_P
28 CPU_VDD_RUN_FB_N
CPU_VDD_RUN_FB_P
CPU_VDD_RUN_FB_N
VDD_FB_H
VDD_FB_L
29 CPU_VDDIO_SUS_FB_P
29 CPU_VDDIO_SUS_FB_N
CPU_VDDIO_SUS_FB_P
CPU_VDDIO_SUS_FB_N
VDDIO_FB_H
VDDIO_FB_L
CPU_CLKIN_SC_P
CPU_CLKIN_SC_N
CLKIN_H
CLKIN_L
CPU_DBRDY
DBRDY
DBREQ_L
CPU_DBREQ#
CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI
TMS
TCK
TRST_L
TDI
TDO
CPU_TDO
NC#1
NC#2
NC#3
NC#4
NC#5
NC#6
NC#7
NC#8
VCC1P8V
U2
14,17 CPU_LDT_STOP#
D1
BAT54
R22 8.87K, 1%
C12 47PF
SN74LVC1G17
LDT_STOP#
DESIGN NOTE: See spec update for details.
16 CPU_CLK_P
16 CPU_CLK_N
C10 3.9NF
C11 3.9NF
R21 169, 1%
LAYOUT NOTE: Keep trace to resistor less than 600MILS from CPU pin. Keep trace to AC caps less than 1250MILS
CPU_TEST25_H
CPU_TEST25_L
CPU_TEST19
CPU_TEST18
CPU_TEST17
CPU_TEST16
CPU_TEST15
CPU_TEST14
CPU_TEST12
TP3
TP5
TP7
TP9
TP11
TEST25_H
TEST25_L
TEST19
TEST18
TEST13
TEST9
TEST17
TEST16
TEST15
TEST14
TEST12
TEST7
TEST6
TEST5
TEST4
TEST3
TEST2
TEST29_H
TEST29_L
TEST24
TEST23
TEST22
TEST21
TEST20
TEST28_H
TEST28_L
TEST27
TEST26
TEST10
TEST8
CPU_TEST29_H
CPU_TEST29_L
R23 80.6, 1%
LAYOUT NOTE: Route as 80 ohm differential pair and place within 1" of CPU.
CPU_TEST24
CPU_TEST23
CPU_TEST22
CPU_TEST21
CPU_TEST20
CPU_TEST26
TP4
TP6
TP8
TP10
TP12
CPU_THERMDC
CPU_THERMDA
RSVD0
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD15
RSVD16
RSVD17
RSVD18
RSVD19
RSVD20
RSVD21
RSVD22
RSVD23
RSVD24
RSVD25
RSVD26
RSVD27
RSVD28
RSVD29
RSVD30
RSVD31
RSVD32
RSVD33
RSVD34
RSVD35
RSVD36
RSVD37
MISC
AMD Socket AM2
HDT Connector
CPU_VDDIO_SUS
J1
CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO
KEY
ASP-68200-07
VCC1P8V
VCC3P3V
R24 4.7K
R25 4.7K
Q2
CMPT3904
CPU_LDT_RST#
CPU_VDDIO_SUS
CPU_TEST26 R26 300
CPU_PRESENT# R27 1K
CPU_TEST25_H R28 510
CPU_TEST25_L R29 510
CPU_TEST21 R30 300
CPU_TEST19 R31 300
CPU_TEST18 R32 300
DESIGN NOTE: Populate for scan function.
CPU_VDDA_RUN
TP14
CPU_CLK_P
CPU_CLK_N
TP16
TP17
CPU_VDD_RUN_FB_P
CPU_VDD_RUN_FB_N
TP18
TP19
CPU_TEST29_H
CPU_TEST29_L
TP20
TP21
CPU_VDDIO_SUS_FB_P
CPU_VDDIO_SUS_FB_N
TP22
TP23
CPU_PWRGD
TP24
LDT_STOP#
TP25
CPU_LDT_RST#
TP26
CPU_THERMTRIP# R
TP27
VCC3P3V
U3
CPU_THERMDA
CPU_THERMDC
TP13
TP15
D1+
D2+
D3+
D-
VCC
SCL
SDA
SMB_CK 18,22
SMB_DAT 18,22
TCRIT#
INT#
CPU_PROCHOT#
ADD0
ADD1
NC1
NC2
NC3
GND1
GND2
LM83
DESIGN NOTE: With no strapping the SMB address = 54h
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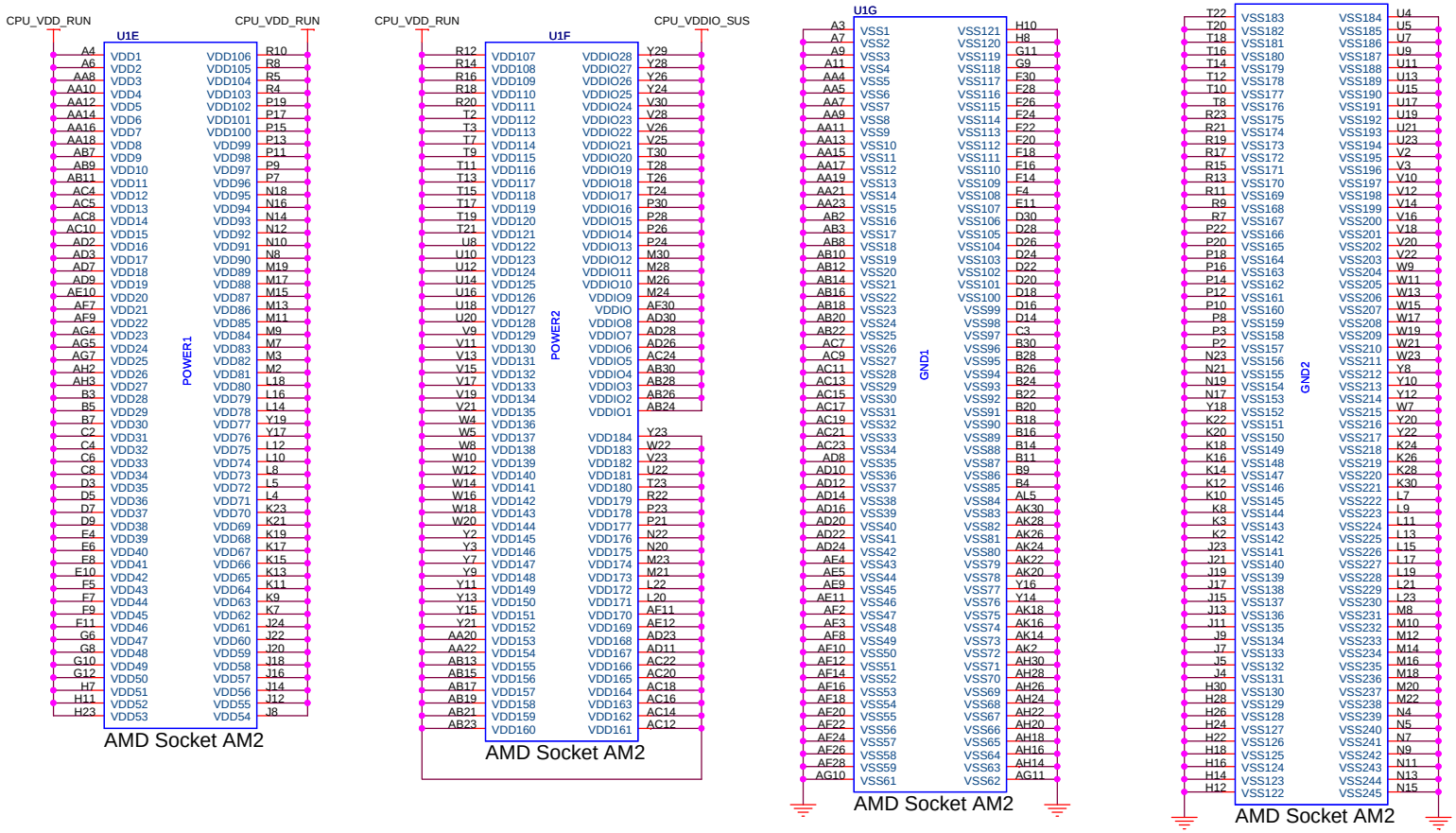
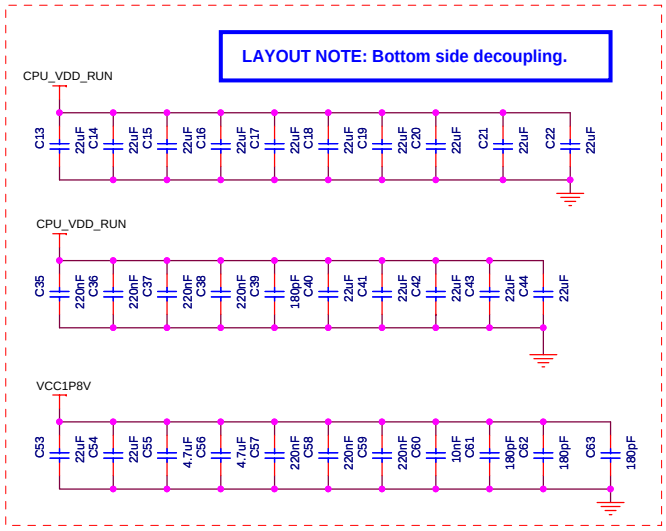
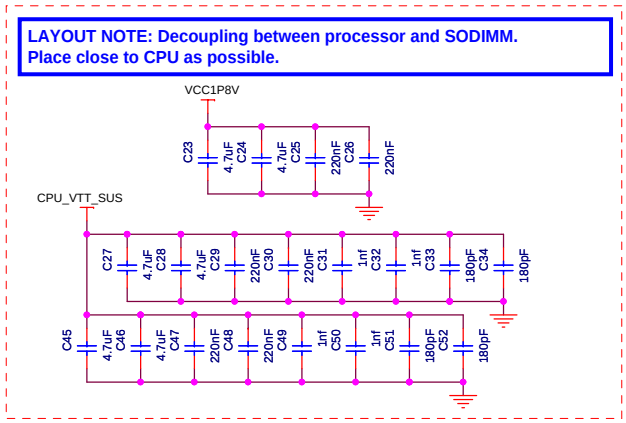
Socket AM2 Control and Debug







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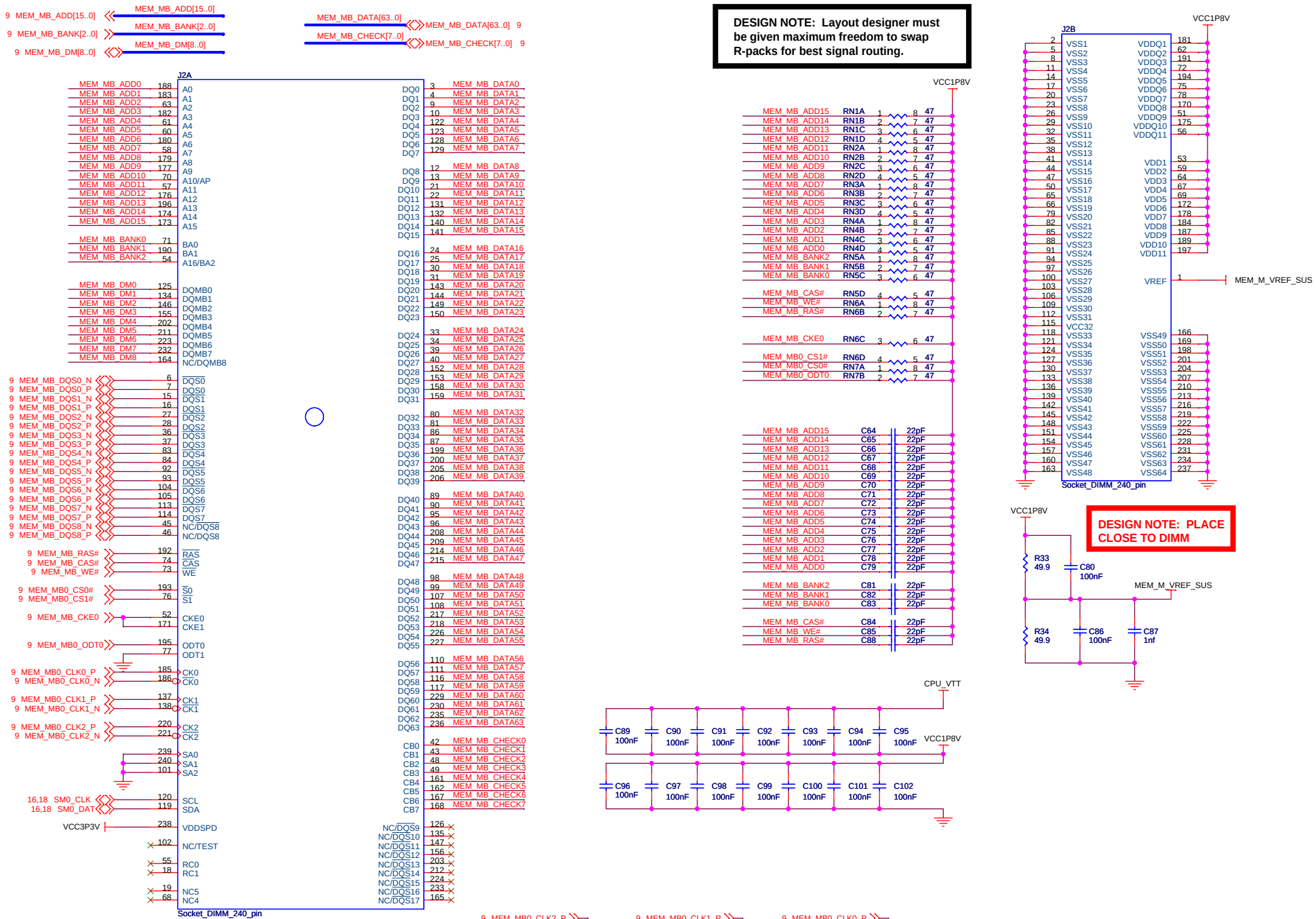
Socket AM2 Power and Ground


DESIGN NOTE: Layout designer must be given maximum freedom to swap R-packs for best signal routing.
J2A
Socket_DIMM_240_pin
J2B
Socket_DIMM_240_pin
VCC1P8V
CPU_VTT
VCC3P3V
MEM_M_VREF_SUS
DESIGN NOTE: PLACE CLOSE TO DIMM
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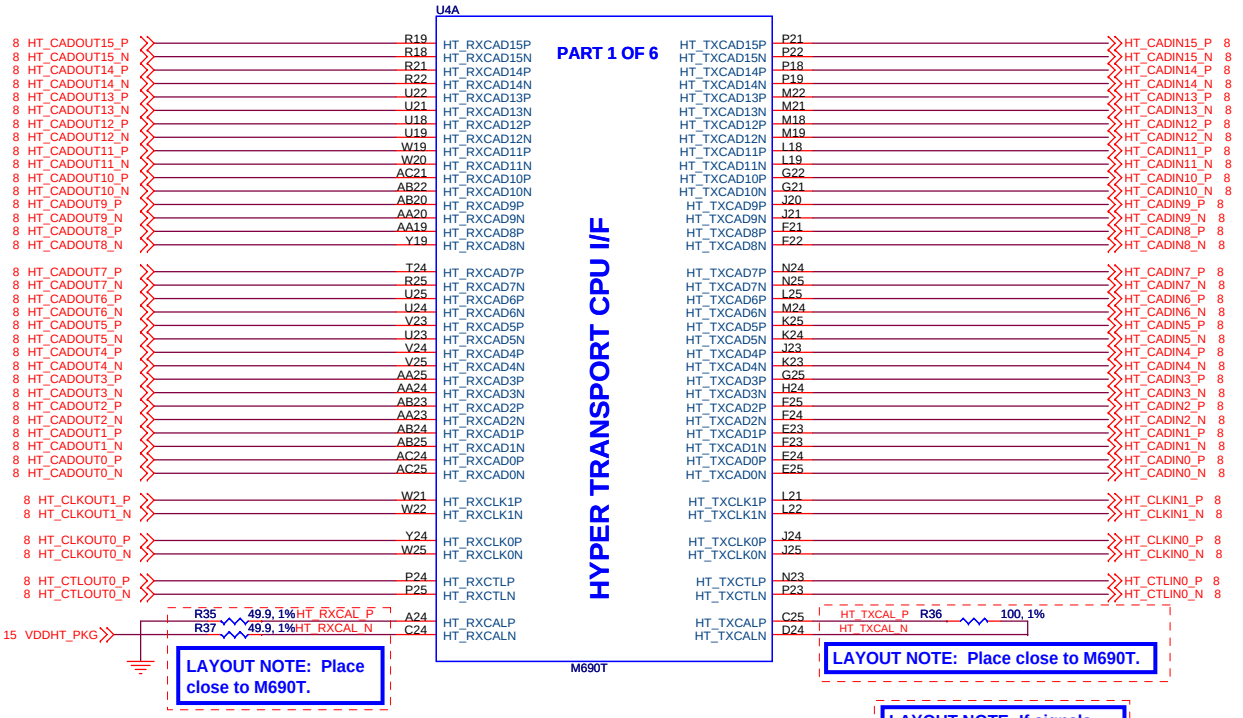
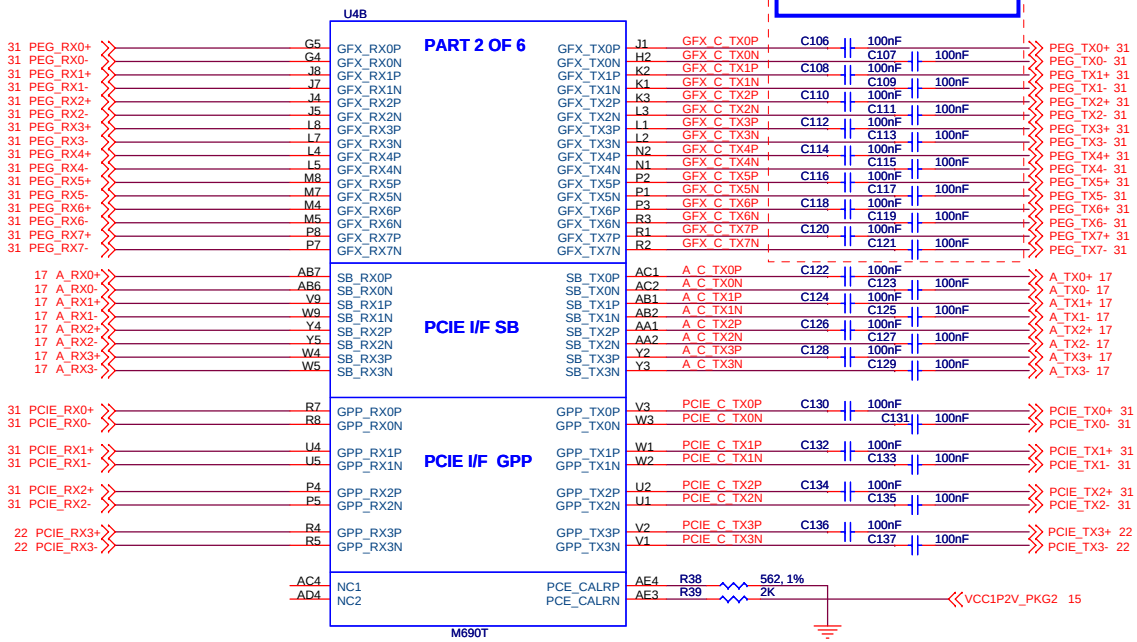
DIMM DDR2



LAYOUT NOTE: If signals are passing through a connector, place caps close to connector. If not, then place close to M690T.



AMD M690T HyperTransport™, PCIe(R), and PCIe Graphics

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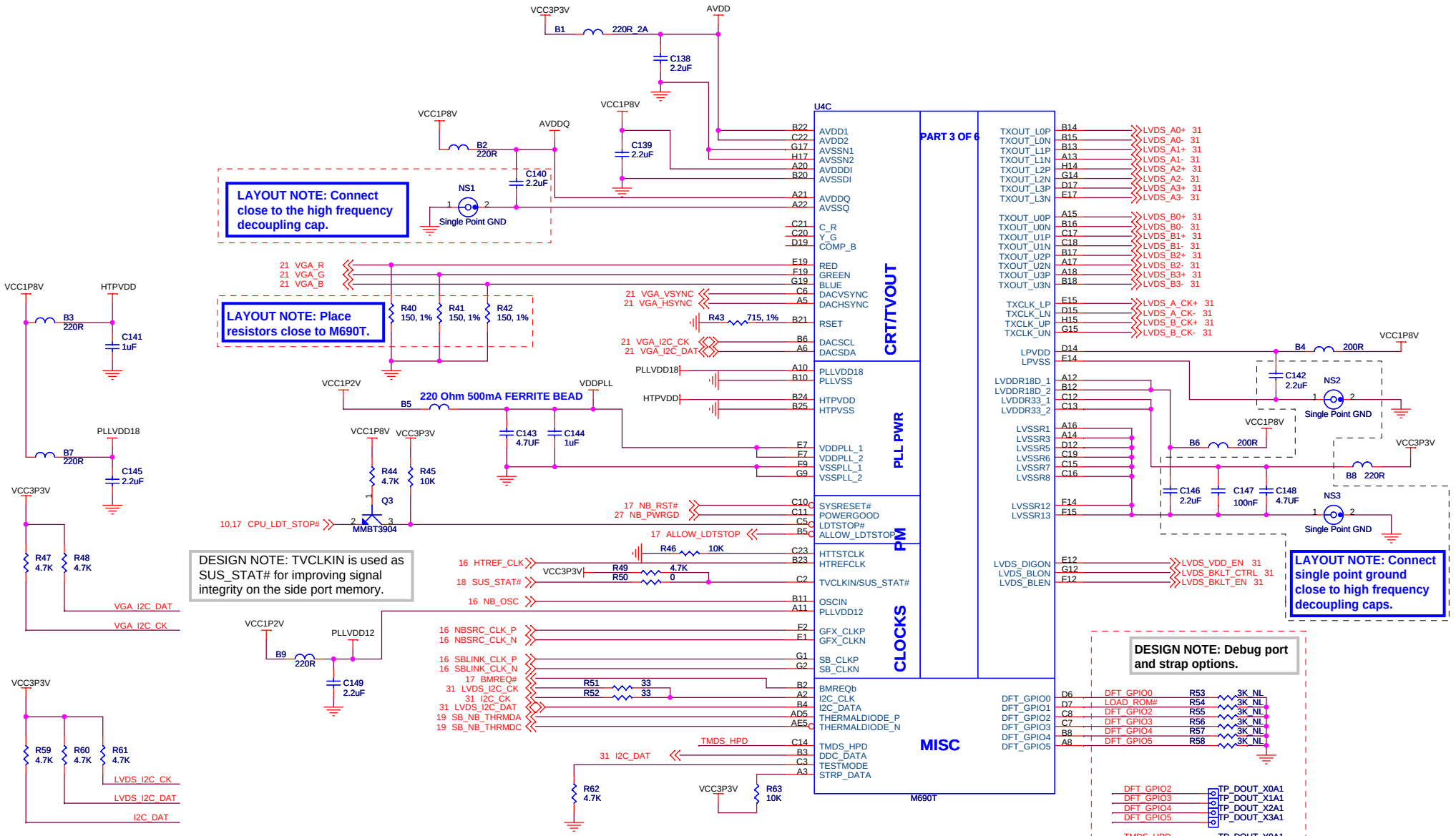

M690T Straping Table

	DFT_GPIO1	DFT_GPIO0	DFT_GPIO[4:2]	DFT_GPIO5
PULL HIGH (internally pulled high)	Use Hardware values REQUIRED SET	Memory side port not available REQUIRED SET	These pin straps are used to configure PCIe General Purpose Port (GPP) mode: 111: Register defined configuration, register default setting to Config E 110: Config A - 4-0-0-0-0 101: Config B - 4-4 100: Config C - 4-2-2 011: Config D - 4-2-1-1 010: Config E - 4-1-1-1-1	Enable debug bus via the memory IO pads, if available in the package. Use default values. REQUIRED SET
PULL LOW		Memory side port available	All other setting are register defined configuration, register default setting to Config E	Use the memory data bus to output the debug bus

AMD M690T PLL and Video Interface

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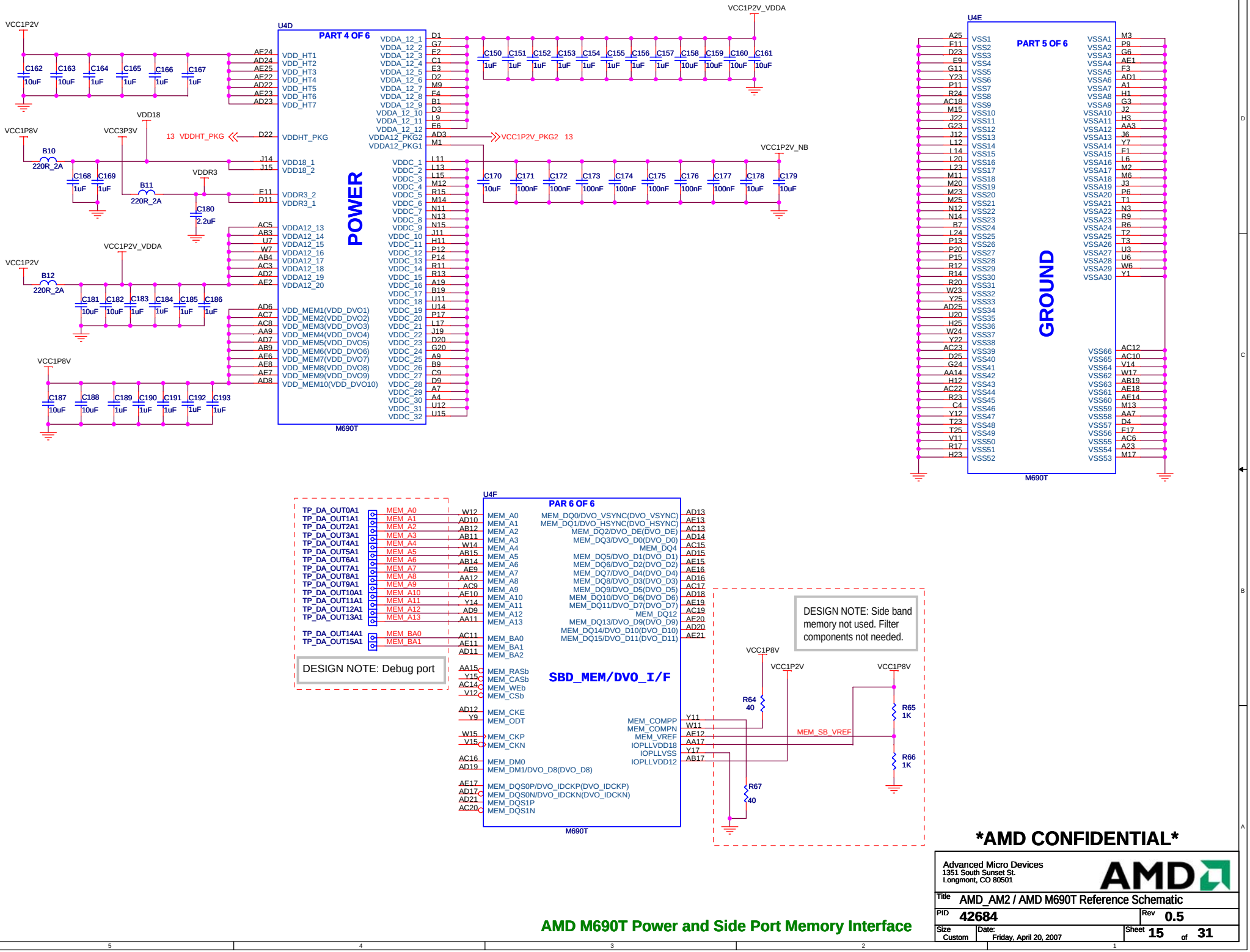

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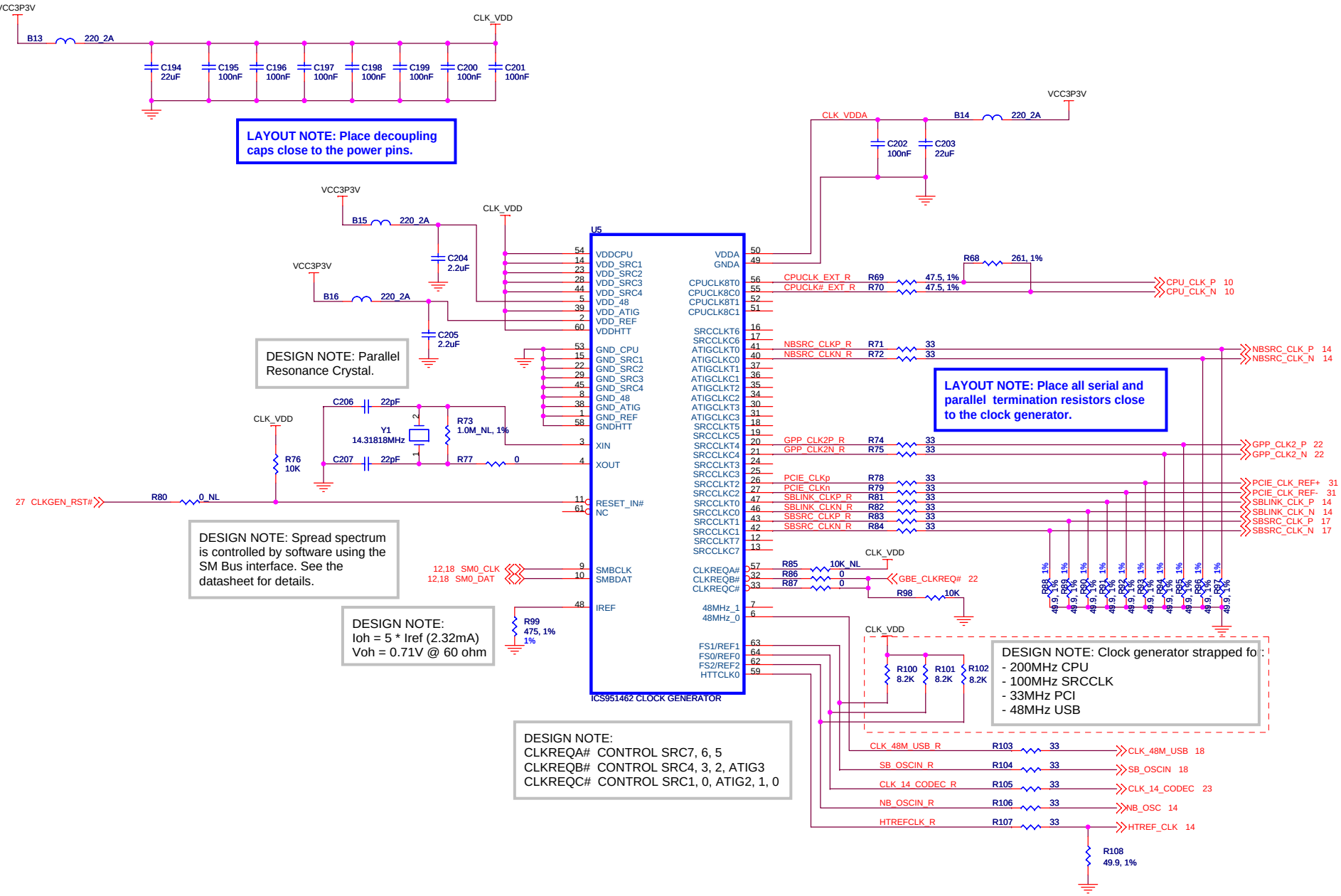
AMD M690T Power and Side Port Memory Interface



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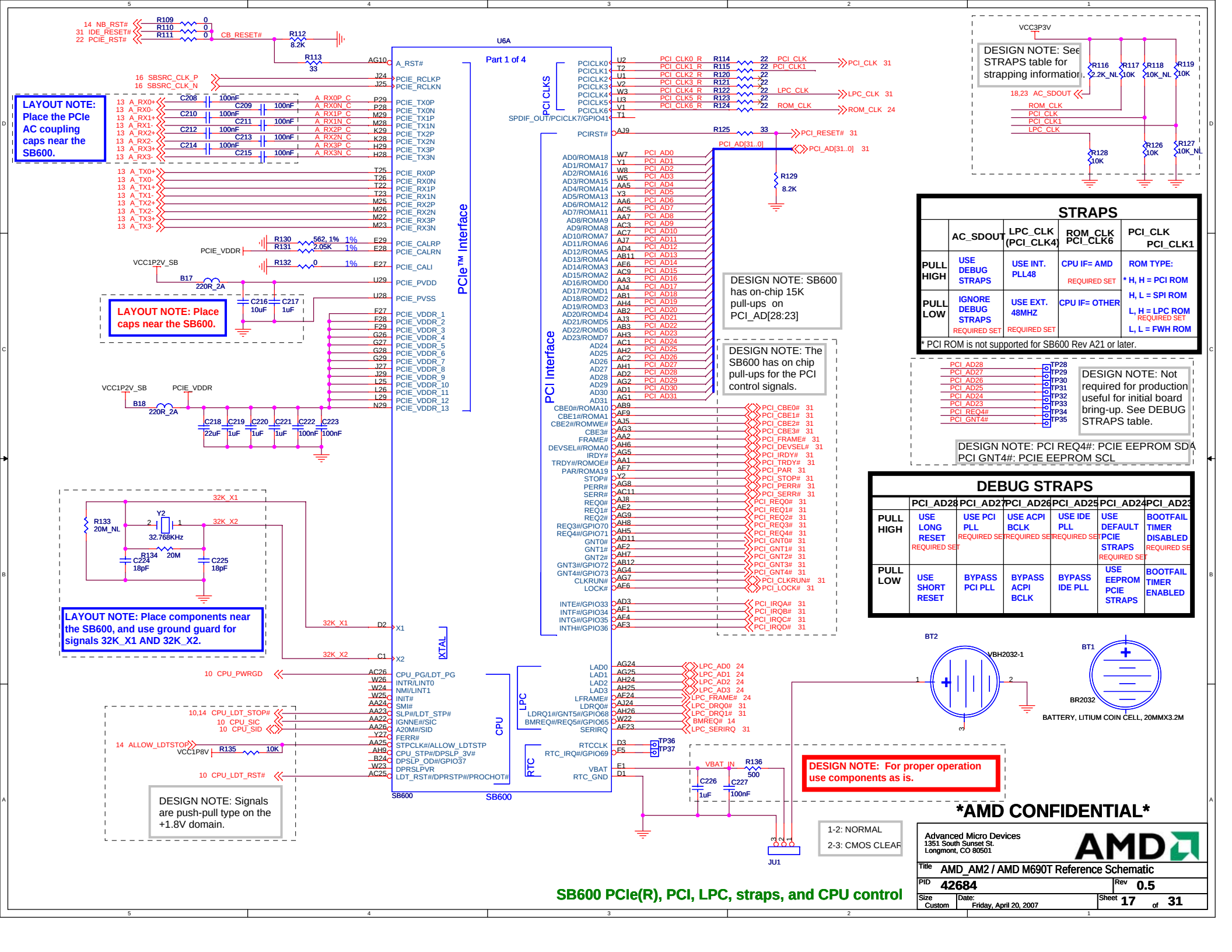
Clock Generator



STRAPS

	AC_SDOUT	LPC_CLK (PCI_CLK4)	ROM_CLK PCI_CLK6	PCI_CLK PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF= AMD REQUIRED SET	ROM TYPE: * H, H = PCI ROM H, L = SPI ROM
PULL LOW	IGNORE DEBUG STRAPS REQUIRED SET	USE EXT. 48MHZ REQUIRED SET	CPU IF= OTHER	L, H = LPC ROM REQUIRED SET L, L = FWH ROM

* PCI ROM is not supported for SB600 Rev A21 or later.

DEBUG STRAPS

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET REQUIRED SET	USE PCI PLL REQUIRED SET	USE ACPI BCLK REQUIRED SET	USE IDE PLL REQUIRED SET	USE DEFAULT PCIE STRAPS REQUIRED SET	BOOTFAIL TIMER DISABLED REQUIRED SE
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAIL TIMER ENABLED

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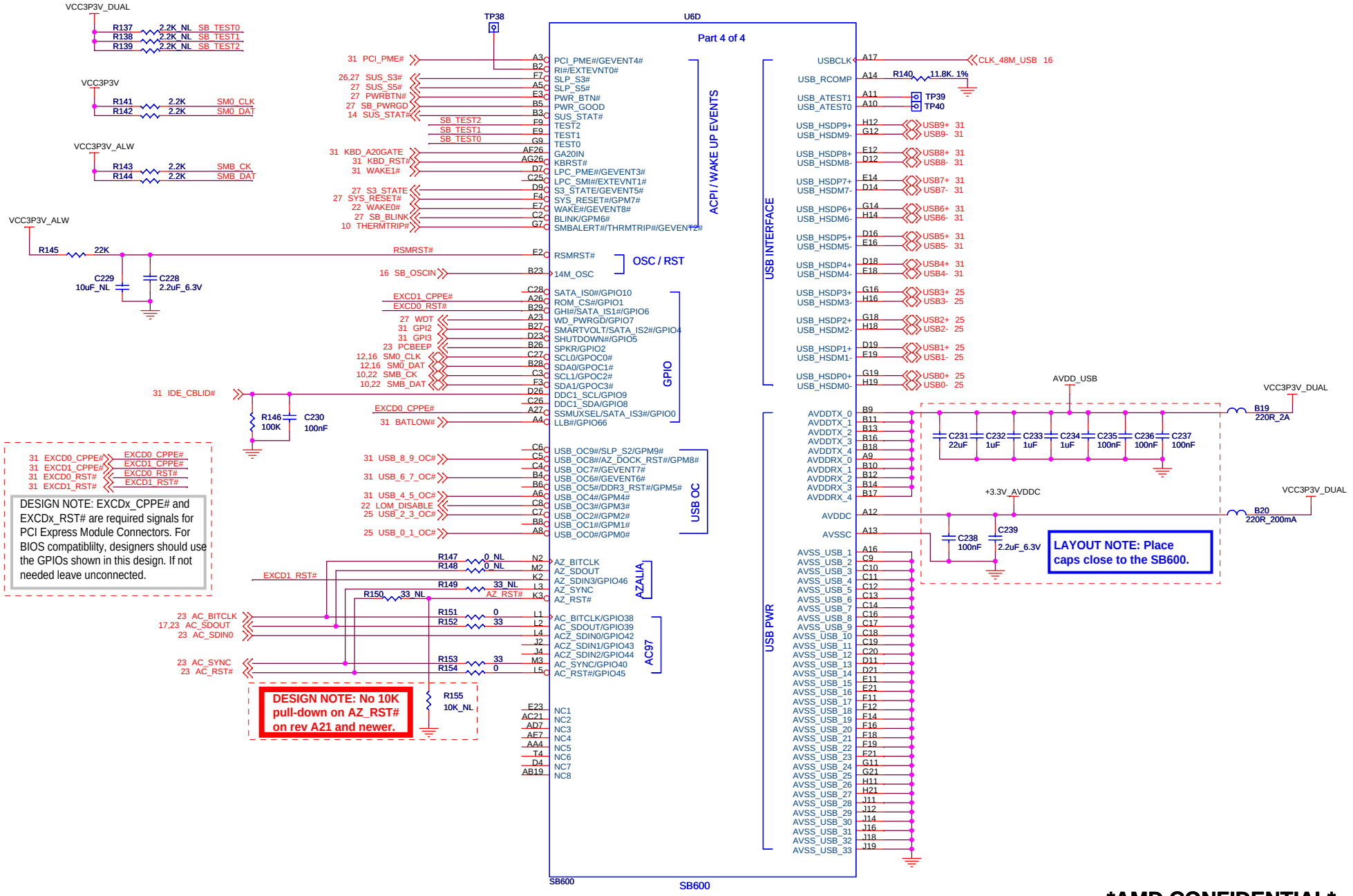

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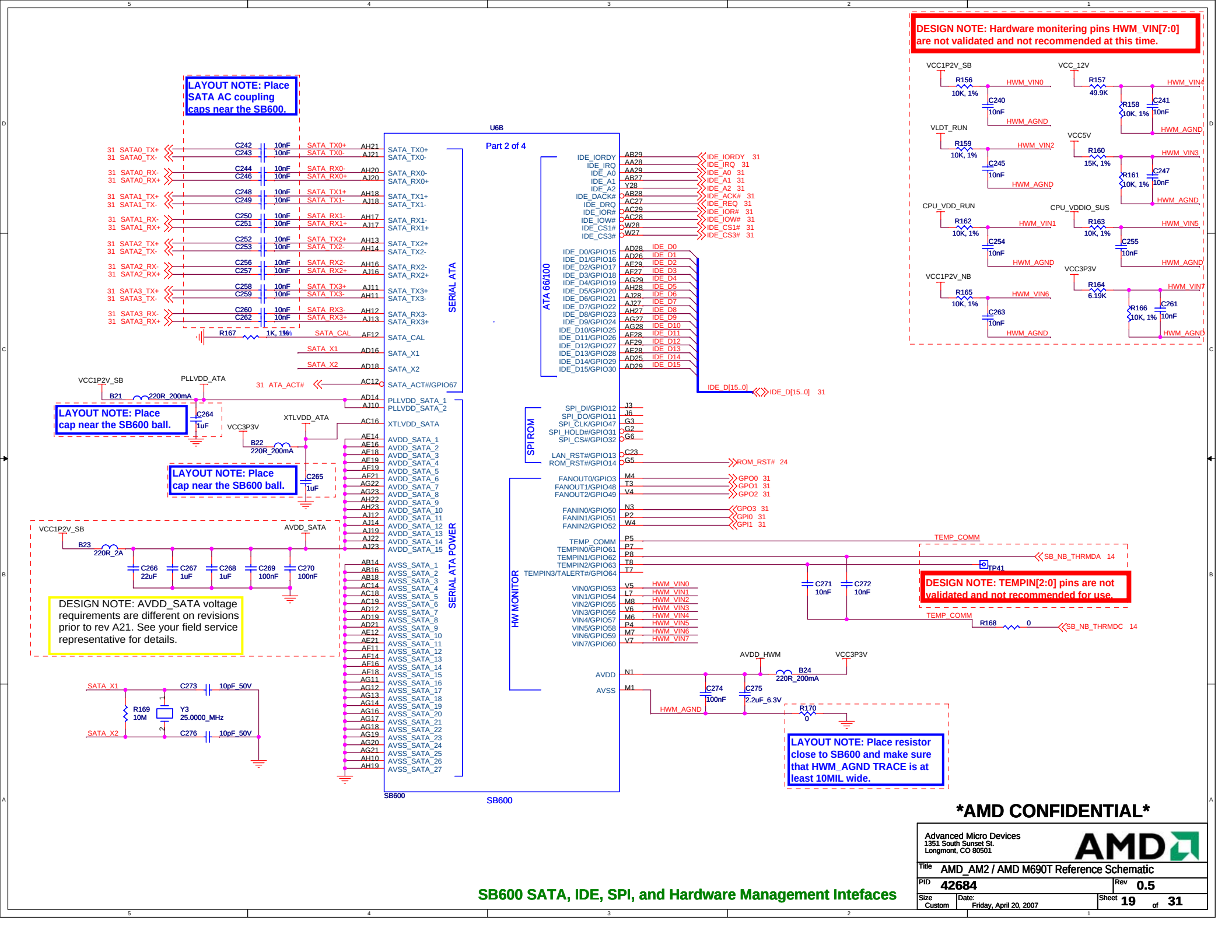
SB600 ACPI, GPIO, USB, and Audio Interfaces


LAYOUT NOTE: Place SATA AC coupling caps near the SB600.
U6B
Part 2 of 4
SERIAL ATA
SERIAL ATA POWER
ATA 66/100
SPI ROM
HW MONITOR
SB600
LAYOUT NOTE: Place cap near the SB600 ball.
LAYOUT NOTE: Place cap near the SB600 ball.
DESIGN NOTE: AVDD_SATA voltage requirements are different on revisions prior to rev A21. See your field service representative for details.
DESIGN NOTE: Hardware monitering pins HWM_VIN[7:0] are not validated and not recommended at this time.
DESIGN NOTE: TEMPIN[2:0] pins are not validated and not recommended for use.
LAYOUT NOTE: Place resistor close to SB600 and make sure that HWM_AGND TRACE is at least 10MIL wide.
SB600 SATA, IDE, SPI, and Hardware Management Intefaces
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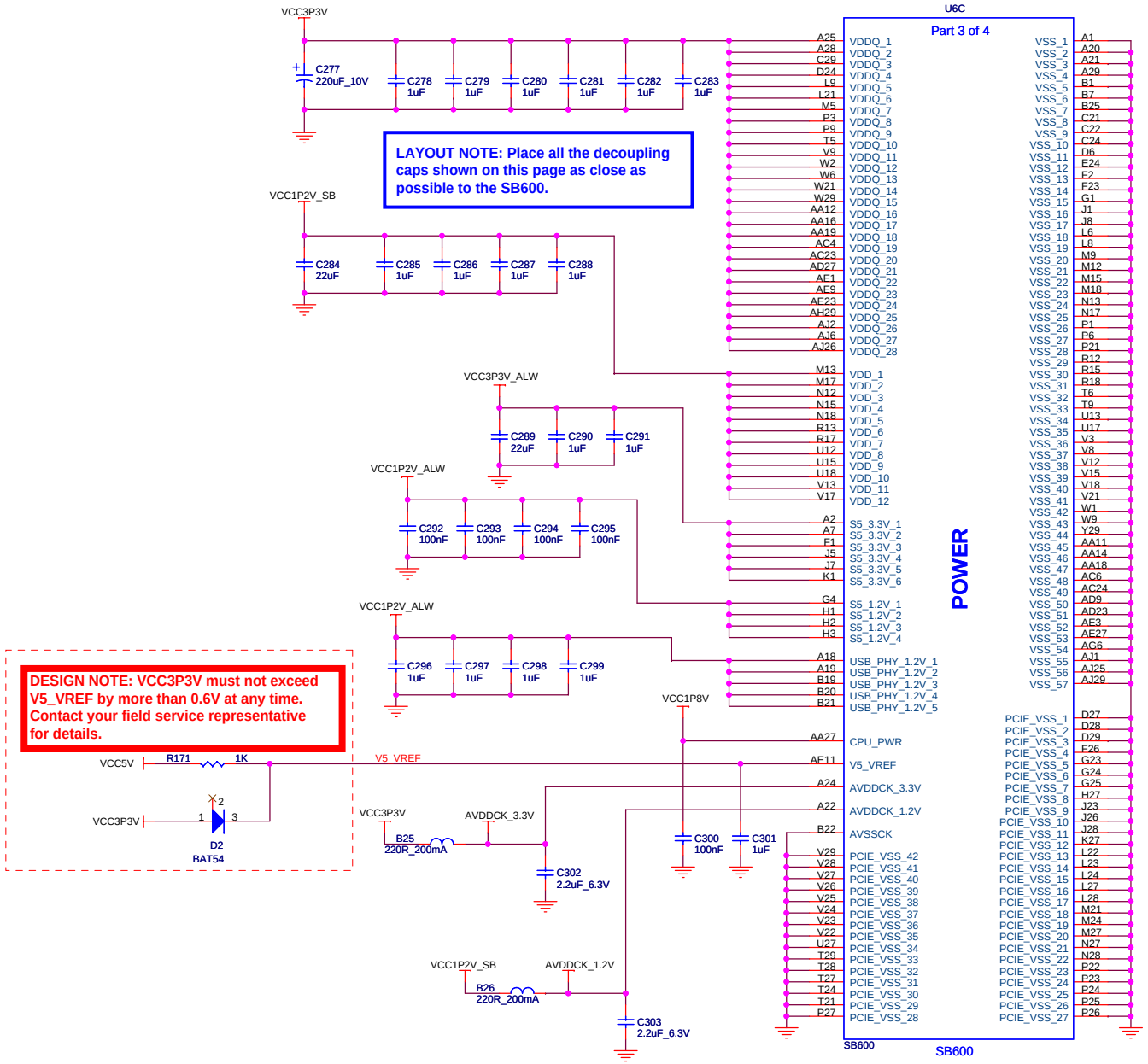

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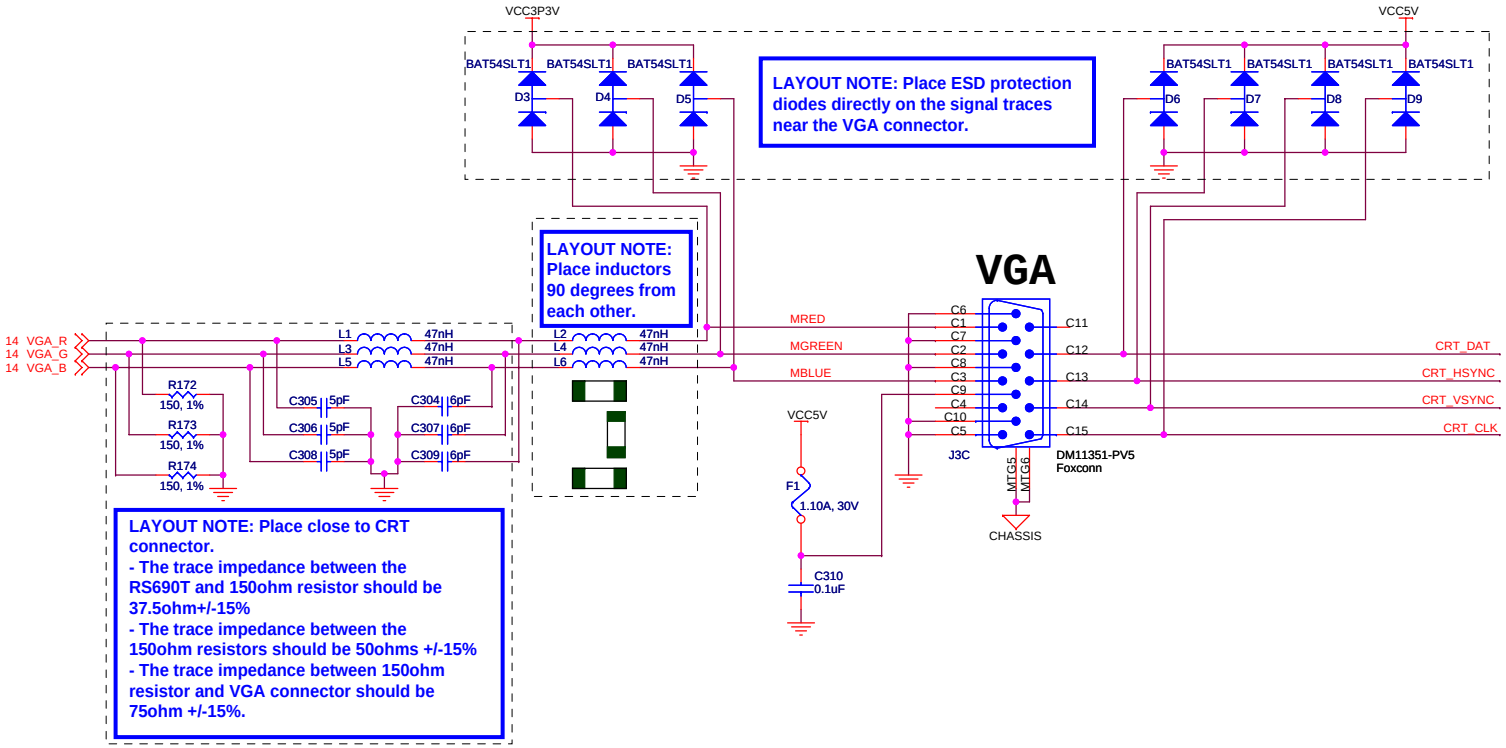
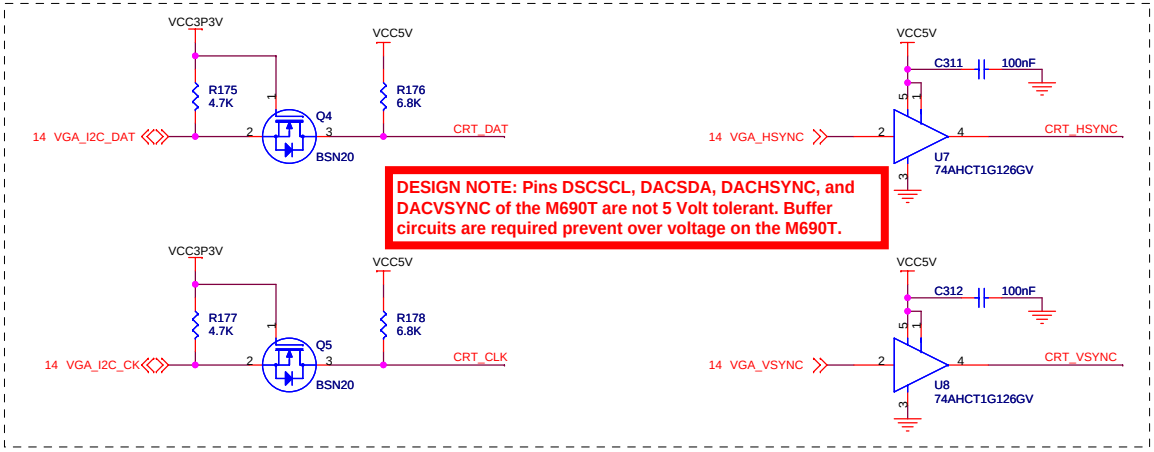
SB600 Power





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CRT Connector

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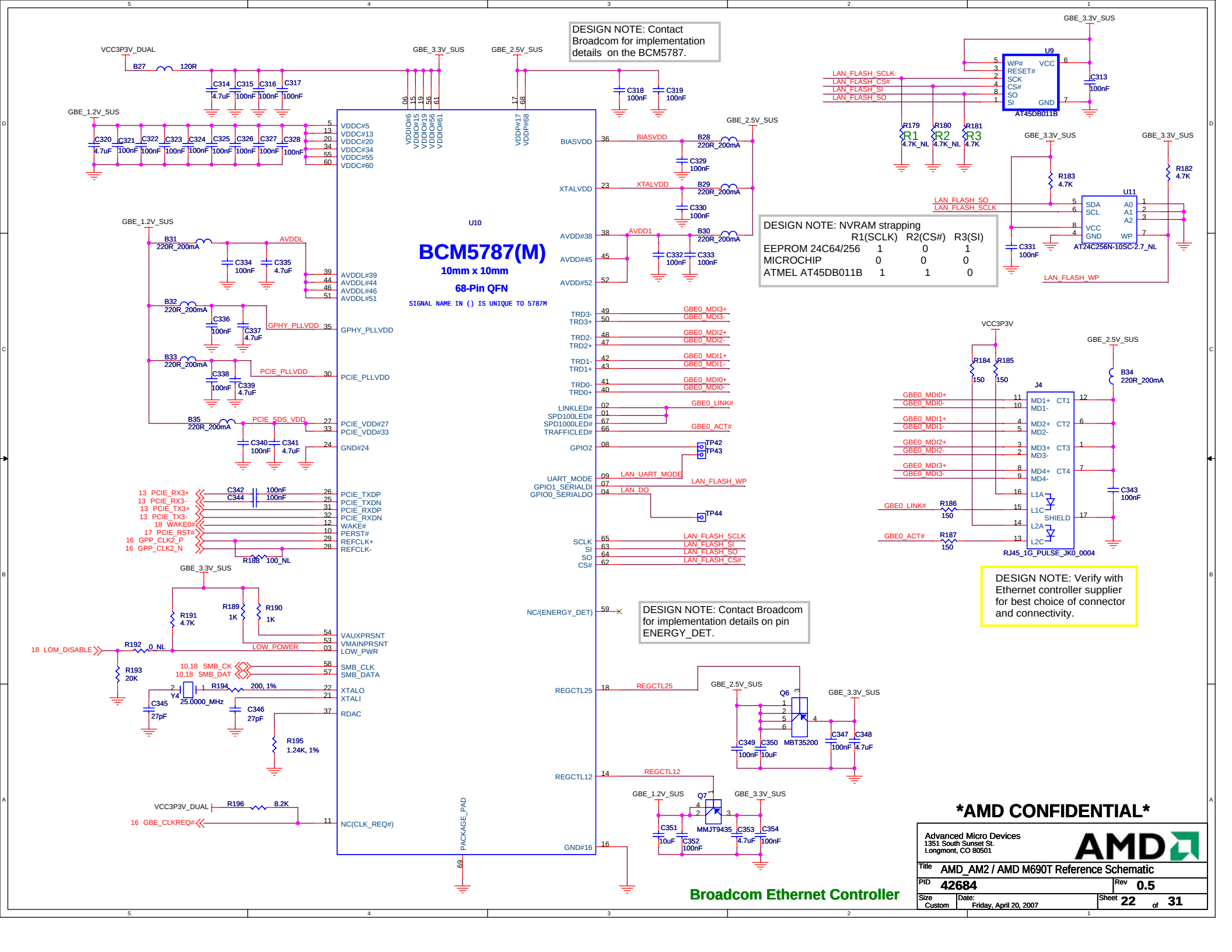
DESIGN NOTE: Contact Broadcom for implementation details on the BCM5787.
BCM5787(M)
10mm x 10mm
68-Pin QFN
SIGNAL NAME IN () IS UNIQUE TO 5787M
DESIGN NOTE: NVRAM strapping
R1(SCLK) R2(CS#) R3(SI)
EEPROM 24C64/256 1 0 1
MICROCHIP 0 0 0
ATMEL AT45DB011B 1 1 0
DESIGN NOTE: Verify with Ethernet controller supplier for best choice of connector and connectivity.
DESIGN NOTE: Contact Broadcom for implementation details on pin ENERGY_DET.
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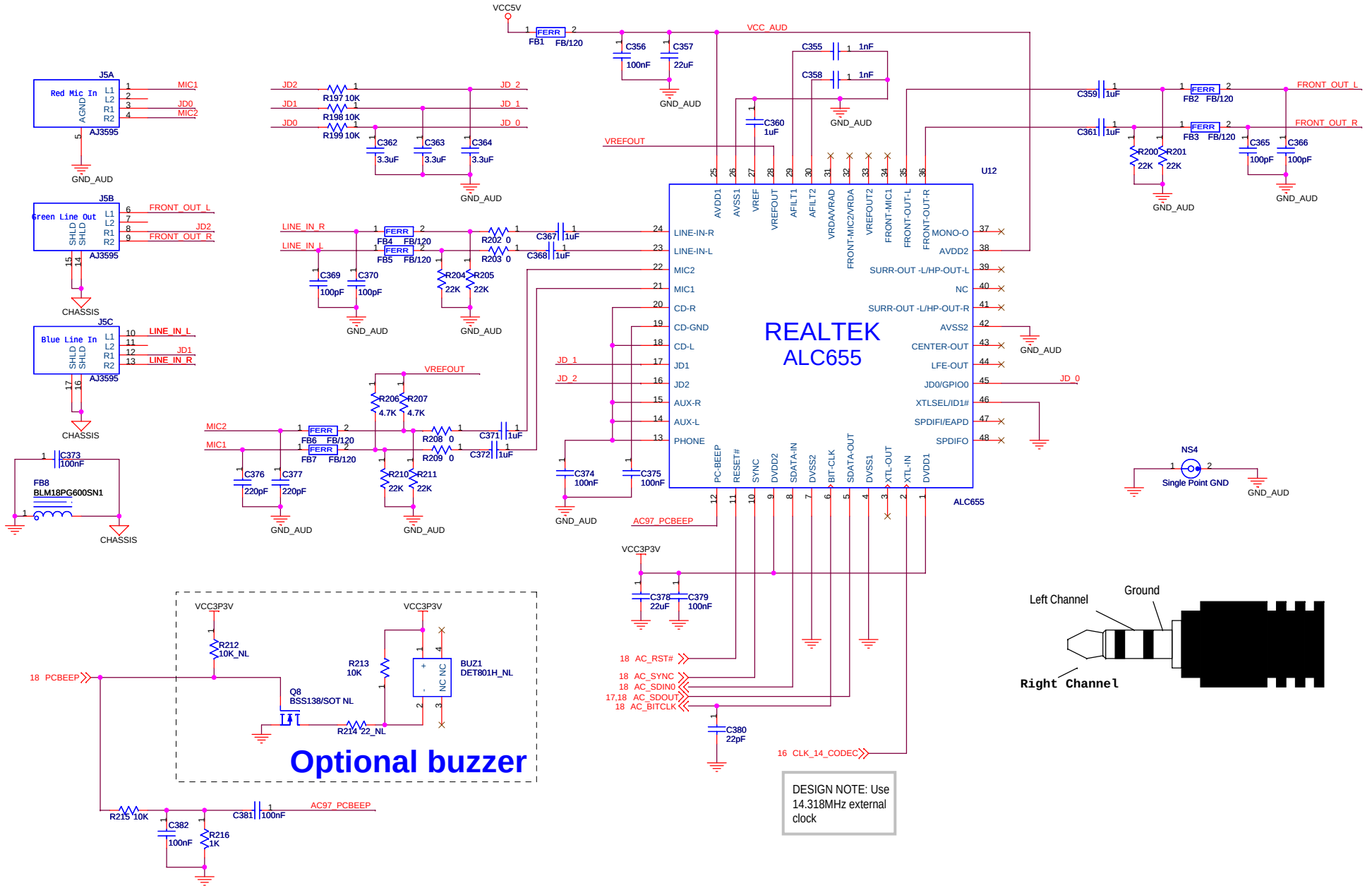
Broadcom Ethernet Controller



Realtek Audio Codec

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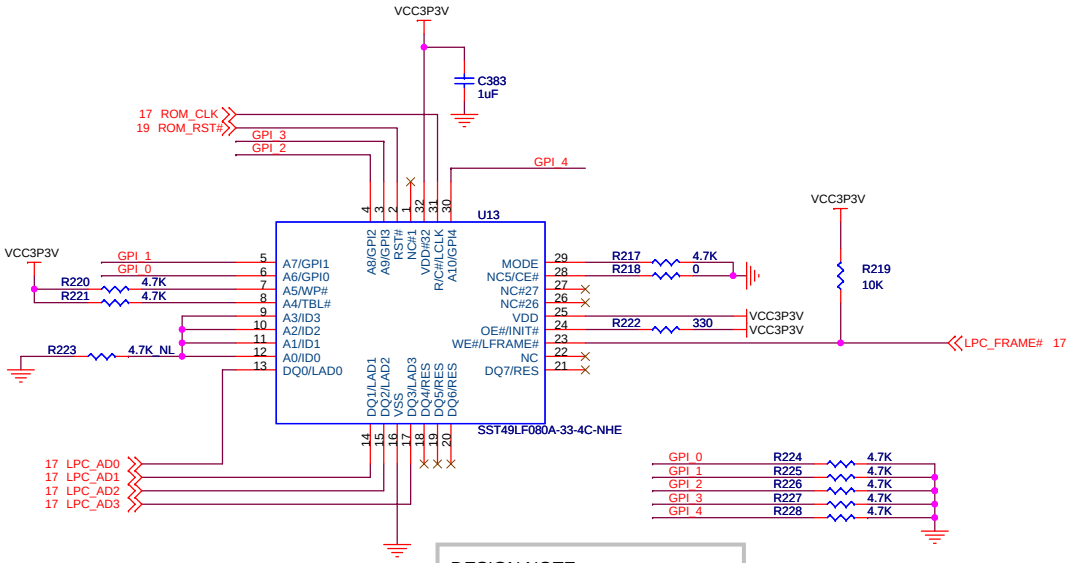

DESIGN NOTE:
MODE: low - LPC mode is enabled
high - programmer mode is enabled
CE#: low - device is enabled
high - device is in low power mode

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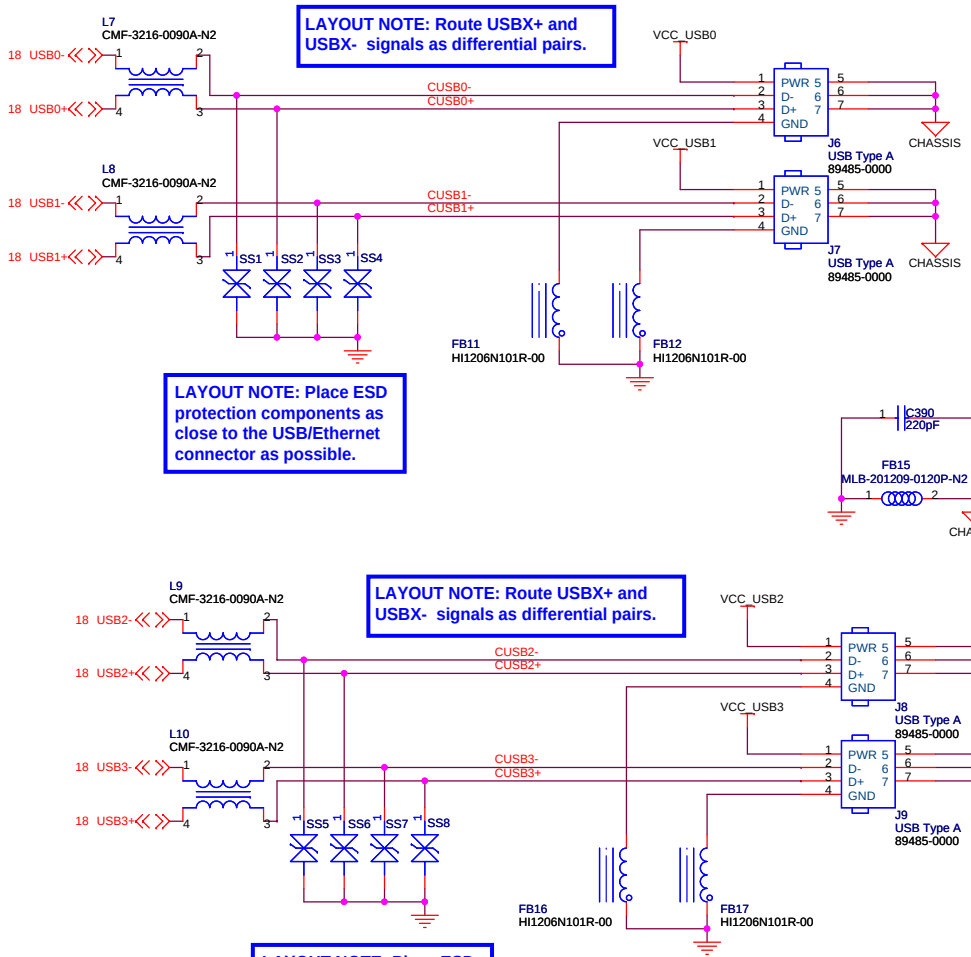
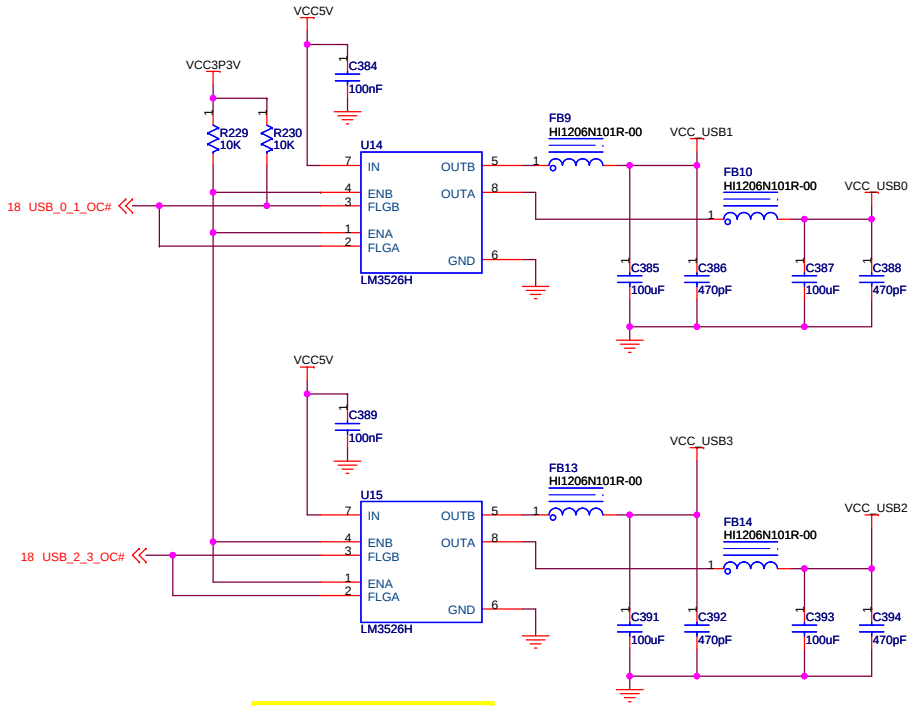
LPC BIOS





DESIGN NOTE: Power supply solution must be able to provide sufficient current on VCC5V to power each USB port with 500mA.

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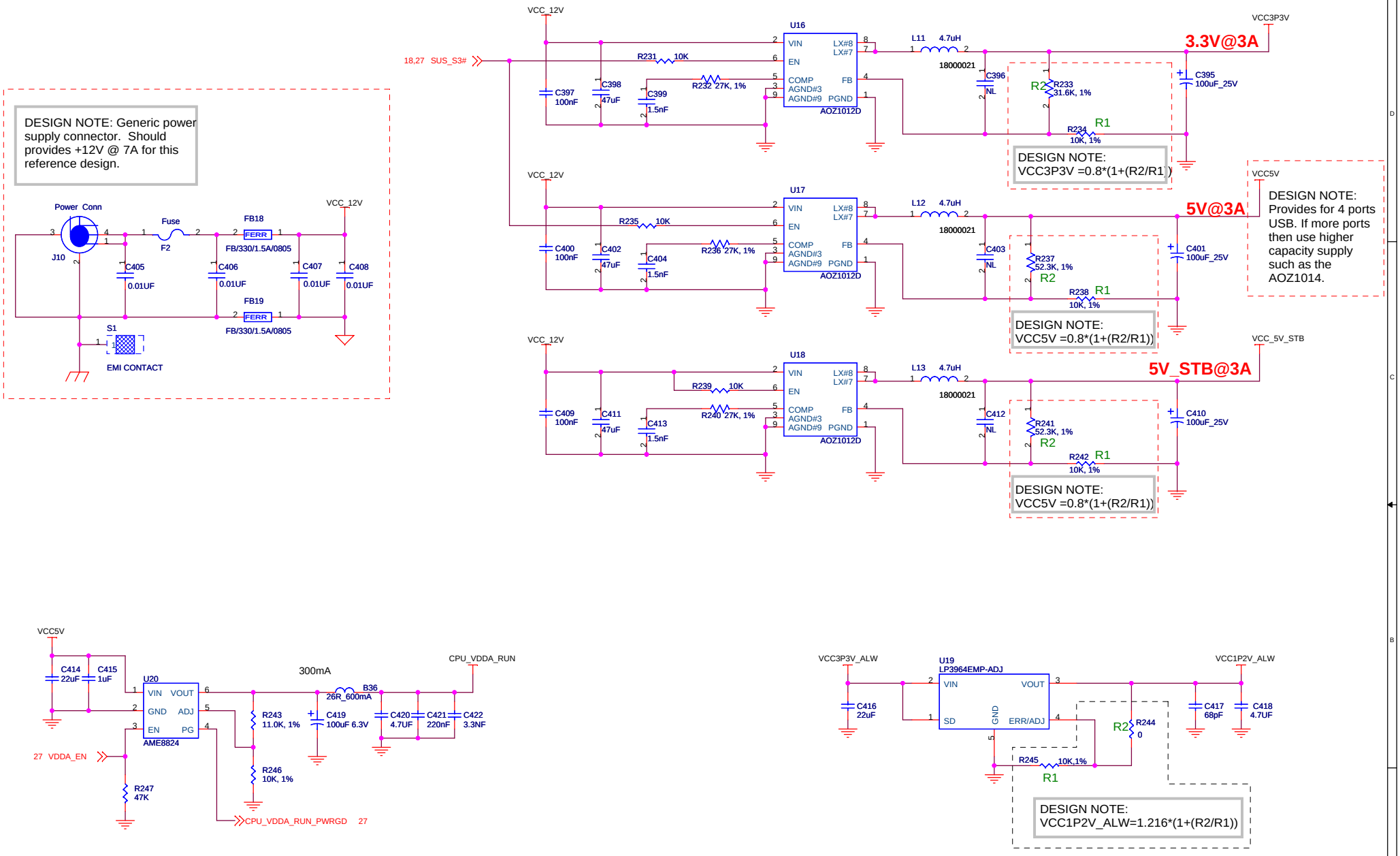
USB Power and Connectors



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Power Main System, SB600 PCIe(R), and Other

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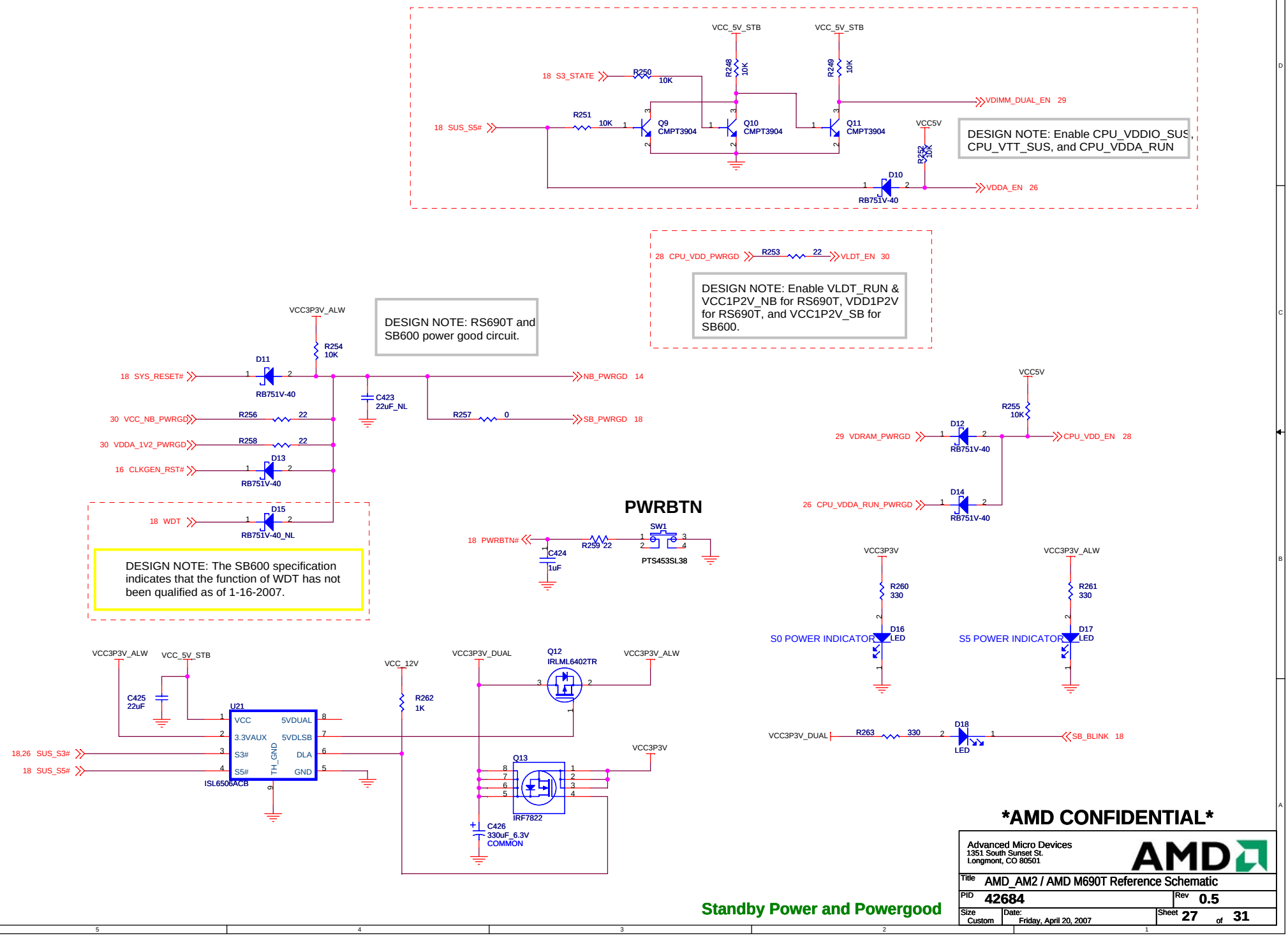

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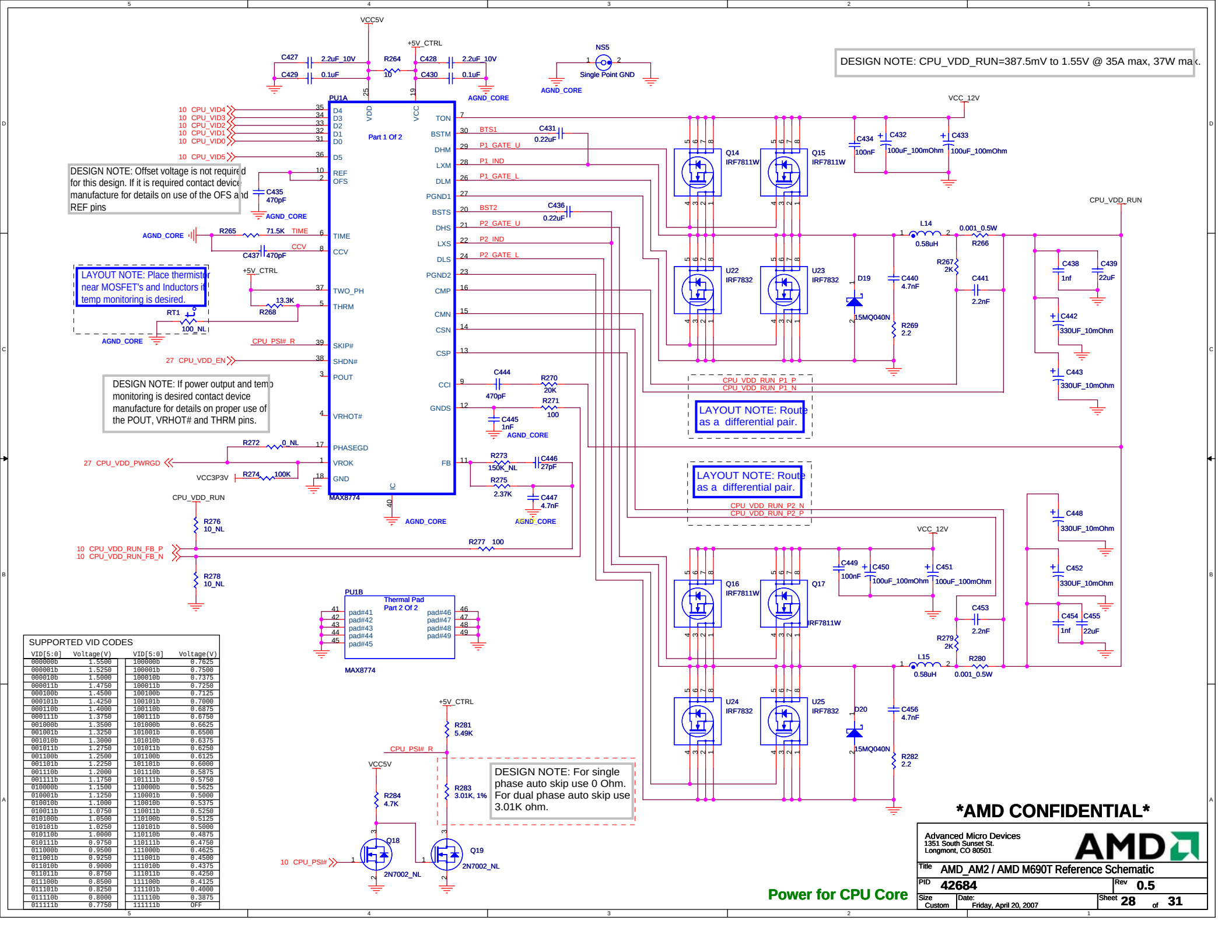
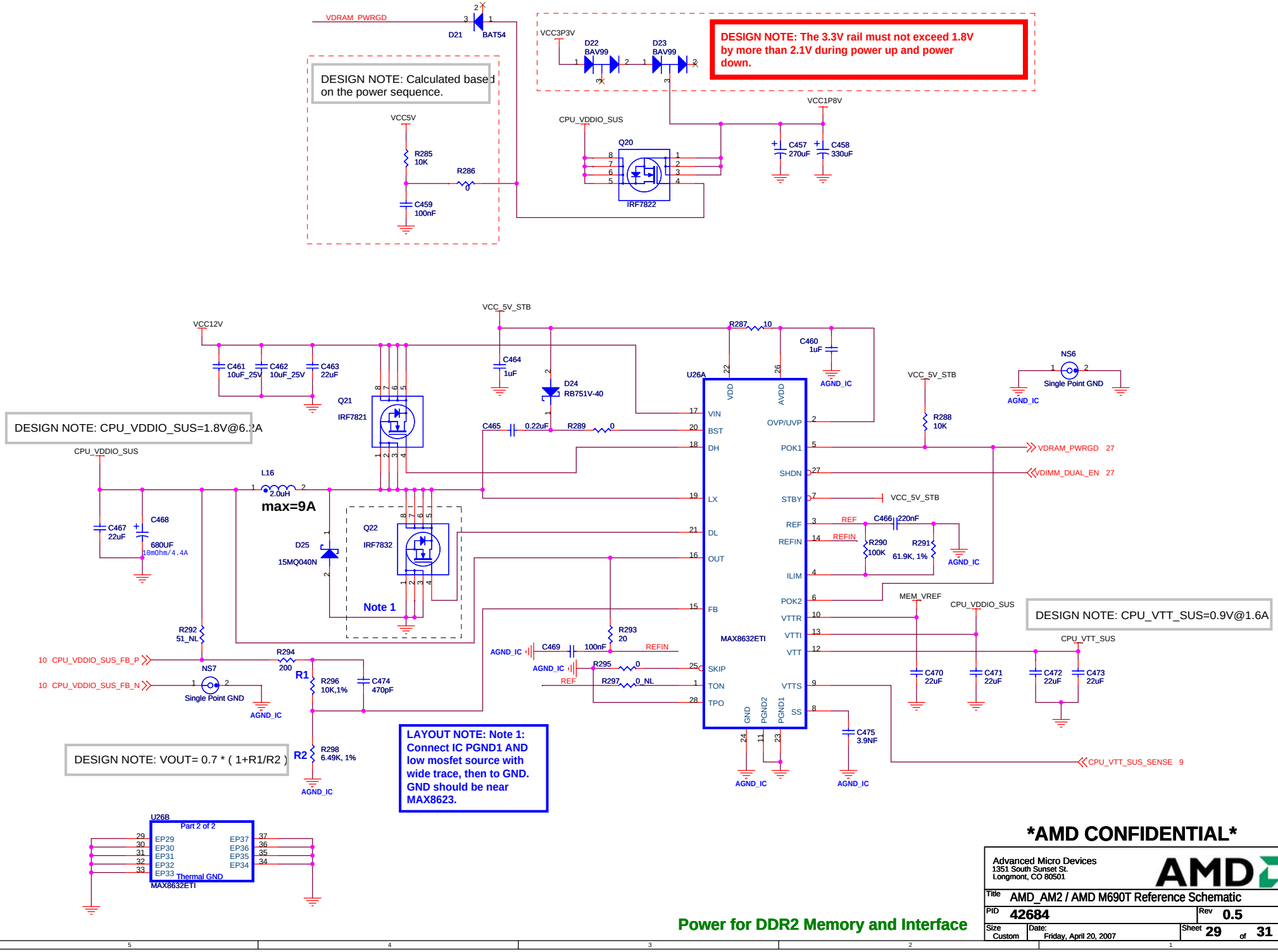
Standby Power and Powergood



SUPPORTED VID CODES

VID[5:0]	Voltage(V)	VID[5:0]	Voltage(V)
000000b	1.5500	100000b	0.7625
000001b	1.5250	100001b	0.7500
000010b	1.5000	100010b	0.7375
000011b	1.4750	100011b	0.7250
000100b	1.4500	100100b	0.7125
000101b	1.4250	100101b	0.7000
000110b	1.4000	100110b	0.6875
000111b	1.3750	100111b	0.6750
001000b	1.3500	101000b	0.6625
001001b	1.3250	101001b	0.6500
001010b	1.3000	101010b	0.6375
001011b	1.2750	101011b	0.6250
001100b	1.2500	101100b	0.6125
001101b	1.2250	101101b	0.6000
001110b	1.2000	101110b	0.5875
001111b	1.1750	101111b	0.5750
010000b	1.1500	110000b	0.5625
010001b	1.1250	110001b	0.5000
010010b	1.1000	110010b	0.5375
010011b	1.0750	110011b	0.5250
010100b	1.0500	110100b	0.5125
010101b	1.0250	110101b	0.5000
010110b	1.0000	110110b	0.4875
010111b	0.9750	110111b	0.4750
011000b	0.9500	111000b	0.4625
011001b	0.9250	111001b	0.4500
011010b	0.9000	111010b	0.4375
011011b	0.8750	111011b	0.4250
011100b	0.8500	111100b	0.4125
011101b	0.8250	111101b	0.4000
011110b	0.8000	111110b	0.3875
011111b	0.7750	111111b	OFF



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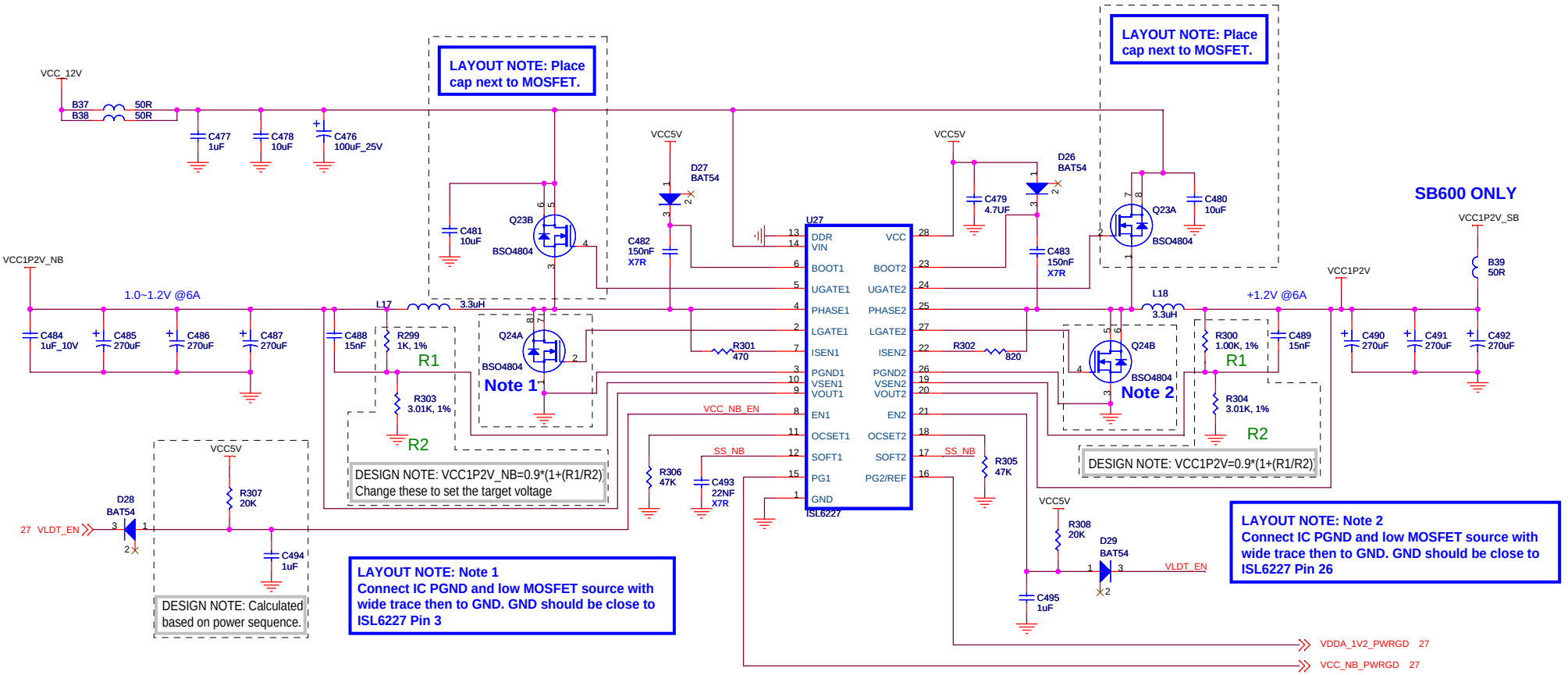
Power for DDR2 Memory and Interface



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Power M690T Core PCIe(R) Interface

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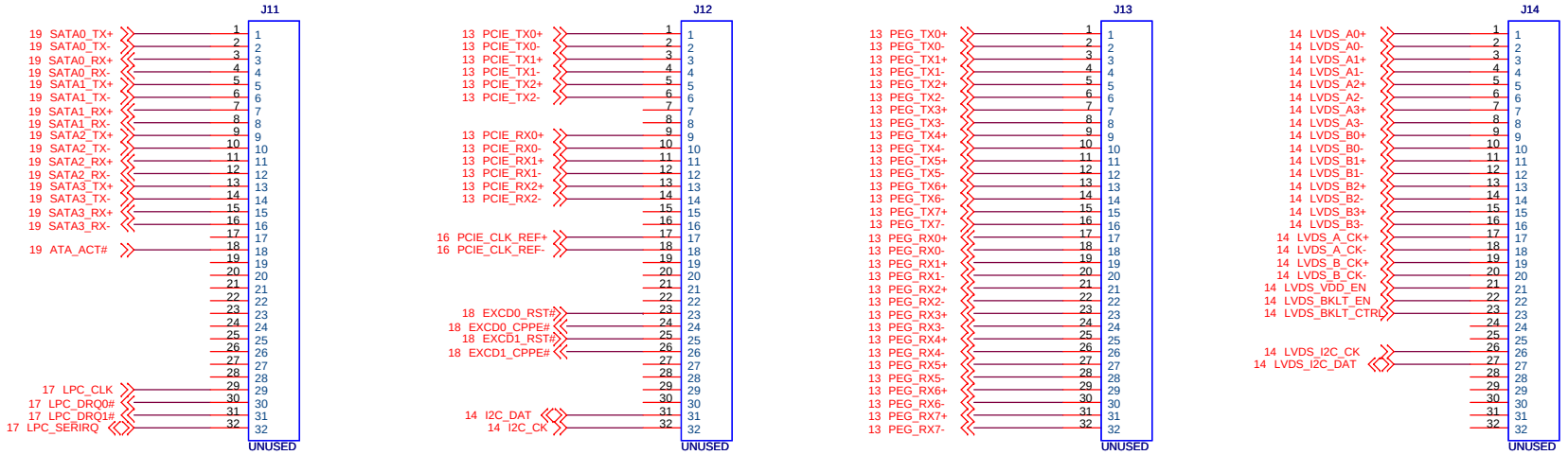

DESIGN NOTE: This page has been included in this schematic to enable the design rule check tool to produce results without errors or warnings. The interfaces on this page do not have connectivity to devices or connectors. This page as well as unused interfaces on the corrosponding pages should be deleted on final schematics.

Unused Interfaces

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