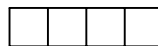
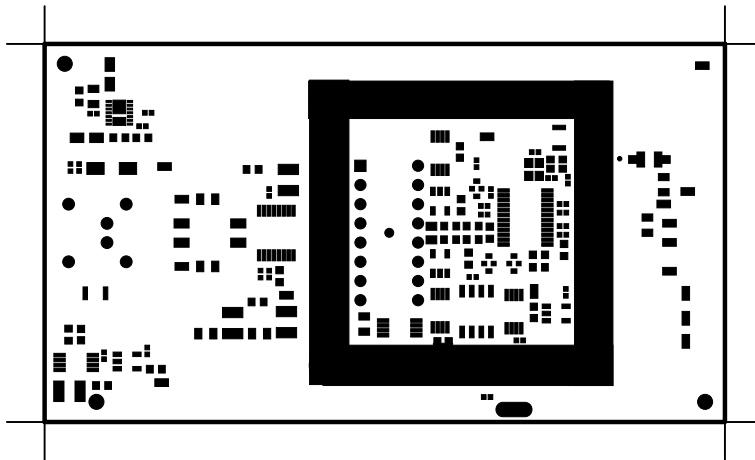


Number	EDA-03803-V2
Drawn By:	N. Beev
DATE	18/09/2018
Checked By:	C. Lesquillier (13/09/2018)

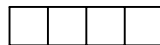


Top Overlay

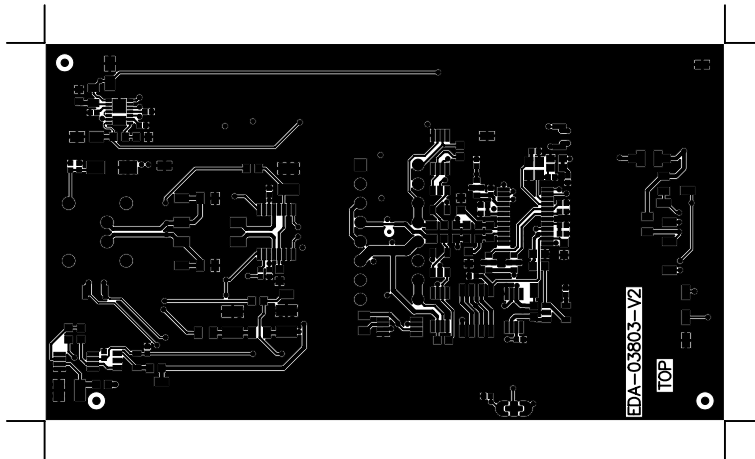


Number	EDA-03803-V2
Drawn By:	N. Beev
DATE	18/09/2018
Checked By:	C. Lesquillier (13/09/2018)

Print Date 18/09/2018 10:19:28  
SCALE: 1,00  
Altium Designer Rev 18.0.12.696



Top Solder

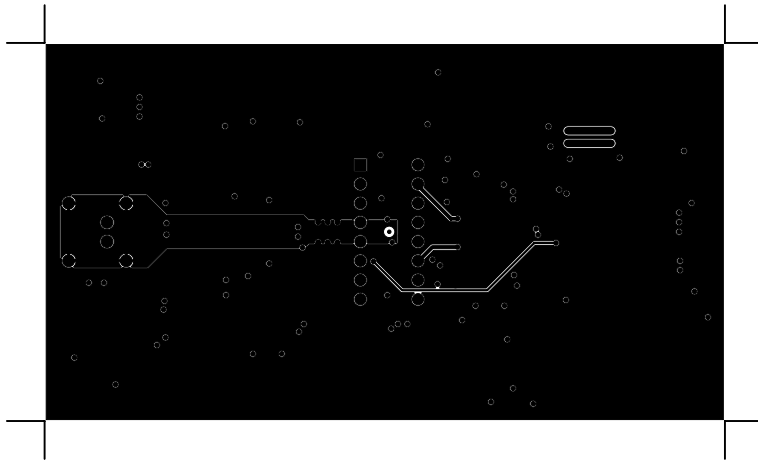


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Drawn By:	N. Beev
DATE	18/09/2018
Checked By:	C. Lesquillier (13/09/2018)

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Altium Designer Rev 18.0.12.696

Top Layer

1			
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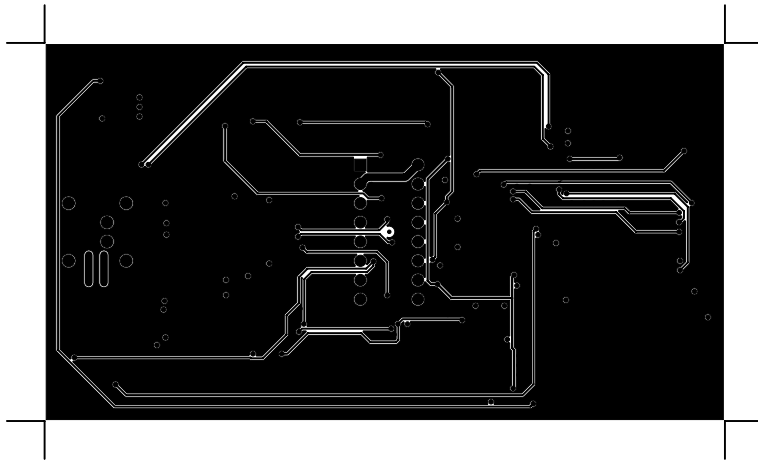


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DATE	18/09/2018
Checked By:	C. Lesquillier (13/09/2018)

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Altium Designer Rev 18.0.12.696

Inner Layer 2

2		
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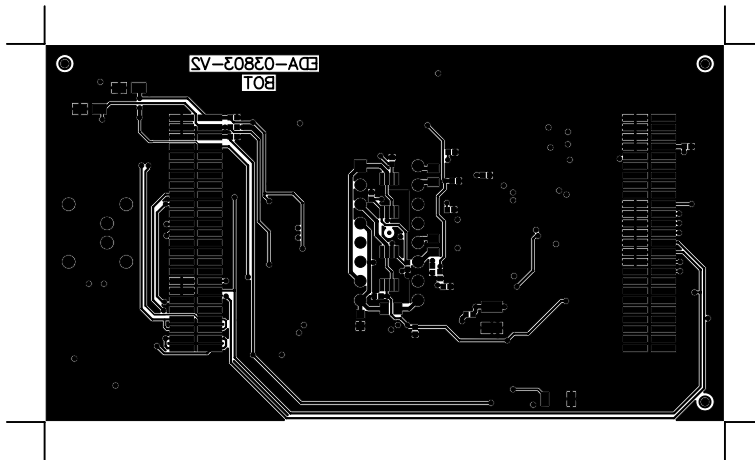


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DATE	18/09/2018
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Print Date 18/09/2018 10:19:27  
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Altium Designer Rev 18.0.12.696

Inner Layer 3

	3	
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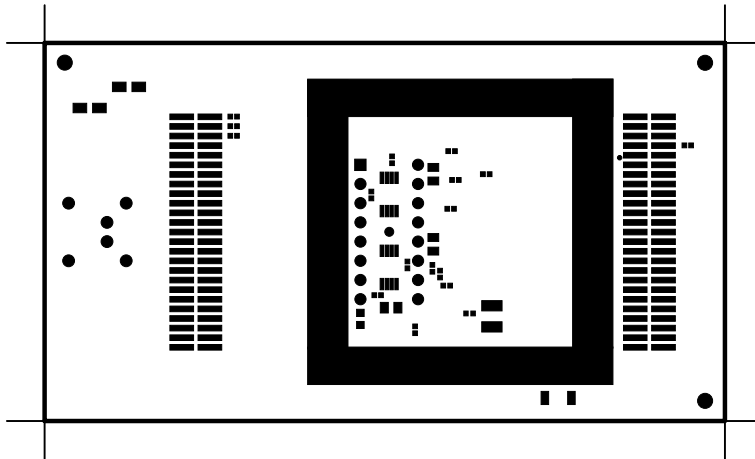


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DATE	18/09/2018
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 Altium Designer Rev 18.0.12.696

			4
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Bottom Layer



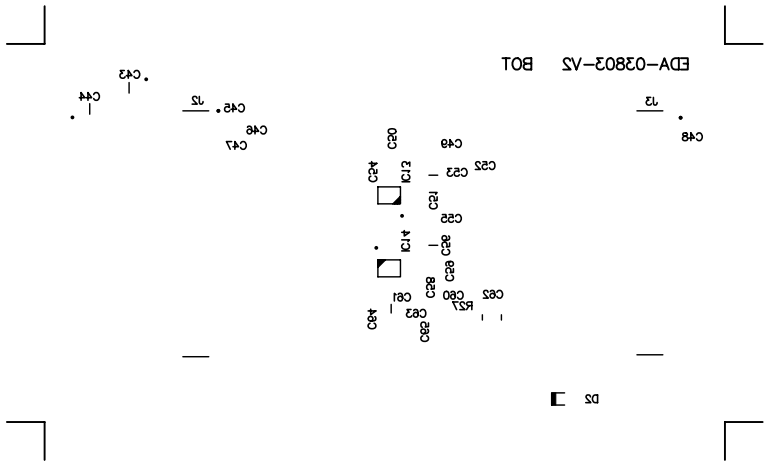
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Drawn By:	N. Beev
DATE	18/09/2018
Checked By:	C. Lesquillier (13/09/2018)

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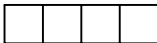


Bottom Soler



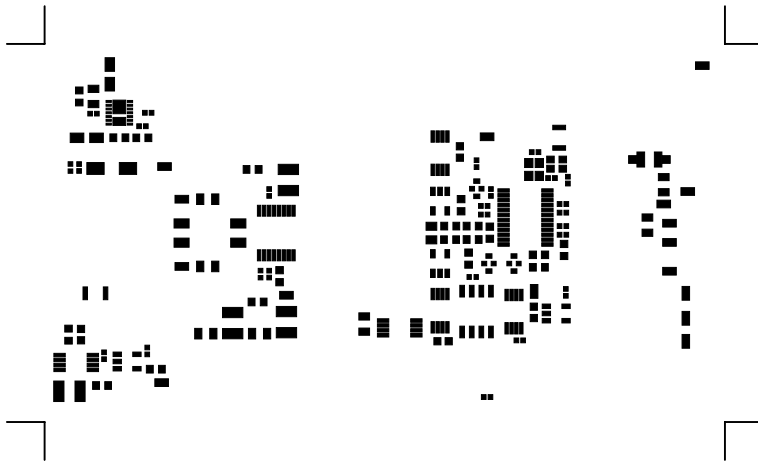


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Drawn By:	N. Beev
DATE	18/09/2018
Checked By:	C. Lesquillier (13/09/2018)



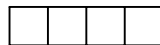
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Bottom Overlay

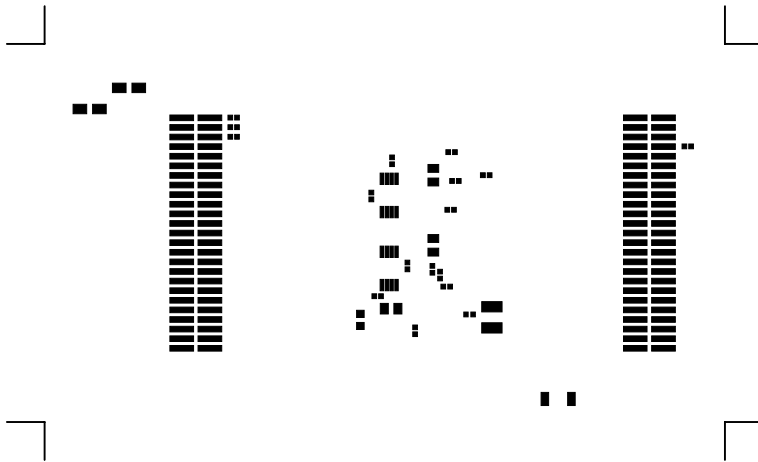


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DATE	18/09/2018
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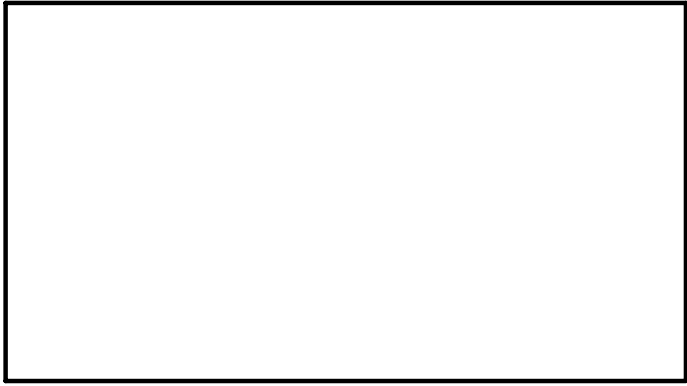
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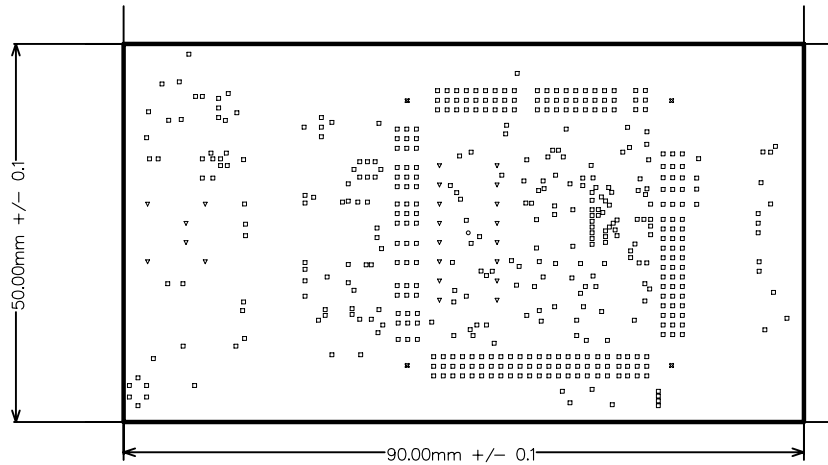
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Drawn By:	N. Beev
DATE	18/09/2018
Checked By:	C. Lesquillier (13/09/2018)



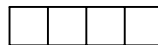
Bottom Poste



Symbol	Count	Hole Size	Plated	Via/Pad
□	473	0.30mm (11.81mil)	PTH	Via
▽	22	0.90mm (35.43mil)	PTH	Pad
⊗	4	2.70mm (106.30mil)	PTH	Pad
○	1	1.20mm (47.24mil)	NPTH	Pad
	500 Total			



Number	EDA-03803-V2
Drawn By:	N. Beev
DATE	18/09/2018
Checked By:	C. Lesquillier (13/09/2018)



Print Date 18/09/2018 10:19:31  
SCALE: 1:00  
Altium Designer Rev 18.0.12.696

Components 145  
Pins 567  
Vias 473  
Holes 500  
Nets 74